IC Fab Lab Manual

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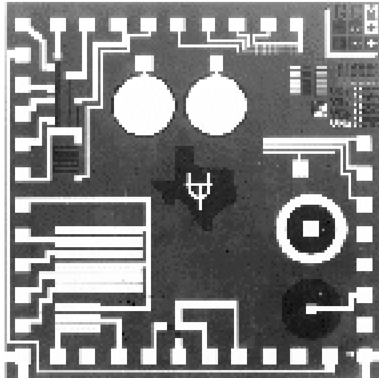
The University of Texas at Austin

Microelectronics Fabrication Teaching Laboratory
Laboratory Manual



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Preface

The Microelectronics Fabrication Laboratory has now been in operation here at UT for almost fifteen years; even so, it is still a lab course which requires constant updating. This course has a number of objectives, chief among them your exposure to basic silicon device processing. You will be required to make use of information from many areas: solid state physics, chemistry, electrical engineering, and computer science. Regardless of your future intentions, we feel the material covered in lecture, and your experiences in the lab, will be very valuable. The use of integrated circuits is pervasive, and knowledge of how they are made is an important compliment to your knowledge of how they can be used.

This laboratory is a synthesis of the work of a number of people. Similar laboratories at Caltech (under the supervision of Prof. Jim McCaldin and Prof. David Rutledge) and at the University of Illinois (originally developed by Prof. Ben Streetman) have provided both inspiration and guidance. Industrial support has been provided by Bell Laboratories, Advanced Micro Devices, Motorola, and Texas Instruments. Both TI and Monsanto have provided silicon wafers for our use. The Semiconductor Research Corporation has also provided generous support for the development of our new mask set. The technical staff (under the supervision of Mr. Harold Traxler and Marty Ringuette) has provided invaluable assistance in setting up and maintaining the lab equipment. The help of Philip Cheung, Doug Miller, Jeff Meitz, Stu Wentworth, Carl Kyono, Doug Holberg, and Garrett Neaves in designing the experiments is also gratefully acknowledged.

This lab is quite different from any other of the labs in your ECE curriculum. The processing we do is very complicated, and there will be frequent, and often very subtle, problems associated with it. You must be very patient and **methodical** at all times. Since we have essentially only one set of equipment, you must also be very careful. Please feel free to make suggestions that you think will help improve the lab.

Updates to this manual are made as necessary; make sure to check the World Wide Web version of the lab manual at:

http://weewave.mer.utexas.edu/DPN_files/courses/FabLab/Fab_Lab_Manual/TOC.html

Dean Neikirk
Fall, 1999

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I. Introduction: Lab Rules

filename: INTRO

A. Laboratory Notebooks and Reports

One important objective of this laboratory is learning how to keep a good lab notebook. You have undoubtedly been told in your other lab courses the importance of keeping an accurate (and comprehensive) account of your work, but I cannot possibly overstate this point. Anyone who works in research and development must keep a complete notebook: many of the companies you may someday work for will in fact require this, and will keep possession of the notebook. Many patent decisions have been based on the worker's lab notebook (or lack of it). Your notebook should be like a diary, recording what you do, and why you did it. Especially in I.C. processing, you should feel free to speculate as to the causes of process failures, of which there will be many. You will frequently learn more from these failures, and your attempts to correct them, than from a process that works perfectly the first time. *It is crucial, however, that your notebook accurately records everything you did.* A good test of your work is the following question: could someone else, versed only in the general processing arts, use your notebook to repeat your work, and obtain the same results? For that matter, could you come back six months later, read your notes, and make sense of them? If you can answer yes to these two questions, you are keeping a good notebook.

To make things easier, you **must** buy a specific lab notebook for this class. This is a duplicate notebook with carbon paper; at the end of each lab you will be required to tear out the duplicate pages and turn them in to the TA for grading. The Co-Op has these notebooks. Your notebook should be neat, but informal. There is no need to copy information from this lab manual into your notebook, except as it reflects what you do. Put in notes on procedures, why you do things, what you observe, and speculations and conclusions. The following rules apply to your notebook:

1. Everything must be written in INK.
2. **Date** every page as you record your work.
3. All data and notes must go DIRECTLY INTO THE NOTEBOOK. The duplicate pages will be collected at the end of each lab period. LOOSE LEAF SHEETS OR SCRAP PAPER SHOULD NEVER BE USED, AND WILL NOT BE ACCEPTED.
4. Label all graphs and tables.
5. Write only on one side of each page. All writing should be LEGIBLE. Leave room for comments by the TA.
6. Each student must keep her/his own lab notebook.
7. If a particular experiment has pre-lab questions, you **must complete them before the lab period begins**. Record your answers in the lab notebook.

The TA's will deduct 5 points from your score if these rules are not strictly adhered to.

Laboratory Reports

SEE UPDATES IN REPORT SECTION

In addition to your lab notebook, after completion of certain stages in the device processing sequence (this will often take several lab periods) you must submit a **Lab Report**. The Lab Report should be typed; it is similar to your Senior Lab technical memos, but not as formal. The Lab Report should contain the following:

1) Experiment title, dates performed, and your lab partner's name.
2) Summary of experimental objectives.
3) Experimental processing procedure: DO NOT SIMPLY RECOPY THE CONTENTS OF THIS LAB MANUAL. A <u>very short</u> summary of important points is sufficient, with emphasis on any changes to the process given in the Lab Manual. You should attempt to explain the reasons any process changes were made, as well as any unusual results in the actual processing. **Normally this section should not exceed about two pages, and may be shorter in later lab reports.**
4) Data: present a summary of the measurements made during the process (originally recorded in your lab notebook) in a **concise, tabular** form. Make sure you do not give numbers to any more than the **proper number of significant digits**. Reference the page numbers in your notebook from which you obtained the raw data. Include sample calculations where necessary. Make clear the estimated accuracy of your measurements.
5) Answers to any specific questions and problems given in the lab manual. Specify any graphs or tables from the lab manual or text book used. Write out any equations used in calculations (but not algebraic details).
6) Brief comments on experimental results. Point out any unusual problems or experimental observations, and explain them if you can.

Further information will be discussed in class.
SEE LAB REPORT GUIDELINES following the Processing Description, p. Reports - 1.

B. Grading

A significant portion of your course grade is your lab grade. Each lab is worth ten points; each Lab Report is worth another fifty points. Grades will be based on the following:

1) **Be present at each lab ON TIME.** This is VERY important. Tardiness will be penalized. Lab work, even more than lectures or homework, cannot be made up in a last-minute rush. Results in the fabrication lab come slowly, and you will need every minute available to you. Arrangements may be made to make up missed lab periods if you have an EXCELLENT excuse.
2) **Be prepared before you come to lab.** There will be assigned readings from the lab manual for each experiment. You MUST COMPLETE these BEFORE coming to lab, since they explain the operating procedures for the equipment you will be using. We may occasionally give lab quizzes over this material, and it will be fair game for the course exams.
3) Keep a complete lab notebook, and answer any pre-lab questions there may be in the experimental description.
4) Lab Reports are due one lab period after you complete the experiment. Unless you have an excellent excuse, late reports will be derated by ten points per week they are late. See the Lab Schedule for due dates.

The lab TA's will take any equipment problems into account when grading your lab work.

ONE FINAL WARNING: I take this lab very seriously, and will STRICTLY enforce all the rules stated in this manual. Whatever you do, don't tell me you didn't know simply because you failed to **read this manual carefully**. Woe will indeed be unto you in those circumstances.

Policy on CHEATING:

It is expected that you will discuss your experimental procedures and results with each other; you are, however, responsible for doing your own written work. All lab notes and Lab Reports should be your own ORIGINAL WORK. If you transpose data collected by your lab partner you should acknowledge this fact in writing, as if this was a reference.

ANY EVIDENCE OF PLAGIARISM OR CHEATING WILL BE TREATED AS GROUNDS FOR FAILURE OF THE COURSE.

C. Safety

We have done everything we can to make this laboratory as safe as possible; we cannot, however, completely protect you without your cooperation. There are very hot furnaces, powerful acids, and strong solvents which are all used, so you must be careful. If you do not show sufficient regard for safety, you will be told to leave the lab, and your grade will suffer accordingly. This section of the lab manual is intended to give some general guidelines, but the most important item is your COMMON SENSE.

THE UNIVERSITY OF TEXAS AT AUSTIN'S LAB SAFETY MANUAL
YOU SHOULD ALSO REFER TO THE MANUAL FOUND ON LINE AT:
http://www.utexas.edu/business/oehs/resources/labman/

OTHER UPDATES TO THIS SECTION CAN BE FOUND ON-LINE AT:

http://weewave.mer.utexas.edu/DPN_files/courses/FabLab/Fab_Lab_Manual/SAFETY.html

--Wear glasses whenever you are in the laboratory.
If you do not ordinarily wear glasses, get a pair of safety glasses from the apparel cabinet when you put on your lab coat.

--**Never** wear shorts or open shoes to this lab. You must always wear long pants and regular shoes when you work in this lab to help insure your safety.

--Keep all the chemicals, whether in beakers or bottles, under the hoods at all times.
Before beginning any work, make sure the water is running in the sink and leave it running at all times. Whenever working under the hoods you should wear the green acid/solvent resistant gloves over your normal gloves. When you finish, rinse the gloves in running water, then remove them, and finally rinse your normal gloves. If you think any liquid has penetrated the gloves, remove them and thoroughly wash your hands. The large sink in the lithography room is more convenient for rinsing your arms than the fume hood sink.

--Never mix an organic solvent with an acid: the combination may explode.
Always rinse chips with high purity water between etching steps and solvent cleaning steps. Acids should be diluted with water in a large beaker, and then poured down the drain very slowly, with the sink water running. Solvents such as ethanol may be poured down the drain with water dilution. **Acetone should NOT be poured into the city drains**.

HYDROFLUORIC ACID

We use a 10% hydrofluoric (HF) acid mixture for etching SiO_2. HF is **EXTREMELY DANGEROUS,** and we use it **ONLY IN THE HF ETCHING HOOD. AT NO TIME**

IS ANY OTHER PROCESSING TO BE DONE IN THIS HOOD. One major problem with HF is the fact that it does not hurt immediately after exposure. When it does begin to hurt a few hours after exposure, it is too late. It will slowly eat through tissue over the course of several days, until it reaches bone, where it is neutralized by calcium. It is excruciatingly painful.

Although an HF burn is very serious, it is also very easy to prevent. Only when the acid is left in contact with the skin for an extended period is it dangerous. Our procedure is very simple: always wear the green gloves when working at the HF etch station, and rinse them with water frequently. When you finish, rinse thoroughly, and finally rinse your hands and arms. The etch station itself is designed to minimize the chance of exposure, but always be VERY CAREFUL. I have never seen a serious HF accident, but this is only because all the labs I have worked in treat it with healthy paranoia. Please do not break my record.

If an accident does occur, there is both a safety shower and eyewash next to the main door. For any chemical splash onto a person's face, they should immediately go to the eyewash and activate it. You should put your face into the water stream and rinse for at least several minutes. For whole body splashes, pull down on the safety shower handle, and leave the water on. A non-injured person should use the phone next to the spill kit to call for emergency help if necessary:

DIAL 9911 FOR EMERGENCY HELP.

TELL THE OPERATOR YOU ARE LOCATED AT THE UNIVERSITY OF TEXAS IN ENGINEERING SCIENCES BUILDING ROOM 214

NOTIFY ME AT ONCE IN CASE OF ANY ACCIDENT.

Please see the Materials Safety Data Sheets (MSDS) in Section IV (p. 192) of this Lab Manual for more information.

II. Experiments: Single Diffused Device Fabrication

filename: FABINT

Introduction

In order that you may understand the flexibility which planar technology affords the circuit designer, we have designed a set of test masks (the Holberg Masks, see p. Masks-1) for use in this lab. This mask set contains device test structures, resolution bars, and alignment verniers. The devices fabricated include several MOS transistors, as well as diodes and MOS capacitors. We will also check diffused resistors, metal step coverage, and metal and contact resistance. In addition to the device chips, we will process, in parallel, unpatterned test chips. These samples will allow us to make several measurements we could not make on our device arrays. You will start with four chips, two identical n-type samples and two identical p-type samples. You will pattern one each of the n-type and p-type chips, as described below, to make your device arrays. The remaining two chips will serve as materials properties test (MPT) samples allowing you to determine such properties as oxide thickness, doping concentration, sheet resistance, and junction depth. Several of these measurements would be destructive or not possible on the patterned device array chips. This is why we process the MPT samples in parallel with the device samples.

Processing Description: Device Array Chips

Starting with an oxidized wafer, a pattern will be etched through the oxide using Mask Level 1 (p. Masks-5) and the Photo-Resist (PR) process outline in OP-L for use with the Positive Resist. The wafer will then be subjected to a boron or phosphorus ambient at high temperature so that the dopant will diffuse into the silicon through the holes in the oxide, forming doped regions on the wafer in those areas delineated by Mask 1. This diffusion is known as the predeposition or "predep" diffusion (see OP-D and OP-E). The rear surface of the wafer will be protected with oxide in this diffusion. We will use both n-type and p-type substrates to facilitate comparisons of device characteristics during the testing phase of the experiment.

After the wafer has been suitably cleaned, it will then be subjected to another diffusion, called the redistribution or "drive" diffusion, this time without the dopant source. The idea here is to redistribute the dopant such that its concentration is more uniform. This diffusion will be initiated in an oxygen atmosphere so that another layer of oxide is grown simultaneously on the wafer to protect the doped regions. See OP-F.

The next step in our wafer fabrication will use a second photoresist (PR) process using Mask Level 2 (labeled **G** for "gate" in the upper right corner of the mask), p. Masks-6, to delineate areas for growth of a high quality gate oxide. After resist processing, a buffered HF (BHF) etch will completely remove previously grown oxides, leaving a clean silicon

surface over the gate region of our MOSFET and over our MOS capacitors. The resist will then be cleaned off, and the Dry Oxide Furnace used to grow a thin, high quality oxide. We will perform these gate oxide growths with chlorine injection to improve the quality of the gate oxide.

After gate oxide growth, a third PR process using Mask Level 3 (labeled **C** for "contact" in the upper right corner of the mask), p. Masks-7, will be used to cut holes down to the doped regions in the silicon, through which contacts can be made. Aluminum will then be vacuum evaporated over the entire wafer, and a 4th PR process utilized to etch the contact pattern using Mask 4 (labeled **M** for "metal" in the upper right corner of the mask), p. Masks-8.

Once the front metalization pattern is etched, aluminum will be evaporated onto the backside of the chip to help form the substrate contact. Before metalization we damage the back with sandpaper to help insure an ohmic contact will be formed (strictly speaking, the damage will insure that any Schottky diode formed between the aluminum and the silicon will be very leaky).]

Finally, you will form the ohmic Al-Si contacts by annealing. This is a process in which the components of a system are heated to a temperature below the system's eutectic point. (The melting point of a given alloy of one substance in another depends upon the percentages of the materials present. That point on a phase diagram of temperature vs. percent of each parent material present where a temperature minimum occurs in the liquidus line is known as the eutectic point.) The eutectic point for the Al-Si system is 576°C. You will use a temperature of 450° which permits the aluminum atoms to move around and spread more uniformly over the silicon surface. In addition, during annealing, the aluminum can diffuse into the silicon itself. This will ensure low resistance contacts to the silicon devices.

This concludes the device processing.

Processing Description: Materials Properties Test Chips

Starting with the oxidized wafers, the ellipsometer is used (see OP-R) to measure the initial field oxide thickness. After measurement, a simple pattern is etched through the oxide. This pattern will simply uncover one-half of the MPT samples. A predep (at the same time as your device chips) is then performed. We can now measure the sheet resistance of the predep layer using the four-point probe (see OP-H). Note this allows you to infer the sheet resistance of the doped regions on your device chips.

After cleaning, we will subject the MPT samples to a drive-in diffusion (again, at the same time as the device samples). After the drive, the oxide thickness grown during the drive is measured, then completely etched away in buffered HF. You will now be able to measure the sheet resistance of the doped layer (note it will not be the same as it was after the predep), as well as the resistivity of the wafer substrate (by measuring on the half of

the substrate that was covered with oxide during the predep). Again, this will give you information about certain areas on your device chips at this point in the process.

The last high temperature process step performed on your samples is the gate oxide growth step. The oxide-free MPT samples will be included with your device chips during the TCE dry oxidation (see OP-C). After completion, you will measure the oxide thickness grown on the MPT chips; this will give you the gate oxide thickness on your device samples. We will also use a technique called junction grooving (see OP-N and Ghandhi, pp 196-197 (1st edition)) to find the depth of the p-n junctions below the wafer surface. Note this step is destructive, requiring the grinding of a groove in the surface of your MPT samples. If possible, after determining the junction depth, you will etch all oxide off the MPT chips so that the sheet resistance of the doped layers can be measured again. This is necessary since the dopants will have diffused during the high temperature gate oxidation. Note that based on the measurements made on your MPT samples, you will now have all the materials properties necessary to analyze the devices on your patterned device chips.

General Comments

In order to complete all the processing required, you must keep up with the schedule on pp. F_int-5-7. In particular, there are three steps that will be batch processed, with everyone's chips together: process step 5, lab 4, the predep process; process step 7, lab 5, the drive-in process; and process step 11, lab 7, the gate oxidation process.**You MUST have all necessary processing and measurements done before each of these steps so that you samples are ready for the batch process.** Catch-up lab periods (outside of normal lab times) will be held before each of these critical steps to allow you extra processing time, if necessary.

Before coming to each lab read the appropriate Processing Description, and any operating procedures used in that section. Answer any pre-lab questions assigned. Use the checklist in the Processing Description at all times to ensure that each step is completed. Do not use the checklist as a substitute for reading and understanding all procedures and instructions **BEFORE** lab begins.

Because of limited equipment and space, different groups will do different portions of a process at different times. In particular, some groups will be making measurements on the MPT samples while others are processing their device chips. For example, during lab period 5 two groups will be using the ellipsometer and 4-point probes on their MPT samples, while the other two groups will be performing the 2nd photoresist process (process step 8) on their device chips. In lab 6 these groups will reverse roles.

Always consult your lab TA at the beginning of the lab period for updated processing instructions. Check with the TA if any mistakes are made in processing or if

you do not complete the procedure outlined for that period. Please be considerate of the other groups in the lab, and do not monopolize the processing equipment.

Process Flow Summary

Process Step	Device Chip	Materials Properties Test Chip
Lab 2 & 3	on one p-type, one n-type pre-oxidized chip	on one p-type, one n-type pre-oxidized chip
1		ellipsometric oxide thickness measurement
2	Photoresist 1: diffusion, Holberg Mask Level 1	Photoresist 1: half mask
3	Etch 1st diffusion windows	Etch oxide from half of chip
4	Strip all resist	Strip all resist
Lab 4		
5	p-type sample: phosphorus predep, 20 min n-type sample: boron predep, 30 min	p-type sample: phosphorus predep, 20 min n-type sample: boron predep, 30 min
6	Strip boro/phospho-silicate glass in BHF	Same as device chips; 4-point probe for sheet R
Lab 5 & 6		
7	Both p- & n-type: drive-in, 1100°C, 30 min.	Same as device chips; after drive: oxide thickness
8	PR 2: gate ox pattern, Holberg Mask Level 2	NA
9	BHF oxide etch	Same as device chips; 4-point probe for sheet R
10	Strip PR	NA

(Process Flow Summary cont.)

Process Step	Device Chip	Materials Properties Test Chip
<u>Lab 7 & 8</u>		
11	Gate oxidation: 1100°C, with TCE	Same as device chip; after ox: oxide thickness
12	PR 3: contact windows, Holberg Mask Level 3	NA
13	BHF oxide etch	same as device chip; 4-pt probe for final R_S; junction groove for x_j
<u>Lab 9-11</u>		
14	Backside damage	
15	Strip PR	
16	Front side Al evaporation	
17	PR 4: Metal contacts, Holberg Mask Level 4	
18	Aluminum contact etch	
19	Strip PR	
20	Backside metallization	
21	Form contacts	

Lab Schedule

filename: fall_lab_schd

Week of	Lab	Topic	
Aug. 30	1	Intro to Safety and Facilities	
Sept. 8		**Lab Report 0 DUE IN LECTURE!!**	
		Group A:	Group B:
Sept. 6	2	oxide thickness;	1st PR: diffusion; etching
Sept. 13	3	1st PR; etching	oxide thickness
Sept. 16-17		Catch-up lab; must be ready for lab 4	
Sept. 17-20		**Batch process: Pre-dep; Process Step 5**	
Sept. 20	4	etch; 4-pt probe	
Sept. 23-24		Catch up lab; must be ready for lab 5	
Sept. 24-Sept. 27		**Batch process: Drive-in; Process Step 7a**	
		Group A:	Group B:
Sept. 27	5	oxide thickness; etch; 4-pt probe	2nd PR: gate mask; etching
Oct. 4	6	2nd PR: gate mask; etching	oxide thickness; etch; 4-pt probe
Oct. 7-8		Catch up lab: must be ready for lab 7	
Oct. 8-11		**Batch process: Gate-ox; Process Step 11c**	
Oct. 18		***LAB REPORT I DUE Monday Oct. 18 IN LECTURE!***	
		Group A:	Group B:
Oct. 11	7	oxide thickness; junction depth	3rd PR: contact windows
Oct. 18	8	3rd PR: contact windows	oxide thickness; junction depth
Oct. 25	9	etch windows; front side evap.; 4th PR	
Nov. 1	10	front side Al evap., 4th PR cont.; Al etch; backside Al evaporation	
Nov. 8	11	4th PR, Al etch cont., backside evap cont.; Al anneals	
Nov. 11-12		Catch up lab: must have device fab complete	
Nov. 15		***LAB REPORT II DUE MONDAY Nov. 15 IN LECTURE!!***	
Nov. 15	12	Electrical Testing	
Nov. 22	13	Electrical Testing	
Nov. 29	14	Electrical Testing	
Dec. 3		***FINAL LAB REPORT III DUE FRIDAY***	

CLASSES END Fri. Dec. 3

REPORTS DUE:
- Oct. 18: Lab Report I, Process and results to date
- Nov. 15: Lab Report II, Complete process summary
- Dec. 3: Lab Report III, Final test results

filename: PROCESS

Device and Materials Properties Test (MPT) Chips
Processing Description

MOSFET/CAPACITOR/DIODE/DIFFUSED RESISTOR FABRICATION

Lab 2 and 3: First Photoresist, Diffusion Mask
Required reading: pp. 7 - 43, , OP-L, OP-O, OP-R

1. Obtain (two each) clean, oxidized n- and p-type silicon chips from your T.A. Record the number scribed on the back of each chip. Store the chips in a clean petri-dish until you are ready to use them.

   Note: Wafers are cleaned using OP-J and wet oxidized for an oxide to serve as a diffusion mask. See the Wet Ox Log Book for oxidation time used on your sample.

   On the oxidized samples provided, measure the oxide thickness on one n-type and one p-type sample using the Filmetrics system and OP-R. Make sure to record the sample numbers on these chips in your notebook, and keep track of them as the materials properties test chips(here after referred to as the MPT chips). **Also make sure to mark these chips so you can tell which half will be oxide-etched and doped.** You will use the other two chips for your device arrays.

   DEVICE CHIP NUMBERS:
   n-type device chip #________
   p-type device chip #________

   MPT CHIP NUMBERS AND INITIAL FIELD OXIDE THICKNESS:
   n-type MPT sample #________: t= ________Å
   p-type MPT sample #________: t= ________Å

2. PHOTO-RESIST I (PRI): Windows for 1st diffusion.

____ a. Bake-out the sample for 5 mins. in post-bake oven. (This step may be skipped if sample did not go through any wet processing prior to PRI).

____ b. Spin-on the Adhesion Promoter (HMDS) at 4000 rpm for 30 sec.

____ c. Spin-on positive-resist (1350J) at 4000 rpm for 30 sec.

____ d. Pre-bake sample for 10 mins in the Pre-bake oven, 95° C.

____ e. On your device samples, use OP-O to align the sample with the 1st diffusion mask, MASK I, so that its edges are approximately parallel to the edges of your chip.

____ f. Using the same OP, do a 15 sec exposure to UV. CHECK LOG BOOK FOR UPDATED EXPOSURE TIMES.

____ g. Dip the sample in developer for 60 sec followed by two rinses in the high purity H_2O beakers. Blow dry the sample. Inspect pattern under microscope.

minimum resolution line: ________ µm
minimum resolution space: ________ µm

____ e'.On your materials properties test chips align the samples to the 50% opaque/50% clear mask so that 1/2 your chip is covered. **NOTE WHICH SIDE OF THE CHIP IS EXPOSED FOR LATER REFERENCE!!!!!!!!**

____ f'. Expose as above.

____ g'. Develop as above.

____ h. Flood expose the chips under the U.V. lamp. Use a 5 sec exposure /pause 5 sec/ 5sec exposure sequence. CHECK FOR UPDATES ON THE TIMING OF THE FLOOD EXPOSURE!

NOTE IF BACK SIDE RESIST COATING PROCEDURE IS USED, IT MUST BE DONE BEFORE POST-BAKE! IF USING RESIST FOR BACK SIDE PROTECTION, FOLLOW THE NEXT TWO STEPS (steps i1 and j1; IF USING THE WAX PROCEDURE, SKIP TO steps i2 and j2. **Check with TAs for updates on these steps.**

****

____ i1. To protect the oxide on the back side of the chip during etching we need to coat it. Resist coating procedure: Working in the small hood, place a VERY SMALL drop of resist on a clean microscope slide. Now CAREFULLY place your chip BACKSIDE DOWN onto the resist. Using forceps, gently press down on the corners of the chip, and rotate the chip to evenly distribute the resist over the back. **CAREFULLY** slide your chip off the the microscope slide (DO NOT TRY TO PULL IT VERTICALLY OFF) and inspect for good resist coverage. Place the chip vertically in the teflon carrier with the other chips; now procede to post bake.

____ j1. Post-bake samples for 15 min in the Post Bake Oven, 125° C.

****

____ i2. Post-bake samples for 15 min in the Post Bake Oven, 125° C.

____ j2. To protect the oxide on the back side of the chip during etching we need to coat it. Wax coating procedure: In the small hood turn the hot plate on, set for LOW, and allow it to warm up. Place a clean microscope slide on the hot plate, and place a SMALL amount of clear wax on the slide by rubbing the wax stick on the slide. Now CAREFULLY place your chip BACKSIDE DOWN onto the molten wax. Using q-tips, gently press down on the corners of the chip, and rotate the chip to evenly distribute the wax over the back. **Quickly** slide your chip off the the microscope slide (DO NOT TRY TO PULL IT VERTICALLY OFF) and inspect for good wax coverage. The chip will cool quickly, then place it back in your petri dish.

****

Check your pattern by examining your chips with the Nikon Microscope; make sure you know what is photoresist and what is bare substrate.

3. Etch windows for 1st diffusion (all chips).

____ a. Etch oxide in buffered HF (BHF) for approximately 4 min. Etch rate is about 1000 Å/min. When etching is complete the etched areas should de-wet. Rinse and blow dry. **Check with TAs for updated etch times.**

____ b. Clean the photoresist off the chips after etching: rinse in acetone/ethanol/HP H_2O.

minimum resolution line etched: ________ µm
minimum resolution space unetched: ________ µm

4. Strip remaining photoresist (all chips).

____ a. Place chips in the boat inside the Plasmod (see OP-K) and oxygen ash at full power for 5 min. THIS STEP MAY BE OMITTED: CHECK WITH THE TA's!

Lab 4: Boron, Phosphorus Predeposition
Required reading: OP-A, OP-D, OP-E, OP-F, OP-H

PRELAB QUESTION: ANSWER IN LAB NOTEBOOK BEFORE LAB PERIOD BEGINS!

1. The operating procedures for the pre-dep furnaces specify that you use several different flow meter settings. Using the settings given find about how long it takes to completely displace the volume of gas contained in the furnace tube for each flow rate given. Why might each of theses rates have been chosen?

2. For the sheet resistance measurements on the MPT chips, what are the dimensions you should use in order to find the correction factors CF_d and CF_t in order to convert I and V measurements into true sheet R's? Remember you have doped only one half of the sample, and think about where the current will be confined to flow.

5. Pre-deposition

____ a. Immediately prior to predep, perform a 5 sec BHF etch to remove any native oxides.

____ b. On the n-type substrates, perform a 30 min. boron pre-dep (see OP-A, OP-D).

____ c. On the p-type substrates, perform a 20 min. phosphorus pre-dep (see OP-A, OP-E).

6. Predep sheet resistances and Oxide thickness measurement.

____ a. Strip boro-silicate/phospho-silicate glass from all chips with BHF etch:
n-type chips (boron-doped): 30 sec.
p-type chips (phosphorus-doped): 15 sec.
Rinse and spin dry.

____ b. Measure the sheet resistance of the doped layers on the materials test chips using the 4 point probes and OP-H. Make three (3) measurements at slightly different locations on each chip to check the accuracy of the measurement.

n-type substrate, boron-doped: R_S = __________

p-type substrate, phosphorus-doped: R_S = __________

Record these results in the appropriate Furnace Log Books.

____ c. Using the Filmetrics system and OP-R, measure the oxide thickness on both the doped and undoped sides of your MPT chips.

ox thickness, n-type : doped__________ undoped__________
ox thickness, p-type : doped__________ undoped__________

Labs 5 and 6: Drive-in, 2nd Photoresist pattern.
Required reading: OP-F, OP-L, OP-O, OP-H, OP-R

PRELAB QUESTION: ANSWER IN LAB NOTEBOOK BEFORE LAB PERIOD BEGINS!

1. How long does it take to completely displace the volume of gas contained in the furnace tube for each flow rate given? Why might each of theses rates have been chosen? During the drive, roughly how much time is spent in an oxidizing ambient, and how much in a non-oxidizing one?

7. Drive-in

____ a. On all your samples, perform a 30 min. drive-in at 1100° C:

i) initiate drive-in in O_2, 1 liter/min., for 5 min.
ii) conclude with N_2, 1 liter/min., for 25 min. (see OP-A, OP-F)

____ b. After drive, on your material properties samples measure the oxide thickness using OP- R. Make sure to measure the thickness on both the doped and undoped sides of the samples.

ox thickness, n-type : doped__________ undoped__________
ox thickness, p-type : doped__________ undoped__________

8. PR II: Gate oxide pattern, Mask 2, on device chips ONLY.

____ a. Dehydration bake, 5 min. at 125° C (use the Post Bake oven).

____ b. Spin on adhesion promoter, 4000 rpm, 30 sec.

____ c. Spin on photoresist (1350J), 4000 rpm, 30 sec.

____ d. Pre-bake: 10 min, 95° C.

____ e. Using OP-O, align the sample pattern to the pattern on Mask 2. Be very careful; do the rotational alignment first, then the x-y alignment. Use the split-field technique.

____ f. Expose for 15 sec.; **check for current exposure time.**

____ g. Develop (60 sec), rinse, blow dry. **Inspect pattern with Nikon microscope! Is it OK??**

x registration error: ________ µm
y registration error: ________ µm

____ h. Flood expose: use a 5 sec. exposure, pause 5 sec., then 5 sec. exposure.

____ i. Post-bake: 15 min, 125° C.

9. Etch all oxide from gate/capacitor areas and all oxide from materials chips.

____ a. Using buffered HF, perform a 4 min. oxide etch. When complete the back side of the chip should de-wet. Remember to include your materials properties test chips. **Check with TAs for updated etch times.**

____ b. Inspect pattern with microscope.

____ c. On the material properties test chips (which should now be completely free from all oxides) measure the sheet resistance of both the doped and undoped sides of the chips using OP-H. Again take three different measurements.

n-type : B doped R_S = _______ undoped R_S = _______
p-type : P doped R_S = _______ undoped R_S = _______

Record these results in the appropriate Furnace Log Books.

10. Strip Photoresist from device chips: NA Fall 1988

____ a. Rinse sample: acetone/ethanol/HPH_2O.

____ b. Strip sample in Plasmod (OP-K), full power, 5 min. STEP MAY BE OMITTED: CHECK WITH TA's!

____ c. Inspect pattern with microscope.

Lab Report I (see p. 34) is due on SOON: see course schedule for exact date!

Labs 7 and 8: Gate Oxidation, 3rd Photoresist Pattern, Contact Windows

Required reading: OP-J, OP-N, OP-C

11. Gate oxide growth on ALL chips.

____ a. Immediately prior to oxide growth, perform a 5 sec. BHF etch, rinse, dry.

____ b. Immediately after the BHF dip perform the RCA cleaning step for inorganic contamination using a 5:1:1 solution of HP H_2O: 30% H_2O_2: 37% HCl for 5 min. (see OP-J). Rinse thoroughly in HP H_2O.

Note: TA's should check temperature of Dry Ox Furnace prior to this step.

____ c. Grow oxide in Dry Ox Furnace, as per OP-C, but before pushing samples into furnace center zone, allow them to heat in the furnace neck for 5 min. Make sure to oxidize all four of your samples. Perform the oxidation WITH CHLORINE INJECTION, for the time indicated by your lab TA.

time in O_2:__________;
time in O_2 + TCE:__________;
time in N_2:_________.

Record in Furnace Log Book!!!!

____ d. On your material properties test samples, measure the thickness of the oxide just grown using OP-R. Measure the oxide thickness over both doped and undoped regions.

n-type, thickness : doped______ undoped______
p-type, thickness : doped______ undoped______
Record in Furnace Log Book!!!!

12. PR III: Contact window pattern, Mask 3, on device chips only.

____ a. Dehydration bake, 5 min. at 125° C.

____ b. Spin on adhesion promoter, 4000 rpm, 30 sec.

____ c. Spin on photoresist (1350J), 4000 rpm, 30 sec.

____ d. Pre-bake: 10 min., 95° C.

____ e. Using OP-O, align the sample pattern to the pattern on Mask 3. Be very careful; do the rotational alignment first, then the x-y alignment.

____ f. Expose for 15 sec. Check for current exposure time.

____ g. Develop (60 sec) in AZ developer, rinse, blow dry. **Inspect for proper results with Nikon microscope.**

minimum resolution line: _________ µm
minimum resolution space: _________ µm
x registration error: _________ µm
y registration error: _________ µm

____ h. Flood expose (5 sec. exposure, 5 sec. pause, 5 sec. exposure).

Note: Do NOT cover back side of chip with wax or photoresist.

____ i. Post-bake: 15 min., 125° C.

13. Etch oxide from contact windows and oxide from materials properties test samples.

____ a. Using the BHF etch station, perform a 4 min. oxide etch. When complete the back side of the chip should de-wet.

____ b. Inspect pattern with microscope.

____ c. Using OP-H, measure the sheet resistance of the doped layers on your materials properties test samples.

n-type substrate, B-doped : R_s = _________________
p-type substrate, p-doped : R_s = _________________

____ d. Using OP-N, measure the junction depth on the doped side of your material properties test chips.

n-type substrate, B-doped R_j = ________________

p-type substrate, P-doped R_j = ________________

Lab 9, 10, and 11: Complete Device Fabrication
Required Reading: OP-G, Vacuum Evaporation

14. Back side damage chip (device samples only for rest of processing).

____ a. Place chip face down on a piece of filter paper. While holding one corner down with your forceps, CAREFULLY damage the back side of your chip with the fine sandpaper provided. It is not necessary to damage a large area of the chip.

15. Strip photoresist.

____ a. Rinse sample: acetone/ethanol/HPH_2O.

____ b. Strip sample Plasmod (OP-K), **1/2 power**, 5 min. STEP MAY BE OMITTED: CHECK WITH TA's!

____ c. Inspect pattern with microscope.

minimum resolution line etched: ________ µm
minimum resolution space unetched: ________ µm

16. Aluminum evaporation

____ a. CAREFULLY follow OP-G to vent and raise the vacuum system bell jar.

____ b. Load the aluminum evaporation filament with 4 inches of aluminum wire. The wire should be very carefully wrapped around the center of the filament. **See TAs for help.**

____ c. Clamp your sample front-side down using the clips on the the chimney cover plate. Remember to put at least one clear glass slide on the cover plate to double check metallization thickness.

____ d. Follow OP-G to pump down the vacuum system. Allow 15 min. for vacuum to improve.

____ e. Evaporate aluminum: see lab TA for up-date on evap system operation.

____ f. After concluding evaporation, allow 5 min. for the filament to cool, then vent and remove your sample as per OP-G.

17. PR IV: Aluminum contact pattern, Mask 4.

____ a. Spin on adhesion promoter, 4000 rpm, 30 sec.

____ b. Spin on photoresist (1350J), 4000 rpm, 30 sec.

____ c. Pre-bake: 10 min., 95° C.

____ d. Using OP-L, align the sample pattern to the pattern on Mask 4.

____ e. Expose for 25 sec. **Note the increased exposure time used when exposing resist over metal. Check for current exposure time.**

____ f. Develop (60 sec), rinse, dry. **Inspect for proper pattern with Nikon microscope.**

minimum resolution line: _________ µm
minimum resolution space: _________ µm
x registration error: _________ µm
y registration error: _________ µm

____ g. Flood expose (5 sec. exposure, 5 sec. pause, 5 sec. exposure).

____ h. Post-bake: 15 min., 125° C.

18. Aluminum etch.

____ a. Etch aluminum in Transene Type A Aluminum Etchant. Etch time should be approximately two minutes; continue etch until pattern is clearly visible.

____ b. Rinse thoroughly in HPH_2O.

19. Strip photoresist.

____ a. Rinse sample: acetone/ethanol/HPH_2O.

____ b. Strip sample Plasmod (OP-K), **1/2 power**, 5 min. STEP MAY BE OMITTED: CHECK WITH TA'S.

____ c. Inspect pattern with microscope.

minimum resolution line etched: _________ µm
minimum resolution space unetched: _________ µm

20. Metallize chip back side.

____ a. Follow OP-G to vent and raise the vacuum system bell jar.

____ b. Load the aluminum filament with metal (4" wire length).

____ c. Load sample back side down. Remember to put in a blank slide to monitor the evaporation.

____ d. Follow OP-G to pump down the vacuum system. Allow 15 min. for pump down.

____ e. Evaporate aluminum at 40 amps for 2 min.

____ f. After completing evaporation, allow 5 min. for cooling, then vent and remove sample as per OP-G.

21. Form ohmic contacts and anneal gate oxide.

____ a. Set N_2 flow in small annealing furnace #1 to 100 with steel ball (160 cc/min). Flush furnace for 5 min. before loading samples.

____ b. Load samples into quartz boat, push into center of furnace. Anneal for 15 min. at 450° C.

Note: This furnace controller gives temperature in **Fahrenheit**, so be careful. Sample fabrication is now complete. You should now proceed to the Lab Report section in the Lab Manual. **Make sure to refer to any updates on what testing is actually required given in class!!!**

Lab Report II (see p. 35) is due SOON, see course schedule for date!

Laboratory Report Guidelines

filename: REPORTS update

This is an update containing further details on your lab reports. You should still read Section A, p. Intro-1, that contains the old information on lab report format; most comments made there are still valid.

GENERAL COMMENTS:

As usual, where ever possible check your results based on "reasonableness" arguments. You should always find several other ways to check each measurement you have made, for instance by checking the expected process results against Ghandhi or the Lab Manual, by checking the process log books in lab, and by performing any calculations that are reasonable. REFERENCE ALL OUTSIDE SOURCES OF INFORMATION, AS WELL AS THE LOCATION OF YOUR RAW DATA IN YOUR LAB NOTEBOOK. As a general rule, the statement "as expected," when used in reference to the results of some measurement, is NOT acceptable, unless you state *explicitly* why it is expected.

MAKE COPIES OF THE TABLES INCLUDED HERE (pp. Up-6 through Up-8) FOR USE IN EACH LAB REPORT. **I STRONGLY ADVISE YOU KEEP A COPY OF ALL YOUR COMPLETED TABLES AND DRAWINGS, IN ADDITION TO WHAT YOU TURN IN.**

TWO COPIES OF REPORT 1 AND 2 MUST BE SUBMITTED!

CRITIUQES

You are not only be responsible for writing lab reports, but also for **critiquing** other group's reports. The quality of your understanding of what you do and observe is influenced by how hard you work on the Lab Reports, and can be greatly enhanced by exposure to alternative views. This is not just a scheme to get you to grade the reports for me; I will read and grade the reports, as well as reading and grading your critiques. **Except for Lab Report 0 you and your lab partner(s) will prepare the reports as a team, submitting one report per group.** You will, however, do your critiques individually.

General comments about critiques:

You will receive a copy of another group's lab report. Read the report carefully; editorial comments should be made in the margins of the report. Try to flag things you do not understand, weak and/or unsupported arguments, or incorrect conclusions. Also flag good points, or conclusions you agree with but did not notice when you wrote your own report.

Fall 1999 Updates on Reports:

LAB REPORT "ZERO": DUE IN CLASS, Weds. Sept. 8:
Every individual must do this assignment

Construct a flow chart which illustrates the major steps in our fabrication procedure.

Separate flow charts for the MPT and Device chips should be used, but they should be drawn in parallel to illustrate the common (and dissimilar) processes used for the two sets of chips. You should read the **entire** Processing Description Section of the Lab Manual, and make sure you understand the sequence of steps necessary to fabricate our devices. This assignment is critical to the successful completion of your devices.

Critique of Lab Report 0, due in class, Monday, Sept. 20.

The remaining reports should be done in formal collaboration with your lab partner(s):

LAB REPORT I (one report per lab group; two copies required), due Monday, Oct. 18:

Give a **very brief** overview of the processing; outline form is adequate. In the tables, **do not** fill out the "Calculated" sheet resistance boxes. **Concentrate on reporting the experimentally measured values, along with their uncertainty estimates.**

Critique of Lab Report I, due Monday, Nov. 1:

Look carefully at significant figures and justification for the precision and accuracy of the measurements.

LAB REPORT II (one report per lab group; two copies required), due Monday, Nov. 15:

Concentrate on presenting your calculations for sheet resistance and junction depth. Use "purely" theoretical means to find the diffusion profiles. Do **NOT** use empirical formulas for pre-dep results. Discuss the impact of possible concentration-dependent diffusion on your measurements, and the agreement or disagreement between theory and actual measurements.

Critique of Lab Report II, due Friday., Dec. 3.

LAB REPORT III and TESTING (one report per lab group; one copy required) due Friday Dec. 3:

Perform only the basic qualification procedure for your MOSFETs as outlined in the DEVICE TROUBLE SHOOTING section of the Lab Manual. Discuss this procedure and your results in Lab Report III. You may skip the rest of the Device Testing Section, but read it, as well as the complete guidelines for Lab Report III in the Lab Manual.

Questions for Lab Report 1

Discuss the following points in your lab reports. Please phrase your answers to questions 2 and 3 below in such a way as to re-state the question being answered. A **short** discussion is appropriate.

1. Give a brief overview of the process to date; an **outline format** would probably be most appropriate. You should clearly identify the location of each device in the Holberg Mask Set (pp. 38-47), along with the function of Masks 1, 2, 3 and 4 in terms of how they form the devices. You should include **accurate, clearly labeled cross-sectional drawings** of the MOSFET, diffused diode, and MOS capacitor with guard ring, at the following points in the processing: after step 4 (immediately before pre-dep); after step 6 (immediately before drive); and after step 10 (immediately before gate ox). Based on data gathered from your MPT chips you should be able to give some of the actual thicknesses of various layers in the devices.

2. Discuss the geometry correction factors necessary to interpret the four point probe measurements. Be careful to distinguish between the doped and undoped sides, and how this affects the dimensions you use for calculations of sheet resistance. Which measurements can be used to calculate a resistivity, and which can only be used to determine sheet R? Based on the measurements made so far, for what areas of the chip can you give an actual doping concentration, either background or diffused? Use this data to fill out the appropriate blocks in Tables II and III. Make sure you do not quote numerical results of precision greater than what you actually think is significant. You should give in the Tables an approximate value for the uncertainty. A short discussion of how you calculated each value (both the quantity of interest and its associated uncertainty) should be given.

3. Discuss the ellipsometric results. Again, make sure to consider in which cases your results are reasonable. The index of refraction calculated from your measurements is a good place to start. Reference from a book any materials properties you need to interpret the results. Fill out all the blocks in Table I that you have sufficient information to determine. Again you must determine how many significant figures you have actually measured to. You should give in the Tables an approximate value for the uncertainty. A

short discussion of how you calculated each value (both the quantity of interest and its associated uncertainty) should be given.

4. Use the information gathered in the lab using the registration verniers and resolution bars on the masks to fill out Table IV. "Statistics" are important here, so indicate in footnotes how many measurements your numbers are based on.

Questions for Lab Report 2

1. Provide ACCURATE, CLEARLY labeled cross-sectional drawings of all the completed devices. You should have enough information to label your device cross sections with actual dimensions in **both the vertical and horizontal directions**. Based on the data you have obtained from the MPT chips, you should be able to fill out several more blocks in Tables I and II; as before, a short discussion of how you calculated each value (both the quantity of interest and its associated uncertainty) should be given.

2. Using information in Ghandhi, calculate the junction depths in your n- and p-type chips. Be very careful, and cross check any approximations you might use concerning diffusion constants, etc. Once you have calculated a diffusion profile you can use the Irwin curves to find the final sheet resistance of the diffused layers; compare this calculated value to your measured values, and discuss any differences. Show your junction grooving results, and compare them to your calculations.

3. Use the information gathered in the lab using the registration verniers and resolution bars on the masks to complete Table IV. "Statistics" are important here, so indicate in footnotes how many measurements your numbers are based on.

Questions for Lab Report 3: READ THESE BEFORE YOU BEGIN TESTING

1. Draw diagrams for each device showing the relationship between the the device layout and the electrical connections to the device. Where necessary make sure that you consider connections through the backside of the chip. Indicate how the electrical test connections are made between the probe stations and the device-under-test (the DUT).

2. Device parameter extraction equations should be properly referenced, and great care used in determining what approximations have been used. The Lab Manual and OP's contain some of the necessary equations, but you will probably need to use some 339 equivalent text to get everything right.

Perform only the basic qualification procedure for your MOSFETs as outlined in the DEVICE TROUBLE SHOOTING section of the Lab Manual. Discuss this procedure and your results in Lab Report III. You may skip the rest of the Device Testing Section, but read it, as well as the complete guidelines for Lab Report III in the Lab Manual.

PLEASE NOTE THE SIGN UP PROCEDURE FOR TESTING EQUIPMENT:
For each test station (CV Station; IV Station; Resistance Station) there will be a SIGN UP SHEET posted outside the lab. Please do NOT sign up for more than two time slots at a time.

Table 1: **n-type MPT chips Oxide Thickness Measurements**

Process Step	boron-doped areas		undoped areas	
	thickness (Å)	index	thickness (Å)	index
field oxide				
after pre-dep				
after drive-in				
after gate ox				
Test capacitors: with guard				
without guard				

Table 2: **p-type MPT chips Oxide Thickness Measurements**

Process Step	phosphorus-doped areas		undoped areas	
	thickness (Å)	index	thickness (Å)	index
field oxide				
after pre-dep				
after drive-in				
after gate ox				
Test capacitors: with guard				
without guard				

Table 3: Sheet Resistance Measurements summaries

	n-type MPT chip (boron diffused areas) Sheet Resistance R_S (• per square)		p-type MPT chips (phosphorus-diffused) Sheet Resistance R_S (• per square)	
Process Step	measured	calculated	measured	calculated
after pre-dep				
after drive-in				
after gate ox				
from resistors				
$R_{contact}$ (•)				
bend size (squares)				

Table 4: Undoped Wafer Characterization

	Sheet R (4-pt probe) (•/sq)	ρ (calc) (•-cm)	Background Concentration		
			(4-pt probe) (cm^{-3})	(diode C-V) (cm^{-3})	(cap C-V) (cm^{-3})
p-type chip					
n-type chip					

Table 5: Lithography and Etch Results

	Level 1 Diffusion	Level 2 Gate	Level 3 Contact	Level 4 Metal
PR min line				
PR min space				
Etch min line				
Etch min space				
x reg				
y reg				

Table 6: MOS Device Characterization

	V_{fb}	Threshold Voltage		
	(cap C-V)	(cap C-V)	(long MOSFET #1 I-V)	(short MOSFET #2 I-V)
p-type chip				
n-type chip				

	Transconductance			
	(long MOSFET #1)	(calc)	(short MOSFET #2)	(calc)
p-type chip				
n-type chip				

	"Excess" Surface Charge			
	Q_{ss} (col/cm^2)		Q_{ox} (#/cm^2)	
	w/o guard	w guard ring	w/o guard	w guard ring
p-type chip				
n-type chip				

Holberg Mask Set

filename: MASKS

This section describes in detail the functions of the Holberg Mask Set, shown with all four layers overlaid in Figure 1, and level-by-level in Figure 2, Figure 3, Figure 4, and Figure 5. Each functional block on the chip is discussed separately. These blocks are:

i) Alignment, resolution, and registration patterns
ii) Metal step coverage and leakage patterns
iii) Diffused resistor and contact resistance test structures
iv) Diffused diodes
v) MOS capacitors
vi) Thick and thin oxide MOSFETs

Alignment, resolution, and registration patterns

The purpose of this part of the chip is to allow accurate alignment of each mask level to preceding levels already patterned, as well as to evaluate the accuracy of the alignment and the resolution of both lithographic and etching processes. The area in the upper right corner of the chip (Figure 1) is used for these purpose. Figure 7 shows a four level composite view of this region of the chip.

Figure 8 and Figure 9 shows diagrams to illustrate how the registration verniers are used to determine mis-alignment. In Mask Level 1 (Diffusion, Figure 2) windows are opened to provide the center part of the verniers; each subsequent level patterns bars on either side of the Level 1 pattern. Misalignment is determined by finding the outer and inner boxes which line up, and counting how many boxes from the end this occurs at. Each box from the end corresponds to 1 µm misregistration.

Figure 10 shows a close up of the resolution bars. By inspecting these patterns using a microscope it is possible to evaluate the performance of our lithographic and etch processes. For evaluating the lithographic process, looking at the smallest bars that are of made up of equal widths of exposed and unexposed resist tells us whether we have over-exposed (open, exposed regions wider than photoresist between the open regions) or under-exposed the resist (open, exposed regions narrower than photoresist between the open regions). Simlar inspection after etch can be used to help determine the extent of undercutting during overetch.

Diffused resistor and contact resistance test structures

The purpose of this part of the chip is to allow us to measure the sheet resistance due to our diffusions, as well as to find contact and bend resistance corrections. The area in the upper left corner of the chip (Figure 1) is used for these purposes. Figure 11 shows a three level composite (diffusion: Level 1; contact: Level 3; and metal: Level 4) view of this region of the chip.

There are four basic structures in this region. Two straight resistors, one short (R_1) and one long (R_2), are used to find sheet and contact resistances. Another serpentine resistor (R_3) is used

to find the equivalent size and resistance of bends. The last structure allows four point measurement of sheet resistance, to help remove contact resistance problems from the measurements. See the TEST section for more details.

Diffused diodes

The purpose of this part of the chip is to allow us to evaluate a diffused p-n junction diode. The region in the lower right corner of the chip (Figure 1) is used for this purpose. There are two diodes of identical size, the top device also having a field relief plate over the oxide covering the surface p-n junction.

MOS capacitors

The purpose of this part of the chip is to allow us to evaluate the quality of our gate oxides. The region in the upper center of the chip (Figure 1) is used to make two MOS capacitors at the same time we grow the gate oxide for our MOSFETs. There are two capacitors of equal metal plate and thin oxide areas. The right device, however, also has a diffused guard ring around the perimeter of the capacitor that will reduce somewhat the effective area of the capacitor (and hence its capacitance) compared to the MOS cap without gurad ring.

Thick and thin oxide MOSFETs

The purpose of this part of the chip is fabricate two MOSFETs with different gate lengths, as well as a thick oxide MOSFET to help evaluate the quality of our field oxide. The area in the bottom left corner of the chip (Figure 1) is used for these purposes. Figure 12 shows a four level composite view of this region of the chip. The upper MOSFET (Device 1) has a longer channel than the device below it (Device 2). All three MOSFETs share a common source connection through the upper-most pad shown in Figure 12.

Critical Mask Dimensions:

MOSFET channels:

Device 1	800µm x 30µm
Device 2	800µm x 20µm

MOS cap w guard ring: 600µm diam.

MOS cap w/o guard ring: 550µm diam.

Diode diffusion diam.: 550µm

Diffused resistors (straight):

Device 1	250µm (l) x 25µm (w)
Device 2	500µm (l) x 25µm (w)

Registration verniers: 1µm increments

Table 7: Resolution bars

line number	line	following space	line number	line	following space
1	2 µm	2 µm			
2	2 µm	3 µm	8	10 µm	10 µm
3	3 µm	3 µm	9	15 µm	15 µm
4	3 µm	5 µm	10	15 µm	15 µm
5	5 µm	5 µm	11	20 µm	20 µm
6	5 µm	5 µm	12	20 µm	20 µm
7	10 µm	10 µm	13	25 µm	25 µm
			14	25 µm	

Contact Windows:

Diffusion area: 50µm x 50µm

Oxide window size (metal/semiconductor contact area):
25µm x 25µm

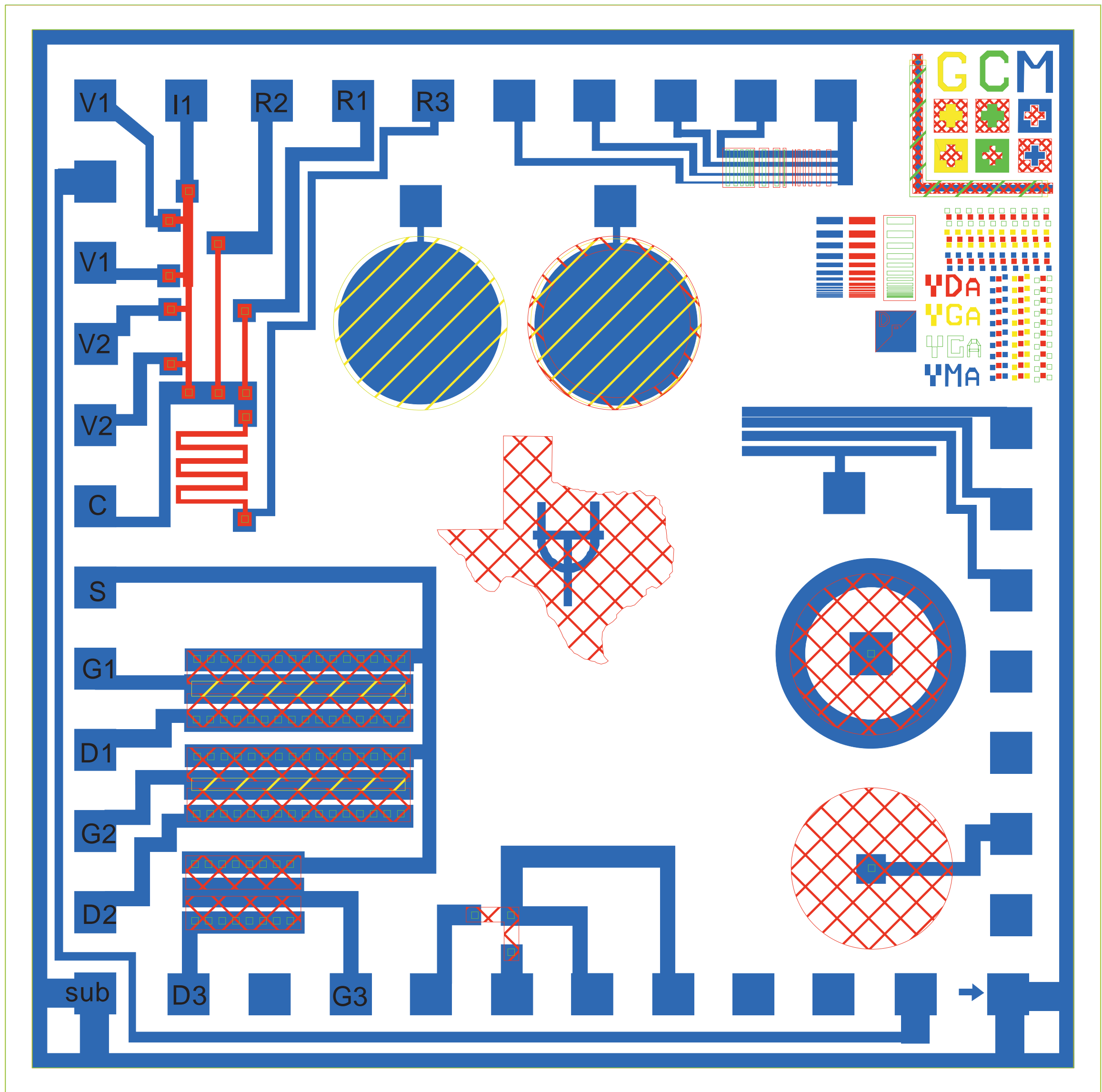


Figure 1: Composite Drawing of Holberg Mask Set.

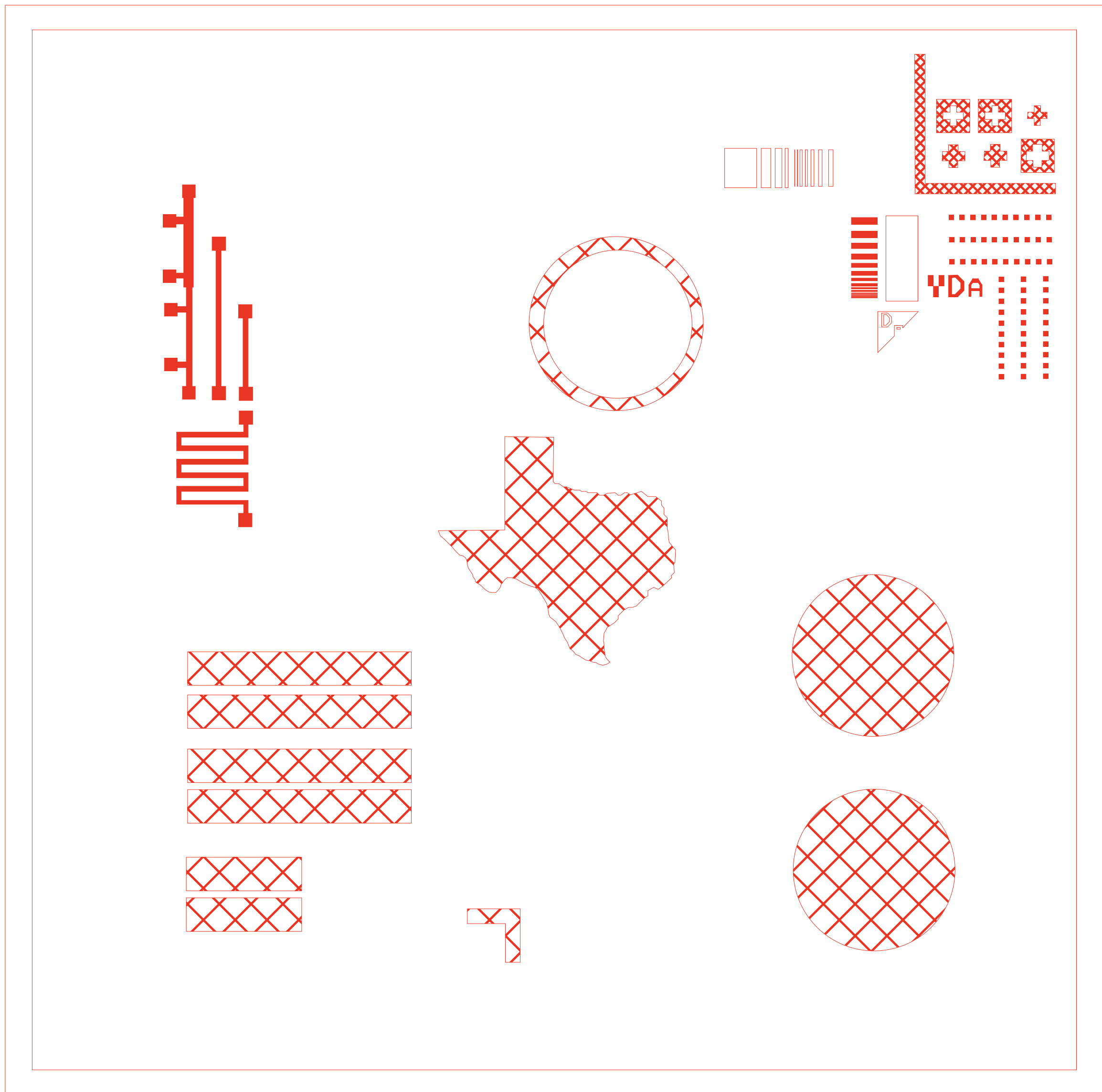


Figure 2: Holberg Mask Level 1, Diffusion

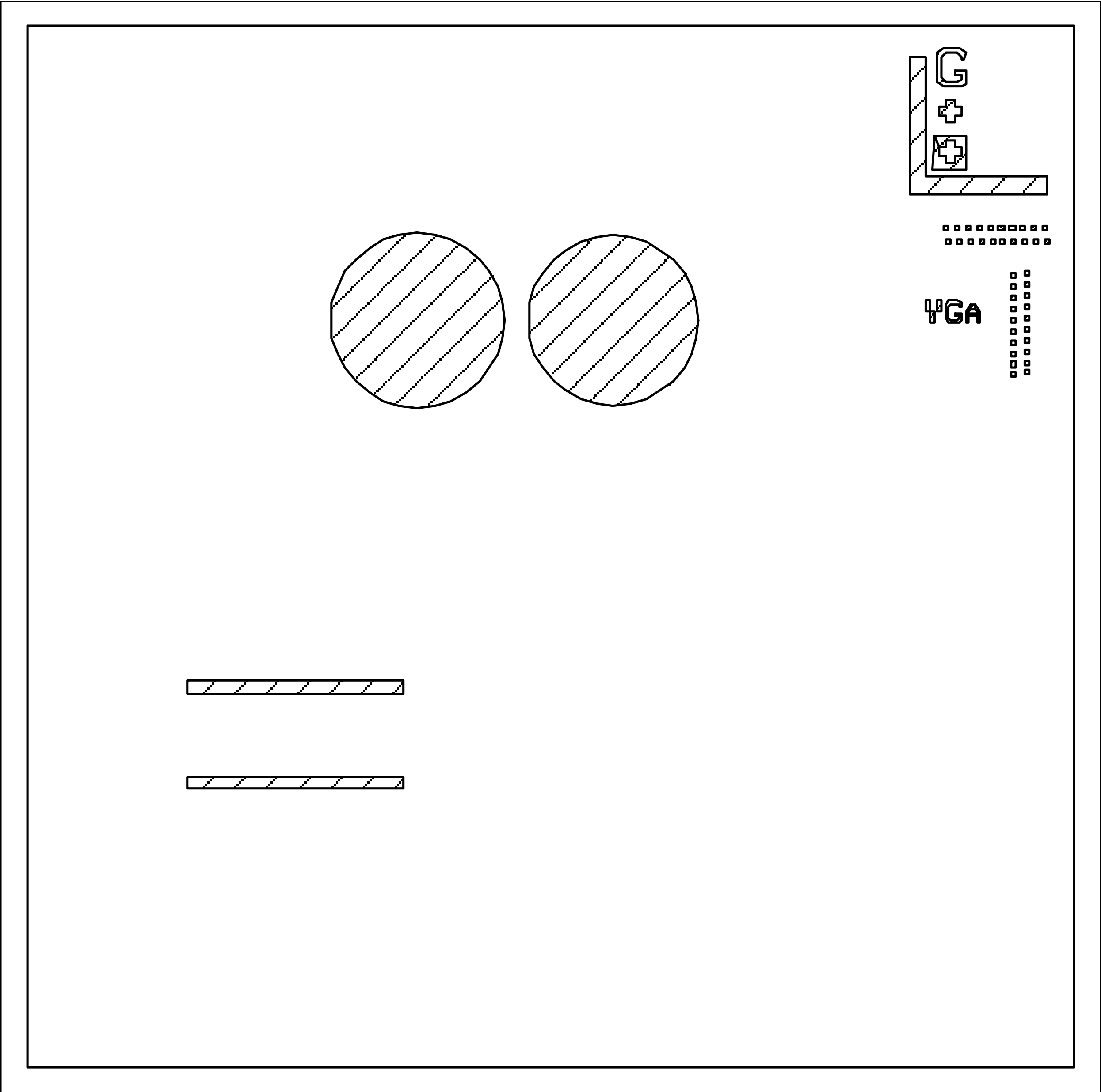


Figure 3: **Holberg Mask Level 2, Gate.**

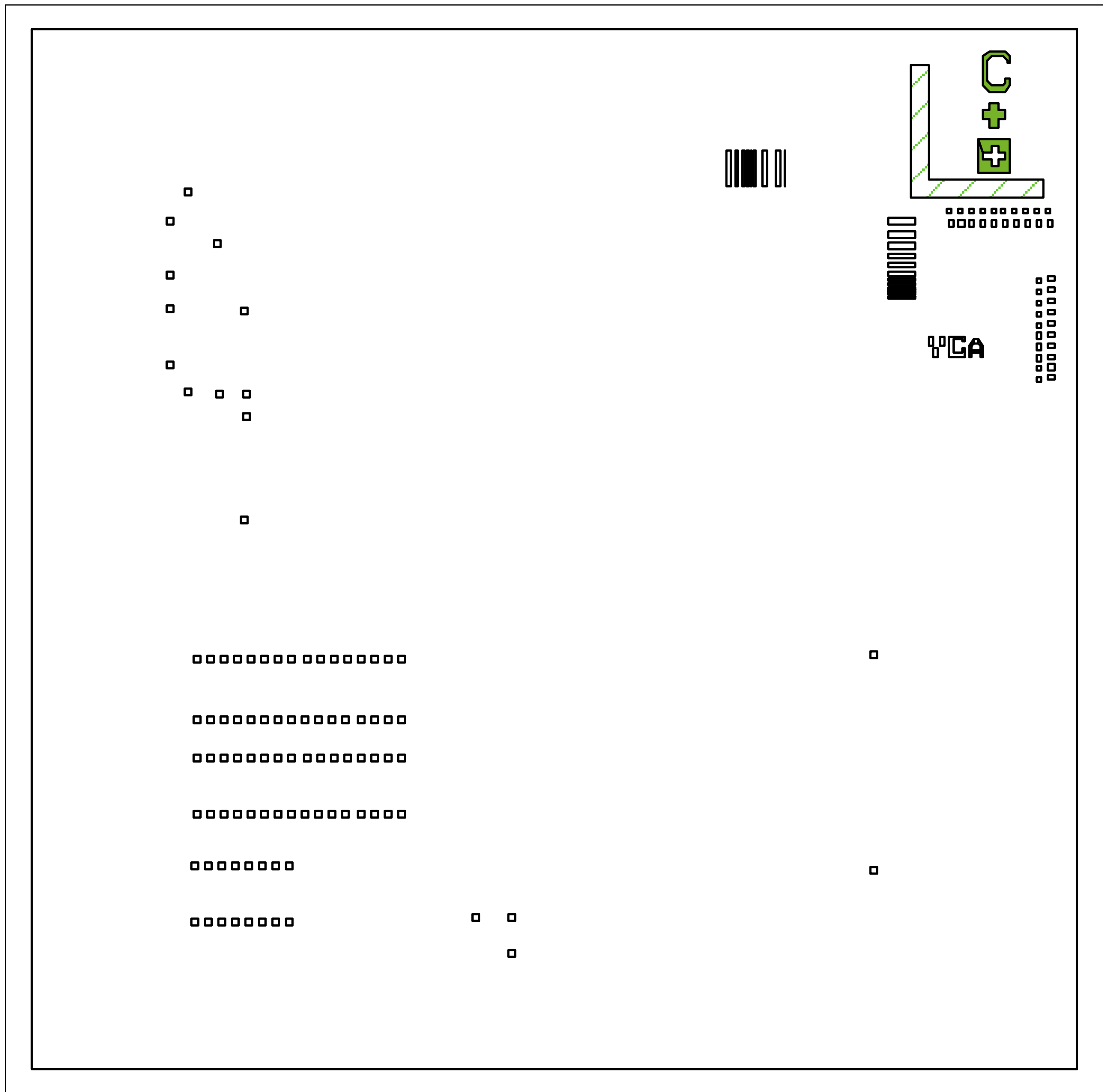


Figure 4: **Holberg Mask Level 3, Contacts.**

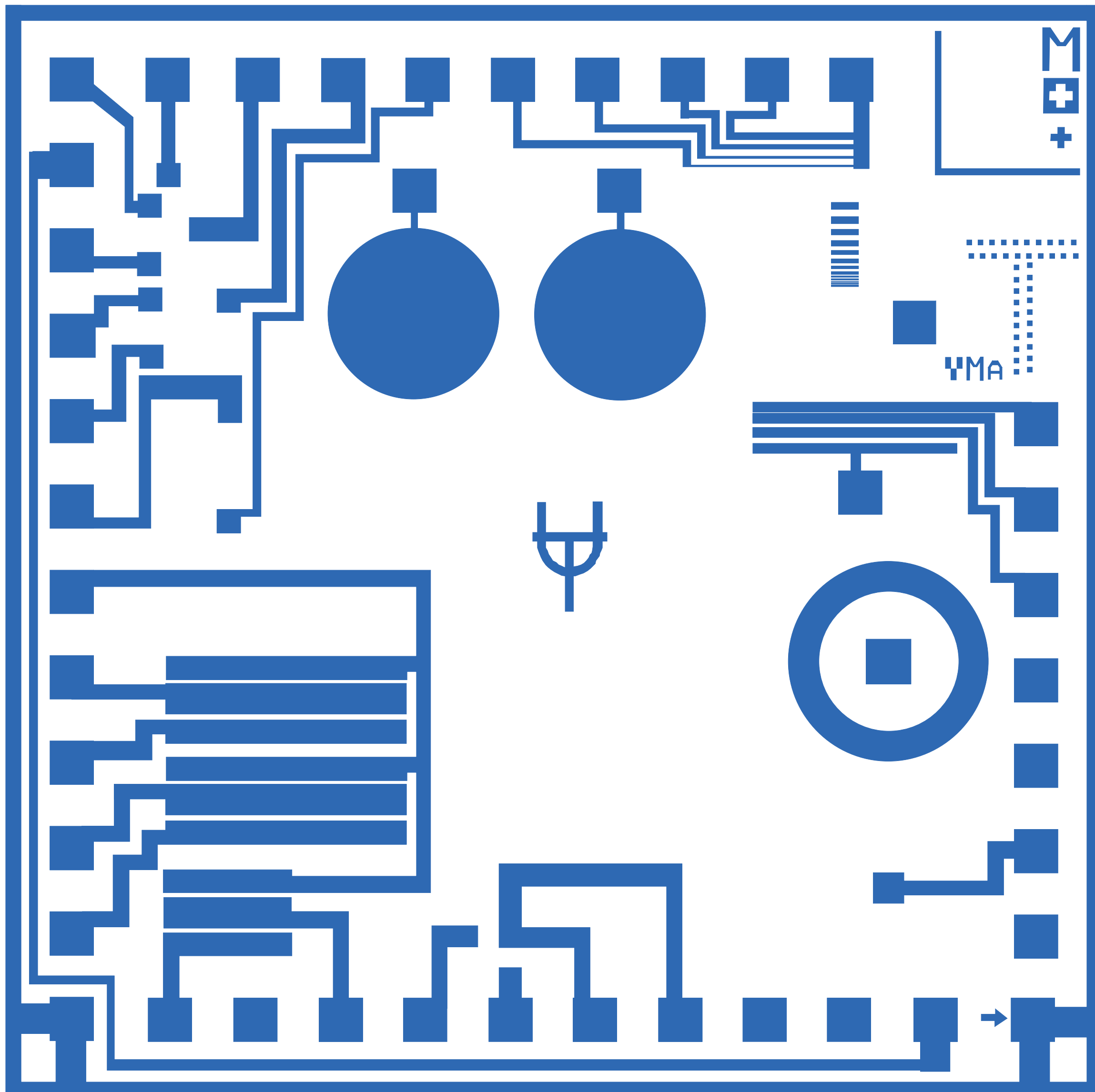
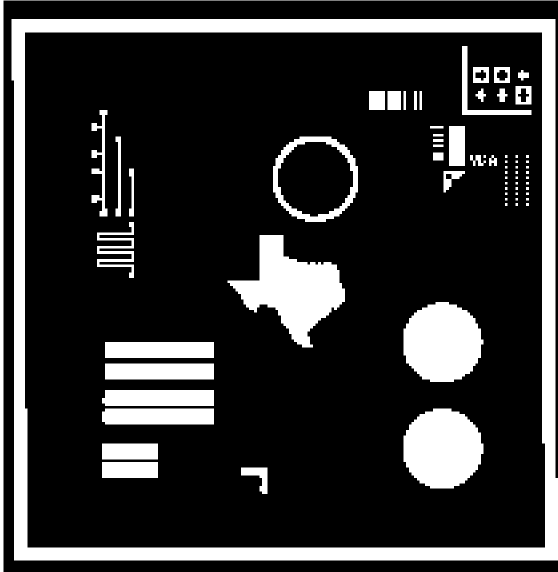
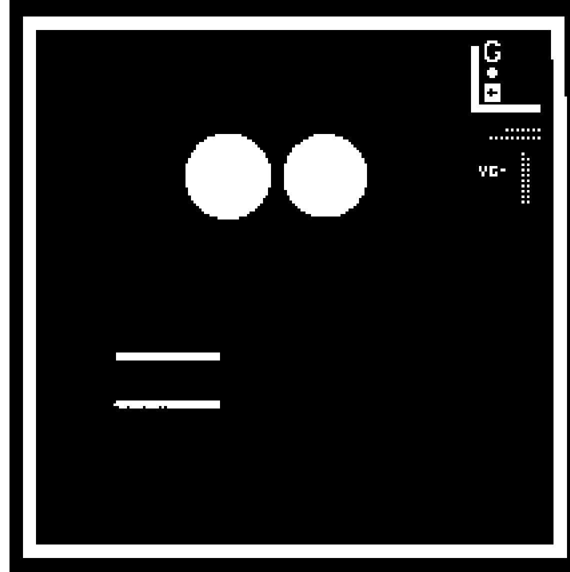


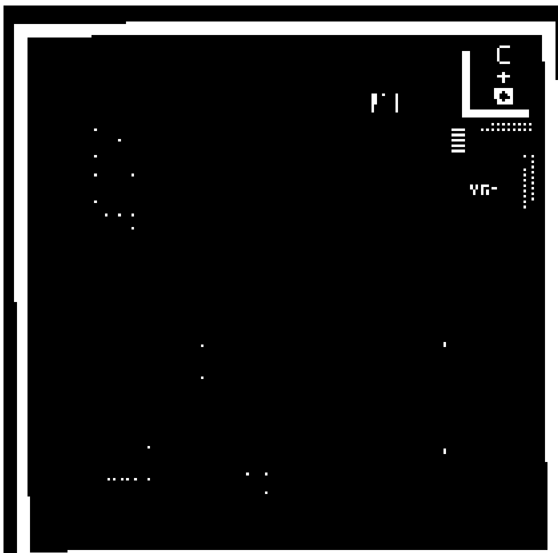
Figure 5: `Holberg Mask Level 4, Metal.`



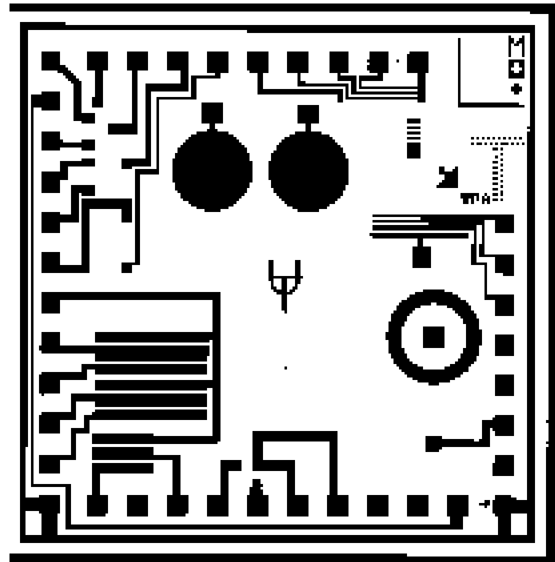
Holberg Mask 1, Diffusion



Holberg Mask 2, Gate



Holberg Mask 3, Contacts



Holberg Mask 4, Metal

Figure 6: Scanned images of the Holberg Masks

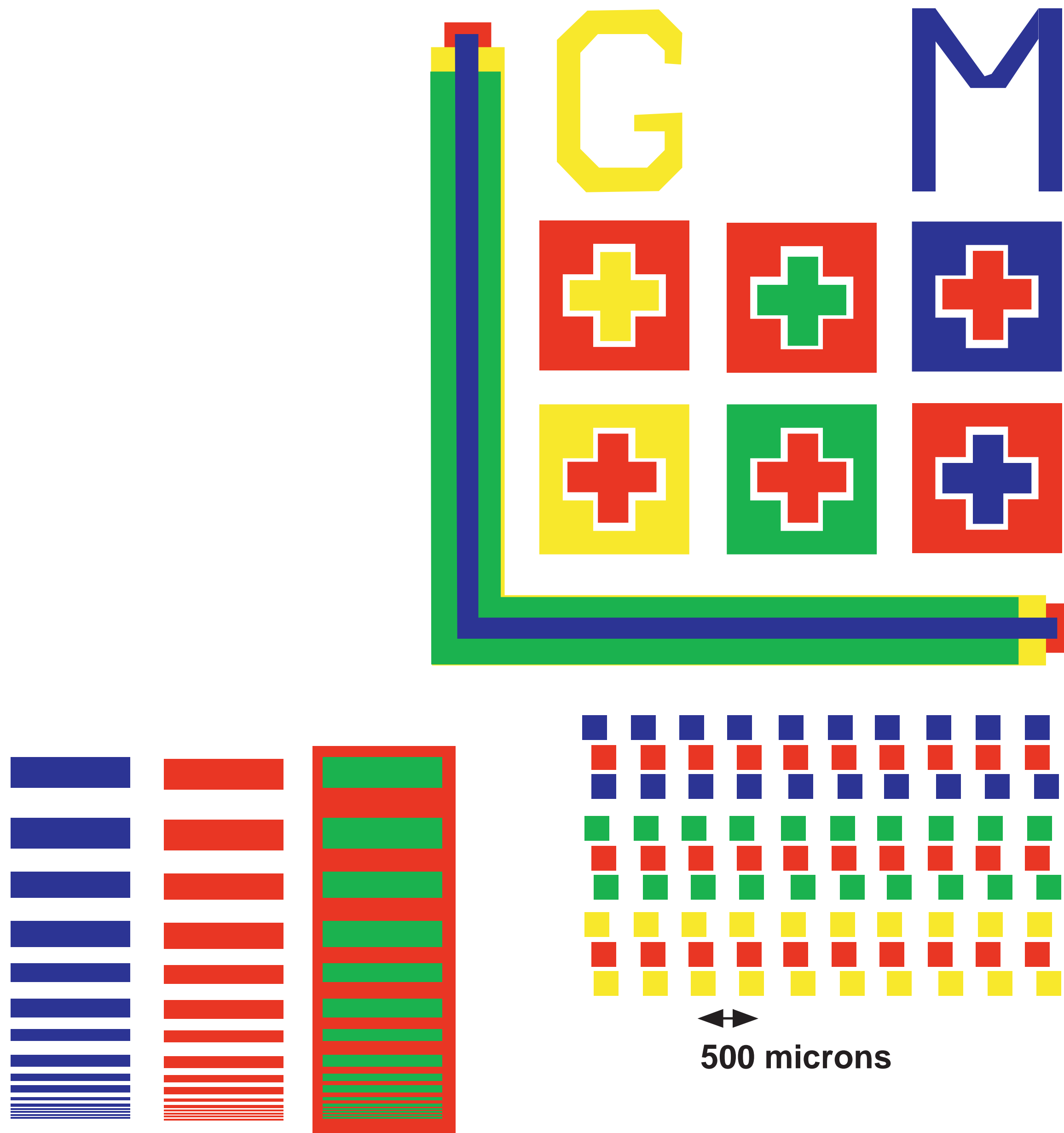


Figure 7: Composite view of alignment and registration patterns of Holberg Mask Set; all four levels are shown superimposed. The scale bar is 50 µm long.

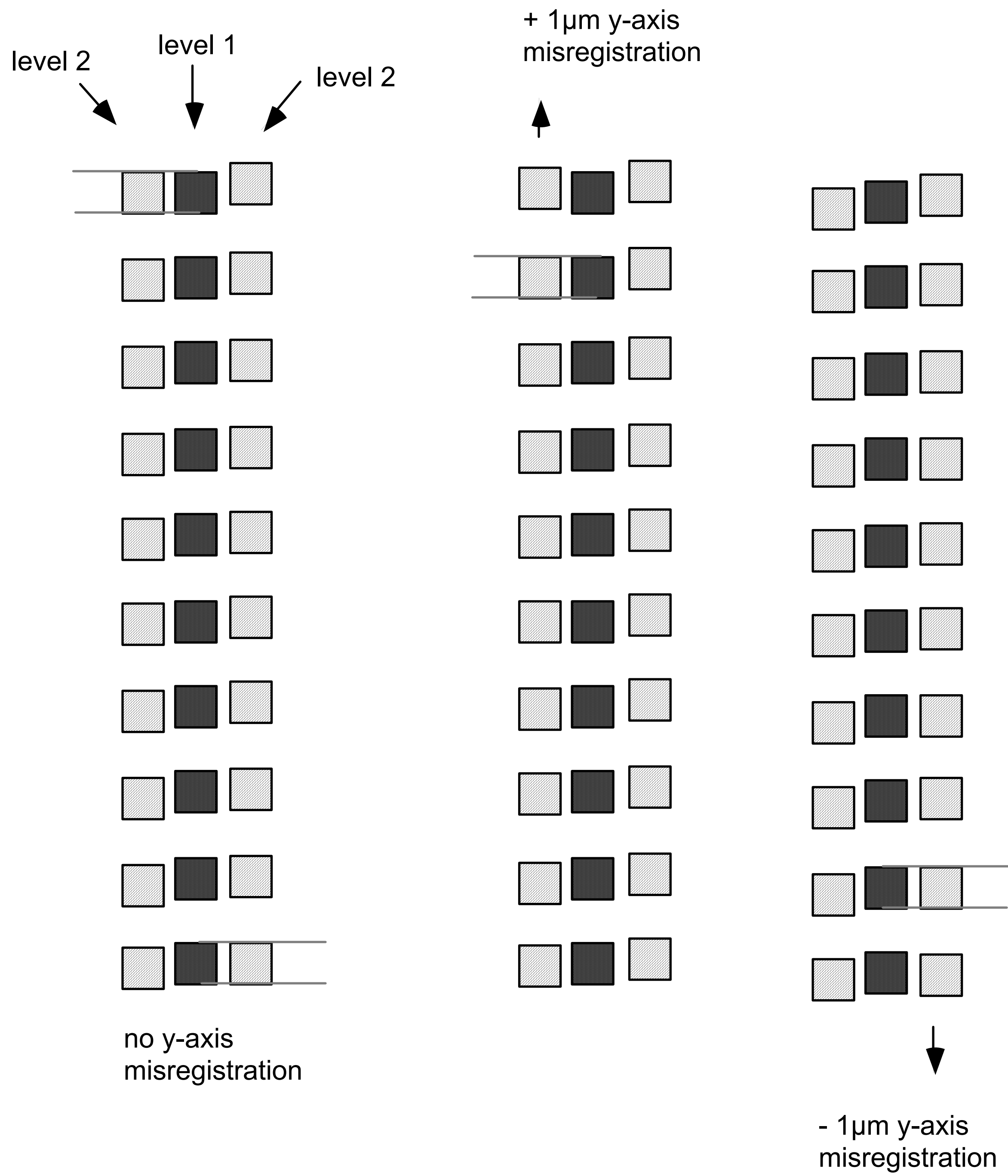


Figure 8: **Illustration of y-axis misregistration verniers. Three cases are shown: zero, +1, and -1 µm misregistration.**

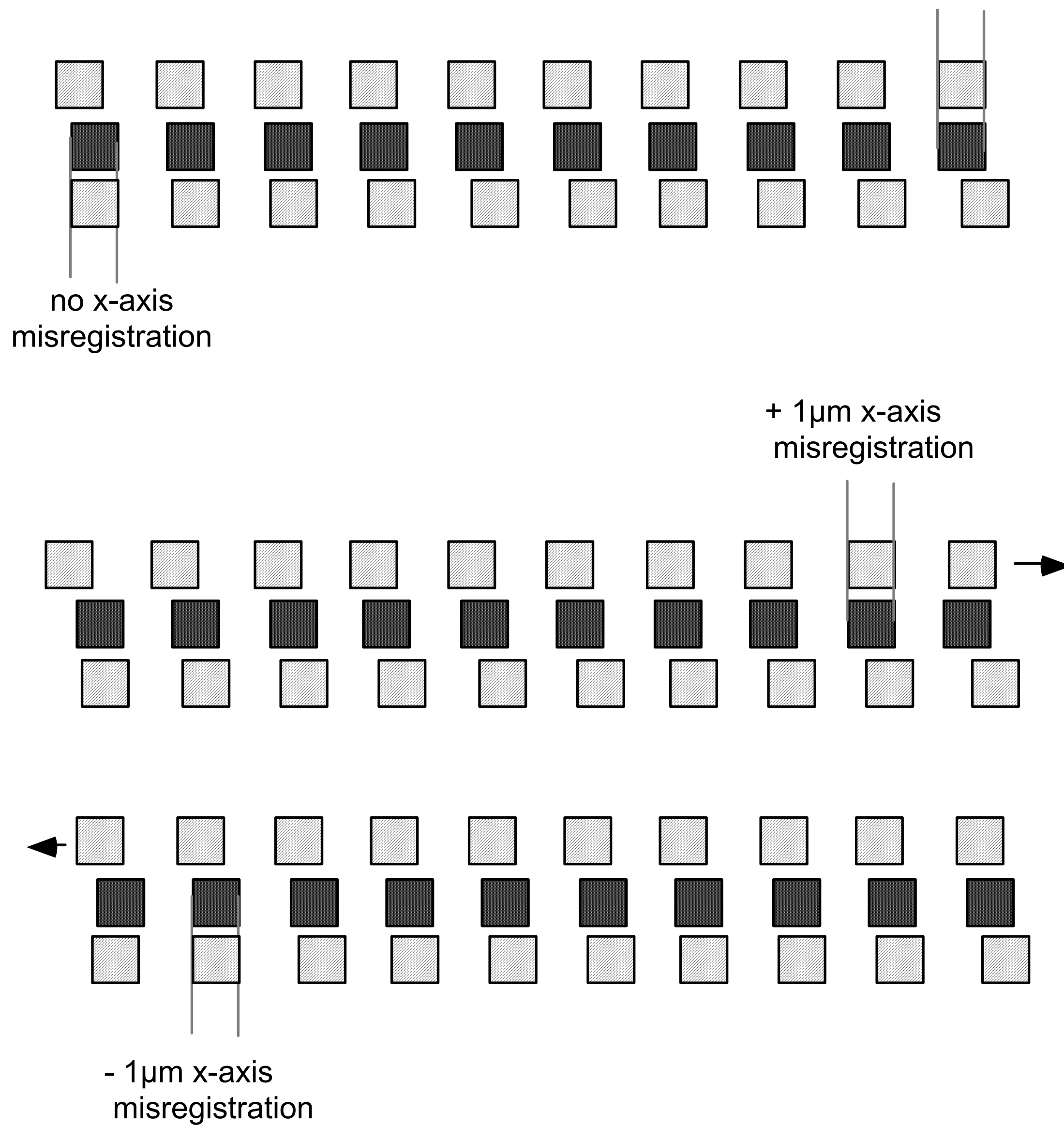


Figure 9: Illustration of x-axis misregistration verniers. Three cases are shown: zero, +1, and -1 µm misregistration.

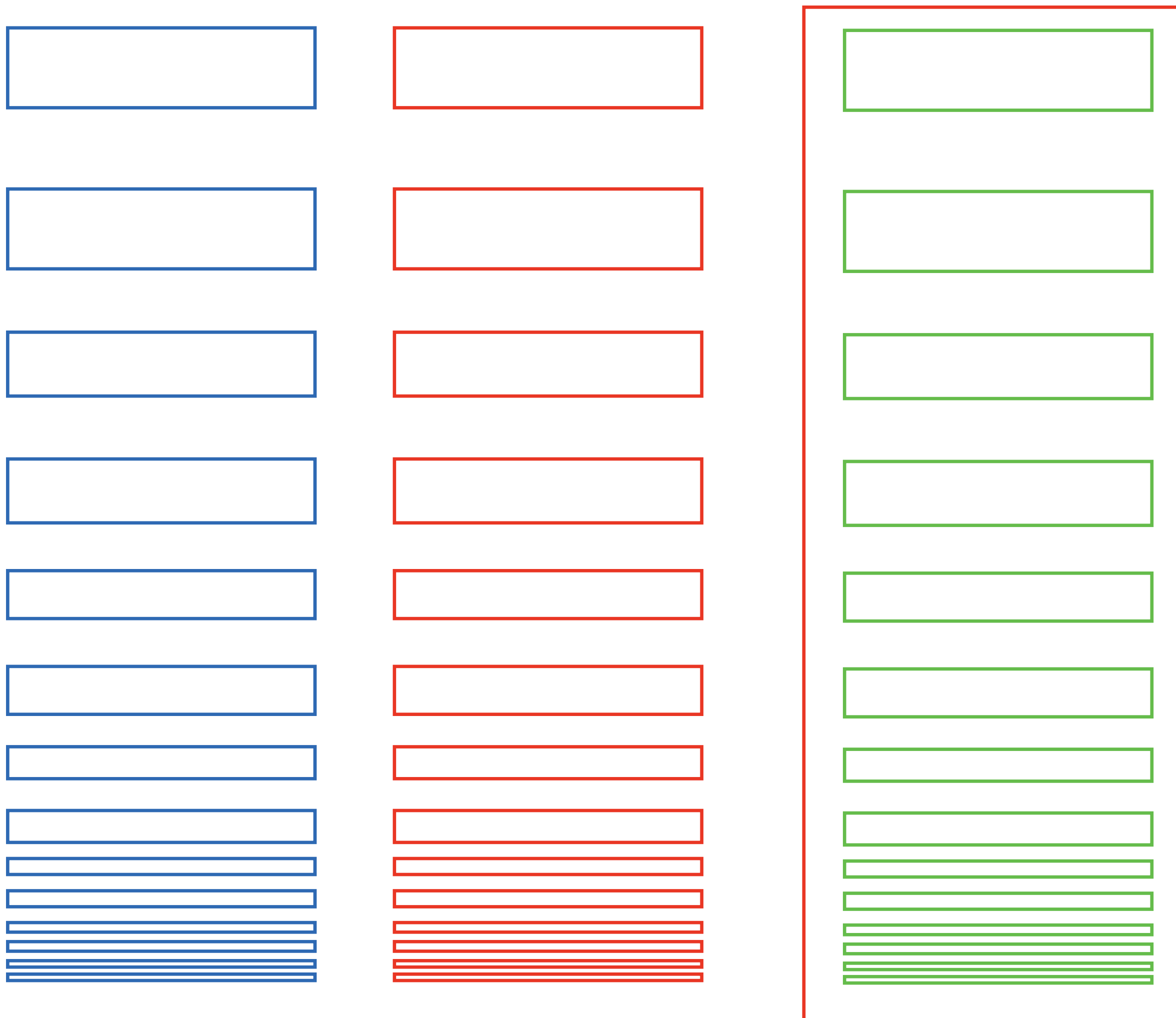


Figure 10: Resolution bars. See Table 7 for dimensions.

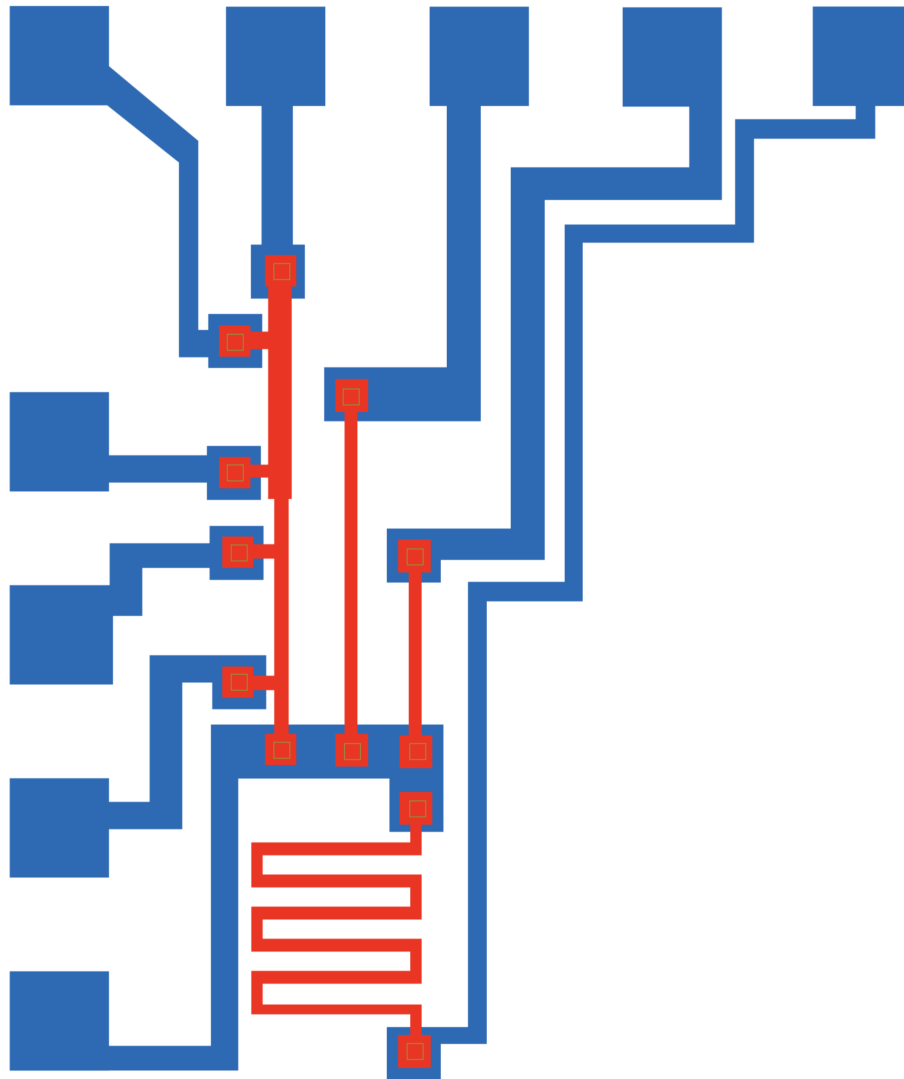


Figure 11: Composite view of resistor patterns of Holberg Mask Set; four levels are shown superimposed: diffusion: Level 1; diffsion: Level 2; contact: Level 3; and metal: Level 4.

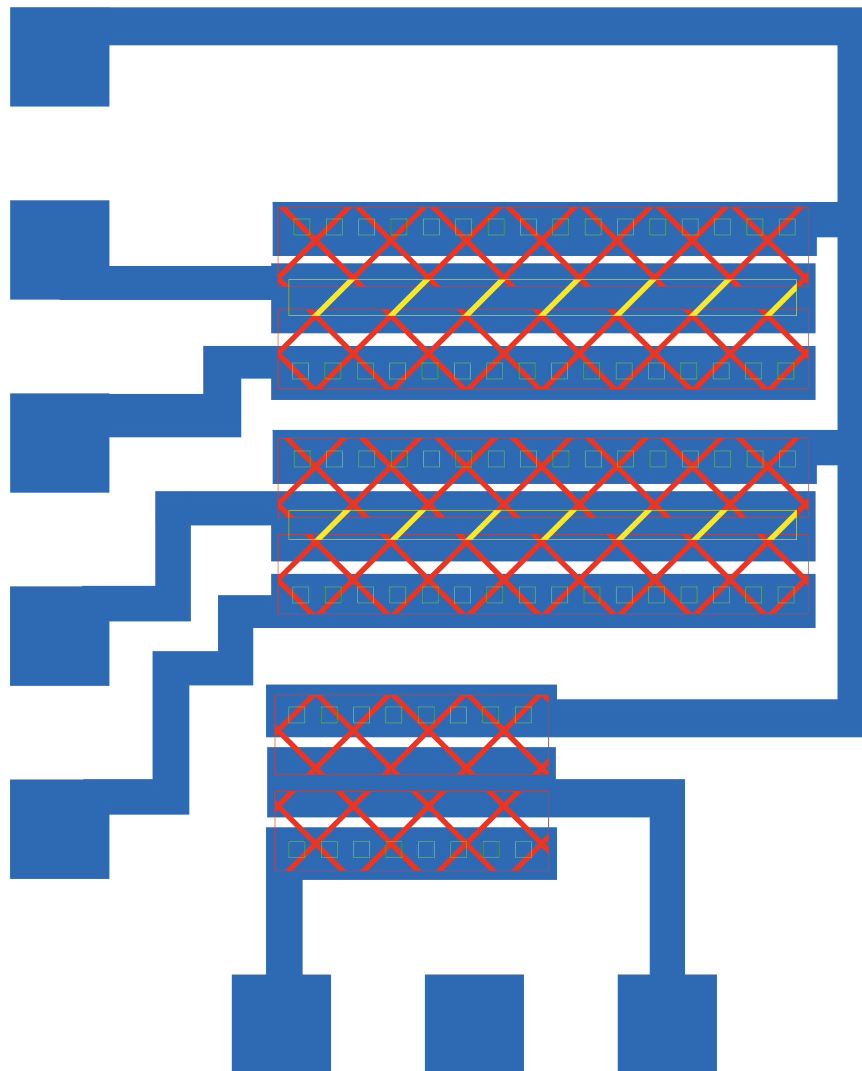


Figure 12: **Composite view of MOSFET patterns of Holberg Mask Set; all four levels are shown superimposed.**

Trouble Shooting During Device Testing

filename: TROUBLE

The device testing done in our lab is one of the most difficult parts of the class. This is because many of you are not accustomed to making measurements of truly unknown quantities. As discussed in the lab report section, we never really know what to expect from our fabrication process. Because the range of electrical characteristics that can result from nonideal fabrication is bewildering, you may feel overwhelmed by the data you collect during the test phase.

STEP ONE: DON'T PANIC!!!!

STEP TWO: **NEVER TAKE DATA BEFORE YOU UNDERSTAND EXACTLY WHAT YOU ARE MEASURING!!**

There are a number of very simple things you need to verify before making a measurement:

Do you have the wires connected correctly between probes and test instrument? to the **substrate chuck**? to the device itself?

These questions are not as simple as they may seem, and require that you really understand how to hook up a device. For an I-V measurement, one way to test the connections between probers and the test instrument is to try to form a "short circuit" at the probe tips (touch them together!). Since you know what the I-V curve of a short looks like (I hope), you can check your connections. Now try an open circuit. These are simple tests, but **very important**.

Once you have verified that you really have the right connections, what do you do if the device doesn't work? Obviously, I would ask: "**How** doesn't it work?" Is it a short? An open? A resistor when you expected a diode? A diode when you expected a resistor? This could go on forever, but you should be asking yourself these kind of questions. You really have to think about how devices work, but don't get too lost in elaborate semiconductor physics.

Another important thing to realize is **the order of your testing is important!** For instance, C-V measurements rarely make sense for devices that pass a large amount of dc current.

- For MOS capacitors this means an I-V measurement should be done to insure the caps are not leaky before any C-V measurements are attempted.
- For diodes, this means an I-V measurement must be performed to insure C-V is done only over a voltage range where the reverse bias leakage current is small.

Note you cannot even make I-V measurements unless you know you have good ohmic contacts to the silicon. A good way to check this would be an I-V measurement between the backside and front-side "substrate" contacts to the chip. What does it mean if this gives a diode-like curve? A resistor-like curve? What **should** it be?

If a device doesn't work the way you "expected," you need a strategy to determine why it didn't work. For a MOSFET, the most useful approach is to look at the various components that make up a MOSFET. For instance, the source-substrate and drain-substrate form p-n junction diodes. A good check would be to measure the I-V curve of these diode "sub-components." What would happen to the MOSFET I-V curves if these junctions are leaky? What would happen to the curves if your source/drain contacts to the silicon exhibit very high resistance? Even if everything is fine with the device, you may still have hooked it up wrong; for instance, what would the I-V curve look like if you select the "wrong" polarity (with respect to the substrate) for the drain bias?

I recommend the following procedures:

- **Before doing any C-V measurements, do I-V testing on the devices to ensure that leakage currents are small.**

- **Don't collect large amounts of "strange" looking data, expecting you will be able to figure it out later.** Think about it while you are measuring, and try different tests to check for obvious errors (mis-connections, leaky diodes, bad contacts, etc.).

- **Do C-V on MOS capacitors before doing I-V on your MOSFETs.** This will allow you to determine what gate biases are needed to operate the MOSFETs.

- Think about the relationships between data seen in one type of device to other devices. How does diode I-V data help you understand MOSFETs? How does MOS cap C-V data help you understand the MOSFETs? What does resistor behavior tell you about diodes, and vice versa?

- **THINK!!!**

How to find a "GOOD" MOSFET:

The following procedure could be used to ensure that you find a "good" MOSFET (or alternatively, find out what part of your MOSFET does **not** work). This sequence is designed to identify the sub-components of a MOSFET, as shown below. To measure a working MOSFET **all** the sub-components must work **properly**.

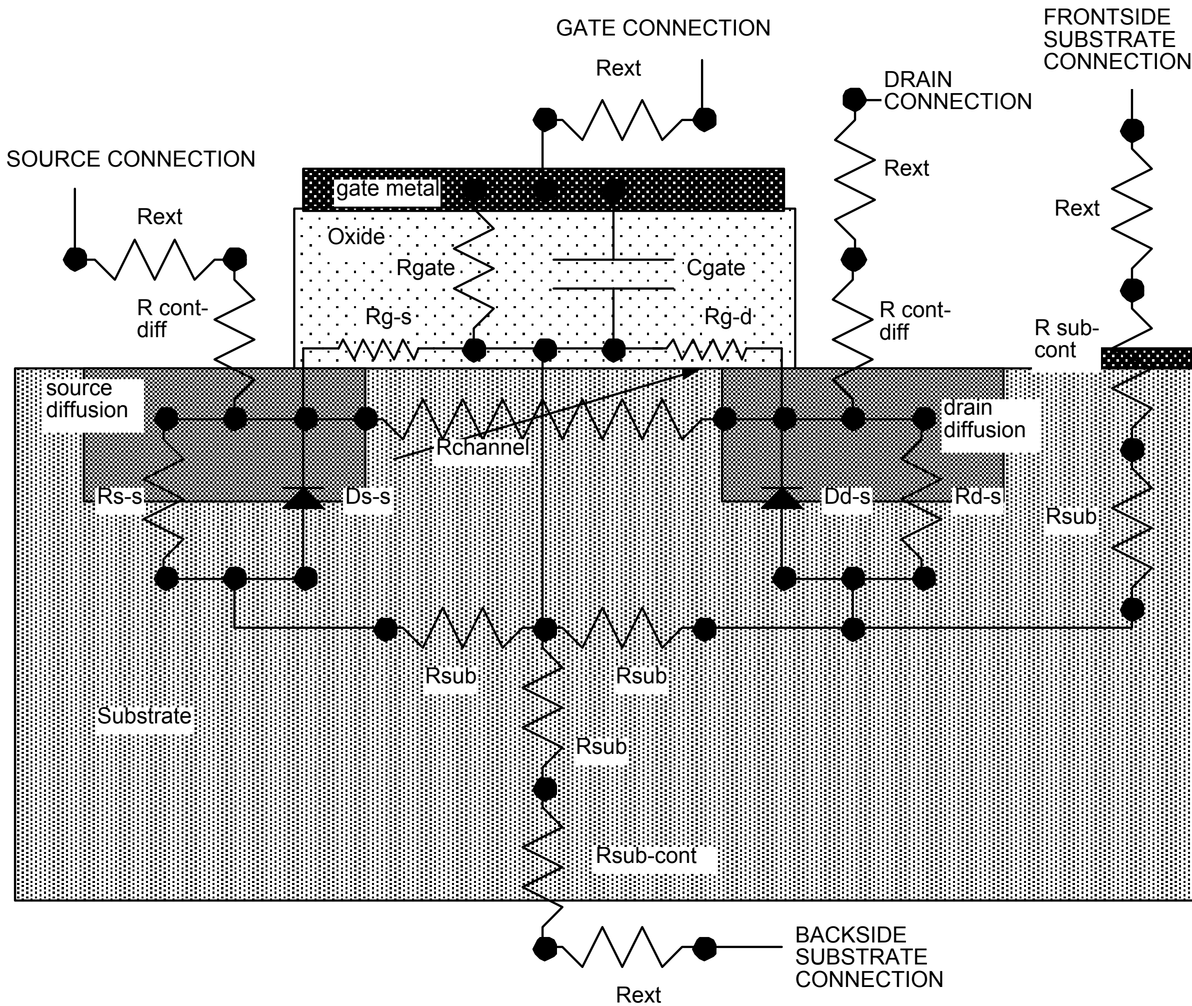


Figure 13: MOSFET sub-components

The sub-components are defined as follows:

8. R_{ext}: external parasitic resistances due to probe cables and connectors
9. $R_{sub\text{-}cont}$ (frontside and backside): contact resistance between Al metallization and the undiffused (substrate) areas of chip
10. R_{gate}: resistance of gate oxide "insulator" to substrate under gate
11. C_{gate}: capacitance of gate oxide
12. $R_{g\text{-}s}$ and $R_{g\text{-}d}$: resistance of gate oxide "insulator" to source and drain diffused regions (respectively) under gate
13. $R_{channel}$: gate voltage-controlled effective resistance of the channel region
14. $R_{cont\text{-}diff}$: contact resistance between Al metallization and the diffused areas of chip
15. $D_{s\text{-}s}$ and $D_{d\text{-}s}$: diodes formed by source-substrate and drain-substrate p-n junctions
16. $R_{s\text{-}s}$ and $R_{d\text{-}s}$: reverse-bias leakage "resistance" of source-substrate and drain-substrate p-n junctions
17. R_{sub}: substrate resistance

Most of us would recognize the essential feature of a MOSFET as the channel, whose equivalent resistance $R_{channel}$ (i.e., the relation between the source-drain current and the source-drain voltage) is controlled by the voltage applied between the gate and the substrate. These characteristics are represented by the conventional family of I_{ds}-V_{ds} vs V_g curves for the device. However, for our "home-made" MOSFETs, the characteristics of all the other sub-components must also be verified. The various structures fabricated with the Holberg mask set should allow you to check each part of the device in turn.

If you understand how a MOSFET works, then you should know what an approximately "proper" value is for each. Here is a check list; indicate with a check mark what value you should get for each sub-component:

Table 8: Trouble shooting checklist

Sub Components	Resistance Value			
	Open	high	low	short
R_{ext}				
$R_{sub-cont}$				
R_{gate}				
R_{g-s}				
R_{g-d}				
$R_{cont-diff}$				
R_{s-s}				
R_{d-s}				
R_{sub}				

For the diode sub-components (assuming the substrate is the grounded reference), we should also determine which polarity is forward bias, and which is reverse. In the following table, indicate whether a positive (+) or negative (-) voltage should be applied to the diffusion contact to achieve the indicated bias condition. Also indicate whether the junction should exhibit a high or low resistance under the given bias condition.

Table 9: Diode checklist

sample	forward bias		reverse bias	
	polarity	resistance	polarity	resistance
p-type substrate, n-type diffusion				
n-type substrate, p-type diffusion				

Now that you have filled in the tables, you know what to look for as you take data. As I said earlier, it is extremely important to examine your data as you take it to see if it is reasonable. The rest of our procedure will be designed to measure each sub-component, ideally one at a time. Some components are almost always connected together, so we may need to be creative in trying to isolate their individual contributions to the measurements.

It is also critical to determine whether a measurement made on one device can be assumed to hold for another, i.e. we need to check for uniformity. For instance, if you find that one p-n diffused diode is "OK," can you assume all the MOSFET source-substrate and drain-substrate p-n junctions are also OK? You need a quick strategy to check for "qualitative uniformity." For this example, one way is to check several p-n diodes; they must ALL have I-V curves which are qualitatively similar. If even one is "bad," since your sample was probably small, the chance of another p-n junction being bad is HIGH! In such a case you will have to individually qualify a single MOSFET, and make **all your measurements on that SAME device**.

MOSFET QUALIFICATION PROCEDURE:

STEP 1: Check R_{ext}: Obviously, you have to make sure the hook-up between measurement instrument and device. You should do this both visually and electrically (for instance, by either shorting or opening appropriate connections).

STEP 2: Check $R_{sub\text{-}cont}$: We must have an **ohmic** contact to the substrate to make any further measurements. One way is to try to measure an I-V curve between the frontside and backside substrate contacts. It should be linear through the origin, NOT a Schottky-like curve.

STEP 3: Check $R_{cont\text{-}diff}$: This is actually very hard to do quantitatively. We have one device on the chip (in the lower center area of the die shown on p. 44) called a Kelvin structure which is specifically designed for contact resistance measurement. At present we are not using this device, but instead use the diffused resistors to estimate $R_{cont\text{-}diff}$. The I-V measurements discussed on p. 64, along with the analysis on p. 69 should be used estimate $R_{cont\text{-}diff}$. You should also do a quick check now to see if the diffusion sheet resistance extracted from the resistors compares well with your four-point probe measurements made on the MPTs.

STEP 4: Evaluate p-n junctions: This should help establish the characteristics of $D_{s\text{-}s}$ and $D_{d\text{-}s}$ (and thereby $R_{s\text{-}s}$ and $R_{d\text{-}s}$). Start with I-V measurements on the diffused diodes, p. 64. In addition, set up to measure I-V between the source of your target MOSFET and the substrate; it should look similar to your diode curves. Same thing for the drain-to-substrate I-V. **These measurements can be made with the curve tracer.**

STEP 5: Check R_{gate}, $R_{g\text{-}s}$, and $R_{g\text{-}d}$: Here we want to determine if gate oxide leakage is a problem. Start with I-V measurements of your MOS Caps, p. 65, done using PicoPete. Also check your target MOSFET, measuring I-V between the gate and substrate, gate and source, and gate and drain.

Assuming all the measurements made above are sensible, we are now ready to progress to C-V measurements

STEP 6: Check C_{gate}: Start by measuring the C-V characteristics of a MOS Cap which I-V has shown to have low leakage. See p. 67. Make sure you look at more than one, and determine the gate voltage range over which the MOS Cap goes from accumulation to depletion. This should establish the polarity of the threshold voltage V_t, and the range over which V_g should be swept when you go back to I-V measurements of the MOSFET.

STEP 7: You are now ready (finally) to measure the family of I_{ds}-V_{ds} versus V_g curves which characterizes your MOSFET. See p. 65. Please make sure to save at least one set of curves for your lab reports. Also make sure to make the transconductance measurement.

Device Testing: FOR REFERENCE ONLY!!!!!!!!!!!!!! DO NOT DO ALL THE TESTING DECRIBED BELOW!!!!!!!!!!!!!!!!!!!

Required Pre Lab Reading: Trouble Shooting, p. 56; OP-Q, Tektronix Curve Tracer; OP-M, Capacitance-Voltage Measurements

Because of limited test equipment each group must schedule their testing time independently. There are a large number of measurements to make, and a great deal of data to analyze. You must work efficiently to get everything done. In addition, make sure you **read the post-lab questions now and begin to think about them**. Where you feel it is necessary you may use any text books or reference works, but you MUST REFERENCE ALL FORMULAS OR EXPLANATIONS YOU FIND IN THESE WORKS.

PLEASE read the section on trouble shooting (p. 56). You can take an enormous amount of data which is utterly meaningless if you are not careful! **Never take data you don't understand, assuming you'll come back someday and think about it.** I guarantee you'll never get around to it, you'll just end up with a very thick pile if garbage. Don't attach this to Lab Report III, expecting I'm going to figure it out for you. Understand your measurements as you do them: spend your time **thinking**, not simply generating numbers! **You MUST complete the procedure for trouble shooting, BEFORE continuing with the complete device testing procedures.**

CAUTION: THE MICROMANIPULATOR PROBE TIPS ARE VERY SHARP, AND VERY FRAGILE. You MUST be extremely careful not to strike the needles against one another or the substrate chuck. It is very easy to bend the tips, making them useless for your measurements. The devices you are probing are fairly small, and only sharp tips will be able to contact them. When you lower the tips to contact your chips be very gentle; you should use the minimum amount of tip pressure necessary to ensure contact. Due to optical injection effects you must make all your measurements in as nearly dark as possible. Make sure you turn the microscope illuminator OFF before making any measurements.

Please use the sign-up sheets posted on the Lab doors to reserve the curve-tracer and C-V system. Sign up in your own lab period slots if possible; do not sign up for more than one period at a time on each system.

Note: We have / are changing software, so the references to the program PCASP below may be obsolete!!

CHECK FOR UPDATES ON REQUIRED MEASUREMENTS BEFORE PROCEEDING!

Part I Current-Voltage Measurements

A) Diffused Resistors

On your n-type and p-type substrates measure:

1. For one "good" R2 resistor measure the I-V curve of the resistor at low voltages using PicoPete. Check at small voltages for linearity as V crosses zero. Make a qualitative sketch of your results. The substrate should be floating for these measurements.

2. For the R1, R2, and R3 resistors measure the total resistance of:
   i) Two resistors near the center of the chip.
   ii) Two resistors near each edge of the chip. Make sure to note the location on the chips of each resistor, along with its resistance.

*** Use the probe station connected to the DMM for these measurements.* This will only work if your ohmic contacts are OK; see step 1 above for linearity near zero bias.**

   This data will be used to determine sheet, contact, and bend resistances, as well as doping uniformity.

3. Connect a current source between the I1 and C terminals, then measure the voltage drop between the V1 terminals, and between the V2 terminals. Check for several currents. This data can be used to check the resistance per square using a four-point type measurement, largely free from contact resistance effects

B) Diffused Diode

[Note: You should remember which diode you probed, and if possible use this same diode for C-V measurements.]

On your n-type and p-type substrates measure:

1. A complete I-V curve for one good diode. You should be able to extract the following parameters: forward resistance, R_F, breakdown voltage, V_{BR}, reverse leakage current, I_L, and turn on voltage, V_O. The breakdown voltage is the voltage required for a leakage current of 10 μA. I_L is measured at $V_{BR}/2$. See diagram on next

page. **Use PicoPete for these measurements.** I suggest outputting your data in table format for future calculations.

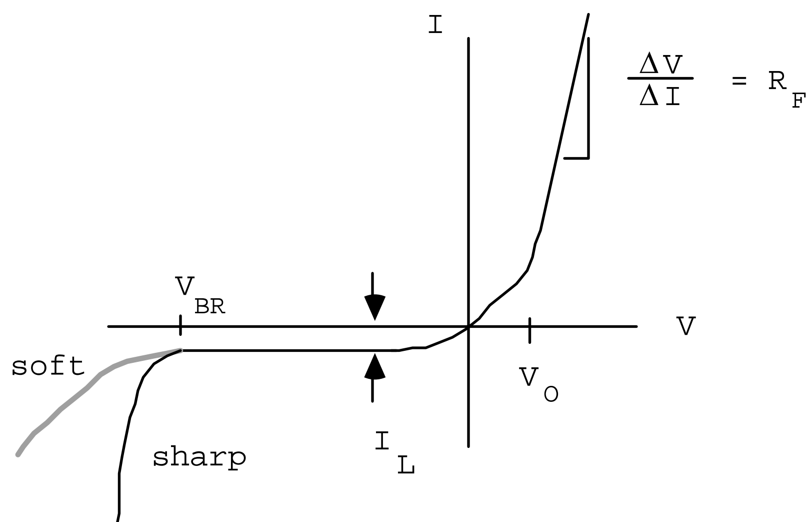


Figure 14: I-V PARAMETERS FOR DIFFUSED DIODE

C) MOS Capacitors

On each of your samples check for leakage currents with a sweep of about $\pm$ 20V applied to the metal electrode. Check several capacitors without guard rings on each chip. Make sure you know which ones are either shorted or leaky, if any. **Use PicoPete for this. Do this quickly; your main objective is to qualitatively determine if your caps are unusually leaky. We do NOT need to see these curves in your lab reports, but we do want a number for leakage current at 10 V bias.**

D) MOSFET (Use PicoPete for this)

See OP-Q for measurement details. The MOSFET layouts are shown on p. 55.

Normal connections to PicoPete are: short source and substrate together, connect to ground; connect drain to V_A (this is the bias line which PicoPete sweeps and simultaneously measures current in); and connect gate to V_B (this is the "BIAS VOLTAGE" line which Pete can step through).

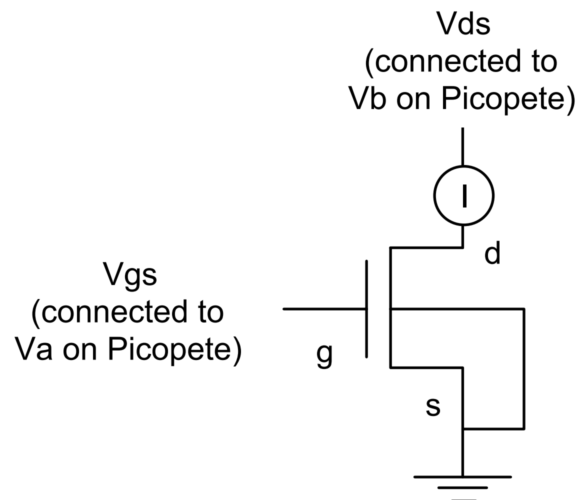
For each substrate:

1. Find the maximum transconductance and threshold voltage at max g_m of at least three MOSFET's on each chip.

First obtain the family of curves describing the MOSFET operation. Connect PicoPete to your devices as discussed above. Start with a gate voltage range (i.e. "BIAS VOLTAGE" in PCASP General I-V Menu) of about -3 V to 0 V, in 5 steps. **See TAs for updates on parameters to use with PCASP.** We do NOT need to see all of these curves in your Lab Reports; this is to determine qualitatively whether you are probing a good MOSFET. We do want you to save one "representative" set of curves.

Now measure g_m and I_{ds} vs V_{gs}:

Change the connections to the MOSFET as indicated below.



You can do this by simply swapping the BNC connections to V_A and V_B on PicoPete. You can now use the PCASP general I-V measurement to measure the I_{ds} vs V_{gs} curves of your MOSFETs. Selection of the differential output conductance option will directly measure g_m, while the I-V option will give us V_t. See pp. 34 below for parameter extraction techniques.

Suggested starting values:

a) Set Source Voltage range to -5 to +5 V; set number of intervals to ; set Bias Voltage to 0.1 V.
b) Select IV curve Table, output to printer; IV Graph, output to Screen.
c) Select Differential Output Conductance Table, output to printer; Differential Output Conductance Graph, output to screen. Now perform measurement.

For ONE good MOSFET on each chip, output the IV and Differential Output Conductance curves to the plotter for your lab reports. They should look approximately as those posted in the lab.

Note: You can do all this very rapidly by measuring one device, then raising all the probes using the z- axis adjustment ONLY, translating the substrate to bring another device under the probes, and finally lowering the probes into contact with the new device. Summarize the data in a table.

Note: Your p-type substrates may yield MOSFET's that are conducting at $V_{gate} = 0$, and may require the application of a negative gate bias to turn them off. See the TAs for recommendations.

Part II Capacitance - Voltage Measurements

A) Diffused Diode

On your n-type and p-type substrates:

1. Find a good diode by quickly measuring the capacitance- voltage curves for several devices. A good diode should have its maximum capacitance at about V=0, and it should decrease with increasing REVERSE BIAS (see the introductory section to OP-M). If you have already done your I- V measurements, use the diode you used there. Don't save this; this is just to locate a good diode.

   Measure the C-V curve from OV to 10V (reverse bias - you may have to reverse the LO and HI connections to the capacitance meter). Use PCASP to set up this measurement. Use the diode data acquisition and analysis screen, and output only the doping profile.

B. MOS Capacitors

On your n-type and p-type substrates:

1. Look at two capacitors near the edges, and two near the middle of each chip. For each cap perform the following:

   Quickly measure the C-V curve from about -10V to +10V (where our convention is to measuring the polarity of the Al electrode with respect to the substrate) for your capacitors. Use the PCASP MIS Capacitor Analysis menu, and select Output Raw CV Data, graph to screen. Once you have a "good" cap, **output the C-V curve to the plotter**. Use PCASP to perform doping profile and flat band analysis on each capacitor. To get good doping profile results, select a source voltage range to take about 10 data points across the transition region from accumulation to depletion. For

the flatband analysis select C_{max} and C_{min} voltages to be ± 10V (polarity appropriate to p or n type chip). Make sure to note the location on the chips of each capacitor. These results will be used to check the substrate background doping and oxide thickness uniformity of your chips.

2. Repeat for capacitors with guard rings. Be careful about the difference in areas for the caps with guard rings.

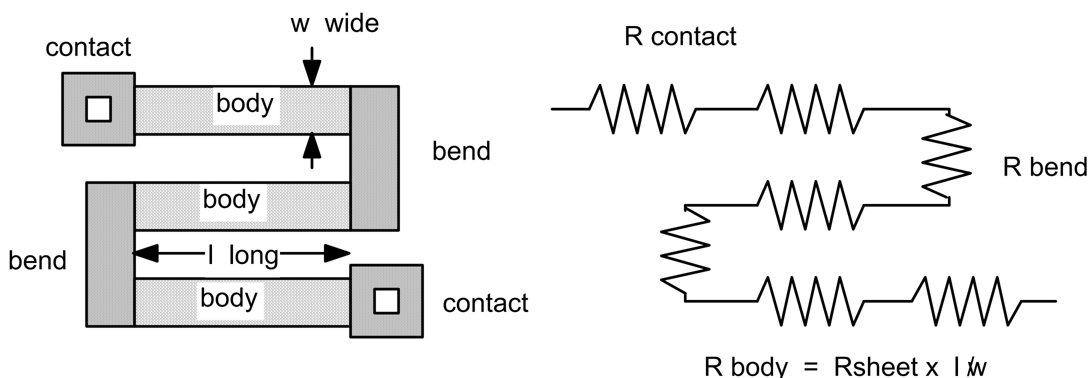
THIS CONCLUDES THE DEVICE MEASUREMENT SECTION

Questions related to device testing:

Remember to be careful about significant figures and error estimates when filling out the Tables!!

A) Diffused Resistor

A simplified schematic of a diffused resistor is shown below. The total resistance is made up of three contributions: the body resistance R_B found from the number of squares and the sheet resistance of the main sections of the resistor; the bend resistance R_{BND} due to current crowding around corners in serpentine resistors; and the contact resistance R_C, due to current injection at the ends of the resistor.



Using the measurements made earlier we can determine the different contributions to the resistance of our devices. For a straight resistor (i.e. R_1 and R_2 on our chips) simple algebra gives both the sheet resistance R_S and the contact resistance R_C:

$$R_S = \frac{R_2 - R_1}{N_2 - N_1}$$

$$R_C = \frac{R_2 - N_2 R_S}{2} \quad \text{or} \quad R_C = \frac{R_1 - N_1 R_S}{2}$$

where

R_1 = measured resistance of resistor 1
R_2 = measured resistance of resistor 2
R_S = sheet resistance due to diffusion
R_C = contact resistance
N_1 = number of squares in body of resistor 1
N_2 = number of squares in body of resistor 2

Compare the R_S from the resistors to the R_S from your MPT chip measurements. Comment on the differences. Also compare your measurement of R_C to the formulas given in Ghandhi (pp. 628-629).

We can find the effective resistance of bends (one complete fold-over) using the data found for contact and sheet resistances:

$$R_{BND} = \frac{R_3 - 2R_C - N_3 R_S}{N_B}$$

where

R_3 = measured resistance of resistor 3
R_S = sheet resistance due to diffusion
R_C = contact resistance
N_3 = number of squares in body of resistor 3
N_B = number of fold-overs in resistor 3
R_{BND} = effective resistance of bend

We can then find the "effective size" of a bend L_{BND} (measured in squares) using

$$L_{BND} = \frac{R_{BND}}{R_S}$$

Compare your measurements to the formulas given in Ghandhi (pp. 628-629). Use this information to complete Table II.

2. Based on your resistor measurements, can you tell if the doping is uniform across the face of the chip? Comments?

B) Diffused Diodes

1. C-V data analysis: [NOTE: we have/are changing programs for the CV section, so PCASP may not be available]

Recall that

$$C = A\varepsilon_{ox}/x_d$$

where A = area of diode (get this from the Holberg Masks) and x_d = depletion layer width.

PCASP uses your C-V data to calculate x_d vs. V. Assuming

$$x_d = BV^n$$

PCASP can find B and n. For an abrupt, one-sided junction we expect the value of n above to be 1/2. Under these conditions the doping at x_d is given by

$$N(x_d) = \frac{-2}{q\,\varepsilon_s \left[\frac{d(1/C^2)}{dV}\right] A^2}$$

PCASP can use this model to calculate the substrate doping, N_B, as a function of depth into the sample. How does this value of N_B compare to the substrate doping measured from your MPT chips? Why can't we obtain (much) information about the diffusion doping profile with these measurements? Use this data to complete Table III.

2. I-V data analysis

A standard way to analyze diode characteristics is to try to fit the I-V curve to the ideal diode equation

$$I = I_o\left[\exp\left(\frac{qV}{nkT}\right) - 1\right]$$

where n is the ideality factor. Plot your I-V data on a semi-log scale, i.e. ln(I) vs V. **Under what conditions (i.e. what voltage bias range) is the slope of a <u>real</u> I-V curve related to the ideality factor?** What ideality factor does your diode give? What is I_o?

C) MOS Capacitors

1. Use the PCASP C-V doping profile results to determine the background doping concentration in your chips. For each cap measured, find the average doping concentration over the measured depletion width. Use this information to complete Table III.

2. From the PCASP C-V flat band analysis measurements, find t_{ox}, and determine how uniform the oxide thickness is across your chips. Compare the calculated oxide thickness here to your MPT oxide measurements. Use this data to complete Table I (note that the index of refraction given by the ellipsometer is $\sqrt{\varepsilon_r}$, measured at the He-Ne laser wavelength, while ε_r given by C-V is measured at 1 MHz). Also use this information to complete Table ??. Please give the excess surface charge Q_{ox} in units of number density, i.e. $\#/cm^2$, NOT IN COULOMBS/cm^2. Comment on possible sources of this excess charge.

D) MOSFET

1. Use the PCASP Differential Output Conductance Tables to find the maximum transconductance g_m^{max} of your MOSFETs. Use this data to complete appropriate entries in Table V. Include one representative plot in your lab report.

A very simple estimate of the transconductance expected from your MOSFETs is given by

$$g_m = \mu \; C_{ox} \frac{W}{L_{eff}} V_{ds}$$

where for an

n-channel device $\mu = \mu_n \bullet 1400 \; cm^2/Vsec$
p-channel device $\mu = \mu_p \bullet 500 \; cm^2/Vsec$

and

$C_{ox} = \varepsilon_r^{oxide} \varepsilon_o / t_{ox}$
W = width of the MOSFET gate
L_{eff} = effective channel length
V_{ds} = drain-source bias used in your measurement.

Using the Holberg masks and the other information (such as the gate oxide thickness t_{ox}) you have, calculate the g_m of your MOSFETs; use this information to fill out Table V. Comments on differences?

2. One way to define the threshold voltage of your MOSFETs is to use the I_{ds} vs V_{gs} measurements described on p. ??. We will use the convention that

$$V_t = 2 \; V_{g1} - V_{g2} - \frac{1}{2} V_{ds}$$

where V_{g1} is the gate voltage necessary to achieve I_{ds} of 100μA, and V_{g2} is that necessary to achieve 200μA. You set V_{ds} when you made your measurements (I suggested 0.1V; if you changed it use the new value). Using the tables of I_{ds} vs V_{gs} you measured, find V_t for each MOSFET measured. Use this information to fill out the appropriate parts of Table V.

III. Operating Procedures

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OP-A: OPERATION OF HIGH TEMPERATURE FURNACES

filename: FURNAC

Our laboratory uses several different kinds of high temperature (T > 400°C) furnaces to perform a variety of processes. These furnaces have many common features, and the purpose of this section is to familiarize you with their operation. The first and most important characteristic is the cleanliness of the furnace quartzware. Semiconductor processing is very sensitive to contamination, especially when the contaminant is exposed to high temperatures. For instance, doping levels of importance in silicon often are as low as $10^{15}/cm^3$; compared to normal atomic densities of 10^{22} atoms/cm^3, this is only one part in ten million. Because of this we use only extremely inert materials like pure quartz (SiO_2) in our furnaces. You must NEVER handle quartzware unless you are wearing clean gloves; finger oil is one of the worst sources of contamination. Also remember that if you touch your face while wearing gloves, the gloves will carry oil to anything you subsequently touch. **PLEASE HANDLE ALL QUARTZWARE CAREFULLY; ALWAYS ASSUME BOATS AND PULL RODS WILL BE VERY HOT. These boats, tubes, and rods were all custom made for our lab; they are both fragile and expensive.**

FURNACE GAS SYSTEMS

All the high temperature processing steps we perform must be carried out in controlled atmospheres. Each furnace has all the necessary gases plumbed to it; for each gas there is a TOGGLE VALVE which turns the flow on or off, and a FLOW METER - NEEDLE VALVE combination which sets the gas flow rate into the furnace tube. Gas flow is reduced when the needle valve is turned clockwise, and increased when turned counterclockwise. Flow rate is measured using a rotameter. This device is simply a tube with a tapered bore, which contains a small ball (see Figure 15). Higher gas flow rates cause the ball to rise higher in the tube. The diameter of the tube at the inlet, the weight of the ball, and the taper of the tube set the range of the rotameter. We use several different meter ranges, and each tube contains both a light ball (the black ball, made of pyrex) and a heavy ball (the silver ball, made of stainless steel), which doubles the effective flow range that can be measured. Table 10 summarizes flow rate settings used in the different furnaces. Most of these rates are chosen to simply prevent backflow from the room atmosphere into the furnace tube.

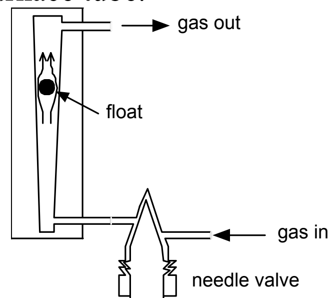


Figure 15: Cross-section of a rotamer type flow meter.

TEMPERATURE CONTROLLERS

All of our furnaces are resistance heated. By using a thermocouple to measure the temperature deviation from some set point, the furnace controller either increases or decreases the current supplied to the furnace. Using this relatively simple operating principle, carefully designed furnaces and controllers can maintain temperatures near 1000°C with an error of only ± 1°C. One important point to remember is that the thermocouple is located at only one place, and there can be appreciable temperature gradients in the rest of the furnace tube. For instance, there is obviously much more heat lost out the ends of the quartz tube than out the middle. If you measure the temperature profile from one end of the tube to the other, only a small region near the center (which is where the thermocouple is located) is fairly constant. This is called the flat zone of the furnace. Furnaces like our boron and phosphorus pre-dep systems have a flat zone of about 8 cm where the temperature varies only ± 1°C.

Our larger furnaces (wet and dry ox, and drive-in) use a more sophisticated design to achieve a longer flat zone, shown schematically in Figure 16. These furnaces are known as 3-zone systems, since there are three independent heating elements. By applying more power to the zones at the ends of the tube, heat loss there can be compensated, and very long flat zones can be obtained. The controllers in these furnaces actually use a pair of thermocouples to measure the temperature difference between the center and the end. We use the center 10-turn pot on the control panel to set the flat zone temperature, and the other 10-turn pots to set the temperature difference. A setting of 500 on these pots would force the end temperature to equal the center; a setting less than 500 gives cooler ends, and greater than 500 gives hotter ends. We actually want the temperature at the ends to be cooler, so we use a controller setting of 100. Even so, these furnaces produce a flat zone (± 1°C) over 20 cm long. Table 11 gives the furnace controller settings used, along with the actual temperature inside the quartz tube, as measured by a thermocouple probe. Note the stand-by settings used when the furnaces are not in use; it is necessary to keep the quartz tubes hot at all times to prevent them from de-vitrifying.

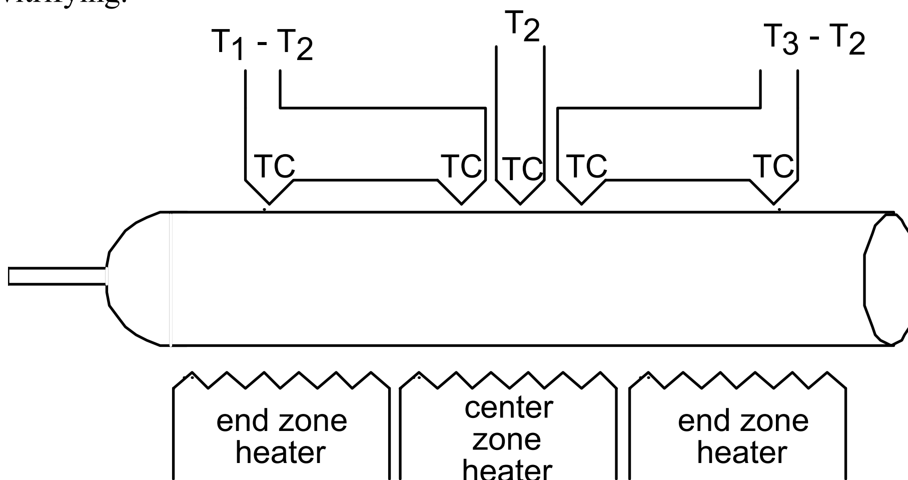


Figure 16: 3-zone resistance heated furnace.

REFERENCES

"Trends in Automated Diffusion Furnace Systems for Large Wafers," J. Maliakel, D. Fisher, Jr., and A. Waugh, "Solid State Technology," December, 1984, pp. 105-109.

Table 10: FURNACE GAS FLOW RATES

FURNACE	TUBE VOLUME (cc)	N_2		O_2		TCE		H_2O	
		cc/min	set pt	cc/min	set pt	cc/min	set pt	cc/min	set pt
Boron pre dep	1600	325	70	0	0	N/A	N/A	N/A	N/A
Phos. pre dep	1600	325	70	0	0	N/A	N/A	N/A	N/A
Drive-in	6700	1000	66 (pyrex)	1000	66 (pyrex)	N/A	N/A	N/A	N/A
Wet ox	6700	0	0	3000	100 (steel)	N/A	N/A	300	150 (steel)
Dry ox	6700	3000	100 (steel)	1000	66 (pyrex)			N/A	N/A

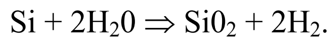
Table 11: FURNACE CONTROLLER SETTINGS

Furnace	Operation		Stand-by	
	Temp. (˚C)	Setting	Temp. (˚C)	Setting
Boron Pre-dep	950	926	650	650
Phos. Pre-dep	650	929	650	650
Drive-in	1100	100/395/100, 900 scale (check for updates)	600	100/100/100, 500 scale
Wet ox	1050	100/260/100, 900 scale (check for updates)	600	100/100/100, 500 scale
Dry ox	1100	100/445/100, 900 scale (check for updates)	600	100/100/100, 500 scale

OP-B WET OXIDATION

filename: WETOX

The growth of $Si0_2$ on Si can be carried out in an atmosphere that is either dry (see) or wet. In the presence of H_20, the oxidation of silicon proceeds via the reaction



$$Si + 2H_20 \Rightarrow Si0_2 + 2H_2.$$

There are two major differences between wet- and dry-grown oxides: 1) oxide growth rate; and 2) dielectric breakdown strength of the oxide. The growth rate in wet ambients is much faster than in dry (the parabolic rate constant for wet oxidation is about 25 times larger than that for dry oxidation at 1050˚C). This is primarily due to a much higher solid solubility of H_20 in $Si0_2$ than 0_2 in $Si0_2$, thus providing a much larger supply of oxidizing species to the Si surface. We supply the H_20 vapor to our furnace using a simple bubbler. A flask containing high purity water is heated to approximately 95˚C to achieve an appreciable vapor pressure of H_20 (approximately 640 Torr), and then a carrier gas (in our system, 0_2) is bubbled through the water. The H_20-saturated gas then passes into the furnace.

The second difference between wet and dry oxides is the lower dielectric breakdown strength of wet-grown oxides. This is largely due to the slightly more porous nature of a wet oxide compared to a dry oxide. Typical values for our wet-grown oxides are in the neighborhood of 8 MV/cm.

REFERENCES

VLSI Fabrication Principles, S. K. Ghandi, Wiley-Interscience, 1983, ch 7.

VLSI Technology, ed. S. M. Sze, McGraw-Hill, 1983, ch 4.

WET OXIDATION PROCEDURE

1. Check H20 bubbler to make sure it is full. Turn heater controller ON; set point should be 94.0˚C.

2. Set furnace temperature controller to 100/260/100 on the 900 scale (check for updates!). This will achieve a temperature of 1050˚C in the flat zone. Allow 30 min. for furnace and bubbler to stabilize.

Steps 1 and 2 should normally be performed by the lab TA before you arrive.

3. Five (5) minutes before loading wafers turn 0_2 gas supply to bubbler ON, set for 150 with steel ball. This is to pre-fill the furnace tube with steam.

4. Remove furnace tube end cap and place it behind the furnace load tray. Carefully remove the pull-rod from its storage tube, and pull the wafer boat out onto the load tray. Replace pull-rod and allow 1 min. for the boat to cool.

NOTE: NEVER USE ANY PULL-ROD OTHER THAN THE ONE SPECIFICALLY FOR THE FURNACE YOU ARE USING!

5. LOAD WAFERS: Place clean Si chips in the wafer boat slots. DO NOT TOUCH THE BOAT WITH YOUR TWEEZERS.

6. Using the pull-rod, perform a slow push of the boat into the furnace flat zone. This should take approximately 1 min. The flat zone is reached when the end of the pull-rod reaches the mark on the furnace tray. Replace pull-rod in its storage tube, and loosely replace furnace end cap.

THE PULL-ROD WILL BE VERY HOT: DO NOT TOUCH ANY PORTION WHICH HAS BEEN INSIDE THE FURNACE.

7. Allow boat to remain in the flat zone for the desired wet-ox time with the bubbler 0_{22} supply on.

8. At the end of the wet-ox time, turn the bubbler 0_2 supply OFF, and turn the DRY 0_2 supply ON, set for 100 with the steel ball. Continue this DRY oxidation for 10 min.

9. At the end of the 10 min dry-ox remove the furnace end cap and pull the wafer boat out onto the furance tray. ALLOW BOAT TO COOL FOR 2 MIN. Remove samples.

10. Store boat in furnace neck, replace cap and pull-rod, turn OFF ALL GAS SUPPLIES.

Stand-by (end of lab shut-down)

-Boat should be in the furnace neck.

-All gas supplies OFF.

-BUBBLER HEATER MUST BE OFF.

-Furnace controller: 100/100/100 on the 500 scale.

Color Chart for SiO_2 (from Ghandhi, p 413)

Intensity enhancement occurs at the wavelength $\lambda_k = \frac{2nd}{k}$, where k = 1, 2, 3,..., d = film thickness, and n = index of refraction of film (1.46 for SiO_2). Also note cyclical reappearance of the colors as the thickness increases. The repeat wavelengths λ_k are related by $\lambda_k = \frac{4nd}{2k+1}$ with k, n, and d defined as above.

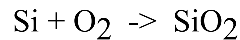
Table 12: Color Chart for Thermally Grown $S10_2$ Films Observed perpendicularly Under Daylight Fluorescent Lighting (adapted from Ghandhi)

Thickness (µm)	Color and Comments
0.05	Tan
0.07	Brown
0.10	Dark violet to red violet
0.12	Royal blue
0.15	Light blue to metallic blue
0.17	Metallic to very light yellow green
0.20	Light gold or yellow-slightly metallic
0.22	Gold with slight yellow orange
0.25	Orange to melon
0.27	Red violet
0.30	Blue to violet blue
0.31	Blue
0.32	Blue to blue green
0.34	Light green
0.35	Green to yellow green
0.36	Yellow green
0.37	Green yellow
0.39	Yellow
0.41	Light orange
0.42	Camation pink
0.44	Violet red
0.46	Red violet
0.47	Violet
0.48	Blue violet
0.49	Blue
0.50	Blue green
0.52	Green (broad)
0.54	Yellow green
0.56	Green yellow
0.57	Yellow to "yellowish" (not yellow; light creamy gray or metallic)
0.58	Light orange or yellow to pink borderline
0.60	Carnation pink
0.63	Violet red
0.68	"Bluish" (Not blue; borderline between violet and blue green; looks grayish)
0.72	Blue green to green (quite broad)
0.77	"Yellowish"
0.80	Orange (rather broad for orange)
0.82	Salmon
0.85	Dull, light red violet
0.86	Violet
0.87	Blue violet
0.89	Blue
0.92	Blue green
0.95	Dull yellow green
0.97	Yellow to "yellowish"
0.99	Orange
1.00	Carnation pink
1.02	Violet red
1.05	Red violet
1.06	Violet
1.07	Blue violet
1.10	Green
1.11	Yellow green
1.12	Green
1.18	Violet
1.19	Red violet
1.21	Violet red.
1.24	Carnation pink to Salmon
1.25	Orange
1.28	"Yellowish"
1.32	Sky blue to green blue
1.40	Orange.
1.45	Violet
l.46	Blue violet
1.50	Blue

OP-C: Dry Oxidation and Chlorine Oxidation of Silicon

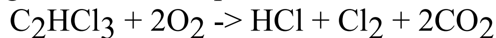
filename: DRYOX

In order to make MOS devices we must grow a very clean, high quality oxide on our silicon. Such devices depend for their operation on the physics of the interface between the silicon and the SiO_2, and the growth of this interface must be very carefully performed. The oxidation of silicon in dry O_2 is straight forward, proceeding via the reaction

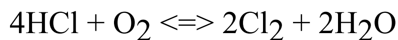


$$Si + O_2 \rightarrow SiO_2$$

We can grow our oxides in such an environment, but for gate oxidations we introduce a small amount of gaseous trichloroethylene (TCE). In the high temperature furnace the following reactions take place



$$C_2HCl_3 + 2O_2 \rightarrow HCl + Cl_2 + 2CO_2$$



$$4HCl + O_2 \Leftrightarrow 2Cl_2 + 2H_2O$$

The presence of all these species affects the oxidation process; for this particular process the equilibrium concentrations are such that CO_2, Cl_2, and HCl are the dominant species present. We can observe one change in the oxide growth quite easily: both the linear and parabolic rate constants increase when TCE is added to the gas stream.

We introduce chlorine during our gate oxidations because it has been found to greatly improve the quality of the grown SiO_2. Such oxides have a greater dielectric breakdown strength. The incorporation of chlorine into the oxide also tends to immobilize sodium, normally a highly mobile ionized species that can cause very unstable threshold shifts in MOSFETs. In addition to improving oxide properties, the chlorine improves the quality of the underlying silicon as well. The chlorine interacts with and removes deep lying impurities in the silicon; this can cause a significant increase in minority carrier lifetimes. Another very important effect is the reduction in oxidation induced stacking faults (OSF's) during halogenic oxidation. When chlorine is present, it is believed to cause an increase in silicon vacancy concentration near the silicon surface. Since OSFs are the result of excess interstitial silicon, an excess of vacancies can combine with the interstitials, thus reducing the number of OSFs.

References:

"Role of Chlorine in Silicon Oxidation," J. Monkowski, Solid State Technology, Part I, July 1979; Part II, August 1979.

"Some Effects of `Trichloroethylene Oxidation' on the Characteristics of MOS Devices," G.J. Declerck et al., J. Electrochem Soc. 122, 1975, 436-439.

"Trichloroethylene Oxidation of Silicon," J.R. Flynn, M.S. Thesis, University of Illinois of Urbana-Champaign, 1980.

Operating Procedure

1. Check TCE bubbler and make sure it is full. The thermometer attached to the bubbler should read between 23°C and 25°C.

2. Set furnace temperature controller to 100/445/100 on the 900 scale. This will give a temperature of 1100°C in the furnace flat zone. Allow 30 min. for furnace and bubbler to stabilize.

Steps 1 and 2 should normally be performed by the lab TA before you arrive.

3. Starting with all gases off, turn the O_2 supply ON, flow meter set at 150 with the steel ball. Allow the furnace tube to flush with O_2 for two (2) minutes.

4. Remove furnace tube end cap and place it behind the furnace load tray. _Carefully_ remove the pull-rod from its storage tube, and pull the wafer boat out onto the load tray. Replace pull-rod and allow 1 min. for the boat to cool.

NOTE: NEVER USE ANY PULL-ROD OTHER THAN THE ONE SPECIFICALLY FOR THE FURNACE YOU ARE USING!

5. LOAD WAFERS: Place _clean_ Si chips in the wafer boat slots. DO NOT TOUCH THE BOAT WITH YOUR TWEEZERS.

6. Using the pull-rod, perform a slow push of the boat into the furnace flat zone. This should take approximately 1 min. The flat zone is reached when the end of the pull-rod reaches the mark on the furnace tray. Replace pull-rod in its storage tube, and _loosely_ replace furnace end cap.

THE PULL-ROD WILL BE _VERY_ _HOT_: DO NOT TOUCH ANY PORTION WHICH HAS BEEN INSIDE THE FURNACE.

7. Start the oxidation timing. Reduce O_2 flow to 66 with the glass ball.

OPTIONAL 7a.: FOR CHLORINE INJECTION ONLY
After oxidation in pure O_2 has proceeded for five minutes, turn the TCE bubbler gas supply (marked CHLORINE on the gas panel) ON, set to 116 with the glass ball.

8. After the desired oxidation time has elapsed, turn the CHLORINE gas OFF (if used), wait 30 seconds, and then turn the O_2 supply OFF. Immediately turn the N_2

supply ON, set to 100 with the steel ball. Allow samples to soak in N_2 for 5 minutes.

9. At the end of the 5 minute N_2 soak, remove the furnace end cap and perform a slow pull of the boat from the furnace: this should take approximately one minute. Allow samples to cool for one minute, then remove them.

10. Store boat in furnace neck, replace cap and pull-rod, turn OFF N_2 supply, and turn O_2 supply back ON, but set for about 5 with the glass float.

Standby:

-Boat should be in the furnace neck.

-TCE (CHLORINE) gas supply OFF, N_2 OFF, O_2 ON, set for 5.

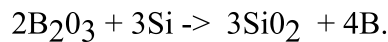
-TCE Bubbler glass stopcocks CLOSED

-Furnace controller: 100/100/100 on the 500 scale.

OP-D: Boron Predeposition

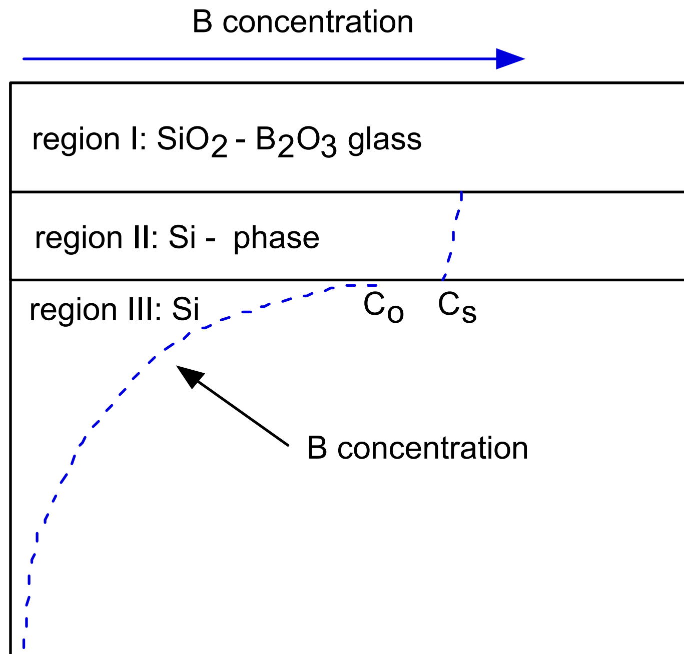
filename: BPREDP

Boron is the most commonly used p-type dopant for silicon, principally because it is the only column III element that can be masked by $Si0_2$. It is introduced into the silicon substrate using a two step, high temperature process. The first step, called the pre-deposition, is an open tube diffusion process that involves the gaseous tranfer of a compound containing the dopant to the Si wafer. The gas may be supplied in several different ways, but in almost all cases the final chemical reaction is



$$2B_20_3 + 3Si \rightarrow 3Si0_2 + 4B.$$

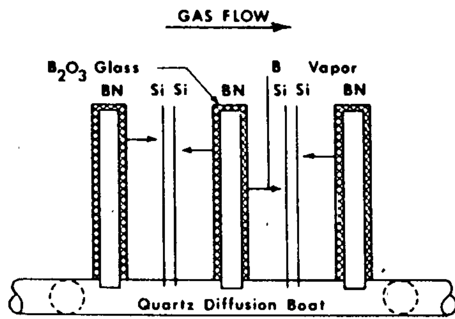
The resulting Si surface at the end of the pre-dep process is sketched in Figure 17. This first stage of doping is referred to as constant concentration diffusion.



Region I: layer of SiO_2 - B_2O_3 glass formed during pre-dep.
Region II: boron rich skin of SiB_x, can be up to 10 nm thick.
Region III: Si substrate with diffused boron. The concentration C_s is a function of temperature, while $C_o = k_s C_s$, where ks is the distribution coefficient between the boron rich region and the silicon.

Figure 17: Boron concentration after pre-dep.

Our boron pre-dep system produces $B_2 0_3$ by an evaporation process from "solid source" wafers. In this method, Si wafers are stacked next to oxidized boron nitride wafers, as shown below. At the pre-dep temperature (in our case, 950°C) a concentration gradient induced diffusion is established between the source wafers and the silicon wafers. This concentration gradient is a function of the distance between the source and silicon, the temperature of the pre- dep, and the composition of the gas ambient (oxidizing or non-oxidizing, presence of $H_2 0$, etc.). Ideally, however, it is not a function of gas flow rate, which is low enough so that the gas between source and wafer is essentially stagnant. The concentration gradient results in the transfer of $B_2 0_3$ to the silicon surface, and so produces a very thin, very highly doped region at the silicon wafer surface. The final level of doping and resulting sheet resistance is determined by time (see Figure 18) and the size of the concentration gradient. Note, however, that the pre-dep temperature is so low that very little boron diffusion into the silicon actually takes place.



The second stage of the diffusion process, called the drive-in, has as its objective the redistribution of the dopant deeper into the silicon, and is referred to as a constant source diffusion. For this process we first remove our silicon wafer from the pre-dep furnace and strip off the $Si0_2$-$B_2 0_3$ glass using HF. The HF actually attacks the $Si0_2$, not the $B_2 0_3$, so care must be used in the pre-dep step to prevent the deposition of excessive amounts of $B_2 0_3$. This is done mainly by assuring no $H_2 0$ is present in the furnace, which would greatly increase the rate of transfer of $B_2 0_3$ to the silicon. Also note the thin Si B_x phase on the wafer is hydrophilic, so the wafer will not de-wet after etching. The actual drive-in is performed at very high temperatures (1100°C in our lab). The drive-in is usually initiated in an oxidizing environment; the initial growth of $Si0_2$ prevents the out-diffusion of the boron during the rest of the process. For operation of the Drive-In Furnace, see 93.

REFERENCES

"System Characterization of Planar Source Diffusion," J. Monkowski and J. Stach, "Solid State Technology," November, 1976, pp 38-43.
"An Improved Boron Nitride Glass Tranfer Process," N. Ditrick and M. Bae, "Solid State Technology," July, 1980.
"Oxidized Boron Nitride Wafers as an In-Situ Boron Dopant for Silicon Diffusion," D. Rupprecht and J. Stach, Journ. Electro. Chem. Soc., Vol. 120, Sept. 1973.
"A Novel Boron Spin-On Dopant," B. Justice, G. Wooster, R. Aycock, and D. Saunders, "Solid State Technology," October, 1984, pp 153-15.
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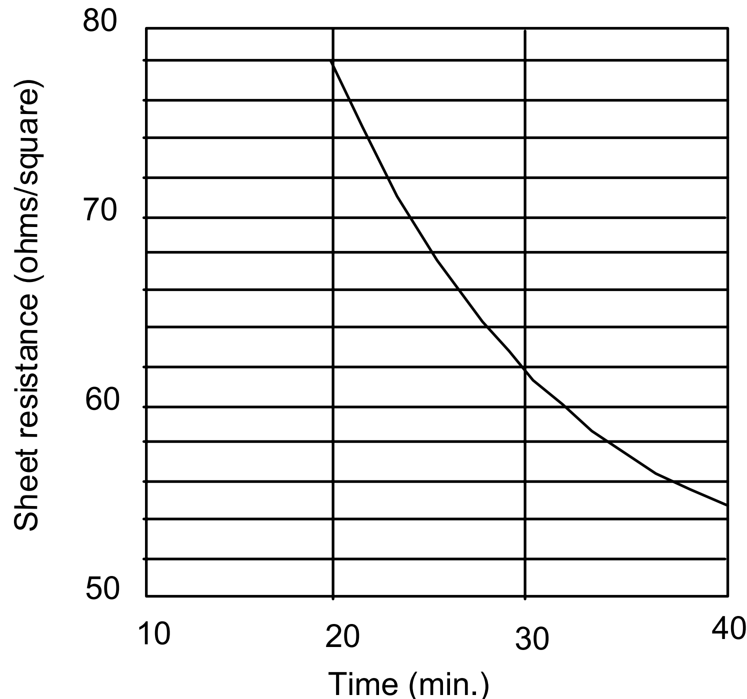


Figure 18: Sheet resistance vs. Boron pre-dep time.

BORON PRE-DEP PROCEDURE

1. Set gas flow rate: N_2 @ 70, steel ball.
2. Set furnace temperature controller: 926. Allow at least 30 min. for temperature to stabilize. This should normally be done by the lab TA before lab starts.
3. Remove furace cap and place it in the beaker on the table. Carefully remove the pull-rod and pull the wafer boat from the neck of the furnace. ALLOW ~ 1 min. TO COOL.

NOTE: NEVER USE ANY PULL-ROD OTHER THAN THE ONE SPECIFICALLY FOR THE FURNACE YOU ARE USING!

4. LOAD WAFERS: Place CLEAN Si wafers in slots immediately adjacent to the BN wafers (polished side next to BN). Note the location of your wafer in the boat in your lab notebook.

DO NOT TOUCH THE BN WAFERS OR QUARTZ BOAT WITH TWEEZERS!

5. Using the pull-rod, push the boat into the neck of the furnace. Allow to equilibrate for 1 min.
6. Slowly push boat into center zone of furnace: 1 min. push. The center zone is reached when the end of the pull-rod reaches the mark on the furnace tray. Replace pull-rod in its storage tube, and replace furnace end cap.

THE PULL ROD WILL BE VERY HOT: DO NOT TOUCH ANY PORTION WHICH WAS INSIDE THE FURNACE.

7. Allow to remain in flat zone for desired pre-dep time.
8. At the end of the pre-dep time, perform a SLOW PULL (1 min.) of the boat from the flat zone to the NECK of the furnace. Allow boat to cool in the neck of the furnace for 1 min.
9. Pull boat out of neck, and allow to cool for 1 min. Remove samples.
10. Store boat in neck of furnace, replace cap and pull-rod.

Stand-By:
-Boat should be in the neck of the furnace.
-N_2 flow-rate: 10, glass ball.
-Controller setting: 650.

Appendix: **Boron Nitride Activation**

The source of boron for our pre-dep system is actually a thin layer of B_2O_3 glass on the surface of the boron nitride (BN) wafers. This glass layer must be periodically grown on the BN, using the following activation procedure.

BN Activation Procedure

1) Wafers should be precleaned, finishing with a HF etch for 1 min., followed by at least 1 hour drying in the furnace neck.

2) Set furnace for 950°C (926 on controller). Allow 30 min. to stabilize.

3) Turn O_2 on, set flow at 100 with steel ball. Allow 10 min. to equilibrate.

4) Oxidize boron nitride: push boat into the flat zone, hold there in O_2 for <u>30 min</u>.

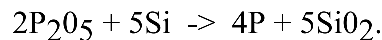
5) Stabilize: turn O_2 off, turn N_2 on at 100 (steel ball) setting, hold for <u>30 min</u>.

6) Pull wafers to neck, turn N_2 down to 10 (glass ball), and set furnace temperature controller back to 650.

OP-E: Phosphorus Pre-Deposition

filename: PPREDP

Unlike the p-type dopants, there are several n-type dopants (column V elements) suitable for use in silicon device fabrication. The three most commonly used n-type dopants are phosphorus, antimony, and arsenic. Of these, phosphorus diffuses at about the same rate as boron, and ten times faster than arsenic and antimony. For these reasons, we use phosphorus as our n-type dopant. As with boron, there are many ways to supply the phosphorus during pre-dep, but the final chemical reaction is



$$2P_20_5 + 5Si \;\text{->}\; 4P + 5Si0_2.$$

The solid source wafers we use are more complex in composition than the simple boron nitride wafers used for boron pre-dep. They consist of silicon pyrophosphate, SiP_20_7, in a porous, inert ceramic binder. These wafers do not require any activation process, but the extremely hydroscopic nature of P_20_5 requires that they be kept very dry at all times. At pre-dep temperatures (950°C) the SiP_20_7 decomposes to P_20_5 and $Si0_2$, which provides the concentration gradient induced diffusion of P_20_5 to the silicon. Figure 19 shows the sheet resistance vs. time curve for our phosphorus pre-dep system.

REFERENCES

"A Solid Planar Source for Phosphorus Diffusion," N. Jones, D. M. Metz, J. Stach, and R. E. Tressler, J. Electrochem. Soc., Vol. 123, pp. 1565-1569, 1976.

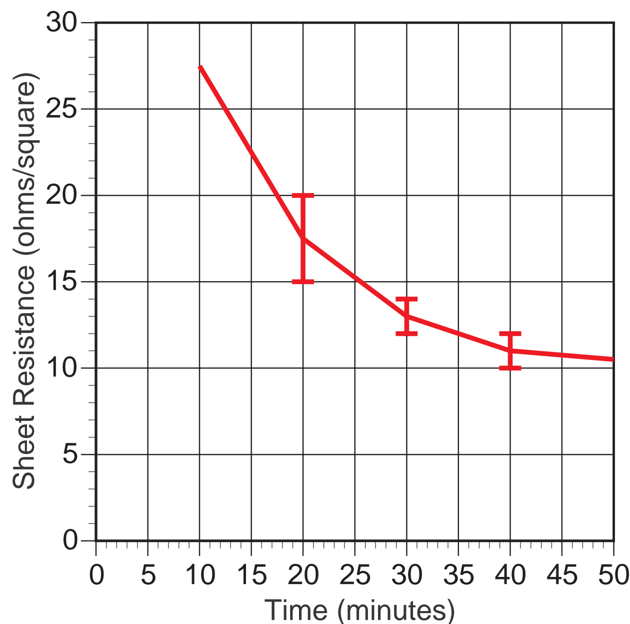


Figure 19: Sheet resistance vs. phosphorus pre-dep time.

PHOSPHORUS PRE-DEP PROCEDURE

1. Set gas flow rate N_2 @ 70, Steel ball.

2. Set furnace temperature controller: 929. Allow at least 30 min. for temperature to stabilize. This should normally be done by the lab TA before lab starts.

3. Remove furnace cap and place it in the beaker on the table. Carefully remove the pull-rod from its storage tube and pull the wafer boat from the neck of the furnace. ALLOW 1 min. TO COOL.

NOTE: NEVER USE ANY PULL-ROD OTHER THAN THE ONE SPECIFICALLY FOR THE FURNACE YOU ARE USING!

4. LOAD WAFERS: Place CLEAN Si wafers in slots immediately adjacent to the P source wafers. Note in your lab notebook the location of your samples in the boat. DO NOT TOUCH THE P WAFERS OR QUARTZ BOAT WITH TWEEZERS!

5. Using the pull-rod, push the boat into the neck of the furnace. Allow to temperature condition for 2 min.

6. Slowly push boat into center zone of furnace: 1 min. push. The center zone is reached when the end of the pull-rod reaches the mark on the furnace tray. Replace pull-rod in its storage tube, and replace furnace end cap.

THE PULL-ROD WILL BE VERY HOT: DO NOT TOUCH ANY PORTION WHICH WAS INSIDE THE FURNACE.

7. Allow boat to remain in flat zone for desired pre-dep time.

8. At the end of the pre-dep time slowly pull the boat from the flat zone to the furnace neck: 1 min. pull. Allow boat to cool in the neck for 2 min.

9. Pull boat out onto furnace rack, allow to cool for 2 min. Remove samples.

10. Store boat in furnace neck, replace cap and pull-rod.

Stand-by:
-Boat should be in the furnace neck.
-N_2 flow-rate: 10, glass ball.
-Controller setting: 650.

OP-F: Drive In Furnace and Diffusion Processing

Filename: DRIVE

One of the most important process steps in silicon device fabrication is the formation of p-n junctions. Several techniques can be employed to form such junctions; the introduction of dopant impurities is usually done with ion implantation or diffusion. In our lab we use diffusion processing since it is considerably simpler than implantation. This process is particularly useful since we can use photolithography and oxide masking to produce intricate patterns of doped areas in the silicon wafers.

We use two different steps in our diffusion process: the predeposition (see OP-D, p. 86, and OP-E, p. 91) and the drive diffusion. Assuming the dopants move in one dimension only (i.e. normal to the wafer surface) the concentration vs. time in the wafer is governed by Fick's Second Law:

$$\frac{\partial N}{\partial t} = \frac{\partial}{\partial x}\left(N \frac{\partial N}{\partial x} \right)$$

where N is the concentration of diffusing atoms, D is the diffusivity, t is time, and x is the distance into the slice. In general, the diffusivity is a function of the concentration of diffusing atoms and of the temperature. However, if we assume that the impurity atom concentration is small relative to the silicon atom density and to the intrinsic carrier concentration at the diffusion temperature, and if we just consider diffusion at a particular temperature, then D can be taken to be a constant, and the preceding equation reduces to

$$\frac{\partial N}{\partial t} = N \frac{\partial^2 N}{\partial x^2}$$

This is often called the one dimensional diffusion equation, and D is termed the diffusion coefficient of the impurity material in the host material. Solutions of this partial differential equation that are applicable to the predep and drive diffusions are obtained by using appropriate initial and boundary conditions. In both cases it is convenient mathematically to assume that the host wafer is infinitely thick, with diffusion taking place from one side only. In practical terms this means that the profile of dopant remains shallow relative to the wafer thickness, typically a few µm relative to 600 µm.

Case I: Predep

In this case we assume there is an infinite supply at constant concentration of dopants at the surface of the silicon wafer (i.e. the BN or P wafers in our predep furnaces). The initial and boundary conditions are then:

$$N(x, 0) = 0 \quad ; \quad N(0, t) = N_o \quad ; \quad N(\infty, t) = 0$$

The solution to the diffusion equation under these conditions is a complementary error function:

$$N(x,t) = N_S \operatorname{erfc}\left(\frac{x}{2\sqrt{D\,t}} \right)$$

$$\text{erfc}(y) = 1 - \frac{2}{\pi}\int_0^y \mathbf{exp}\left(-z^2\right)dz$$

The profile will look roughly like a decaying exponential. In our processing the predep is very short and D is fairly small (because the predep temperature is only 950˚C), so we usually assume the predep profile is roughly a delta function at the surface. This will serve as an initial condition for our drive diffusion.

Case II: Drive-In Diffusion

In this case we assume there is only a limited supply of dopant atoms, initially located at the surface of the wafer, and that the total number of impurities in the sample (called the dose, Q_o) is a constant. The initial and boundary conditions are now

$$N(x, 0) = 0 \quad ; \quad \int_0^\infty N(x,t)dx = Q_0 \, N(0, t) = N_o \quad ; \quad N(\infty, t) = 0$$

The drive diffusion serves to move the impurity atoms into the slice, while lowering the surface concentration. If we assume that all the impurities are initially located at the surface of the wafer (i.e., another initial condition $N(x, 0) = Q_o\ \delta(x)$), then the solution to the diffusion equation is a Gaussian,

$$N(x, t) = \frac{Q_o}{\sqrt{\pi D t}}\ \mathbf{exp}\left(-\left[\frac{x}{2\sqrt{Dt}}\right]^2\right) \quad .$$

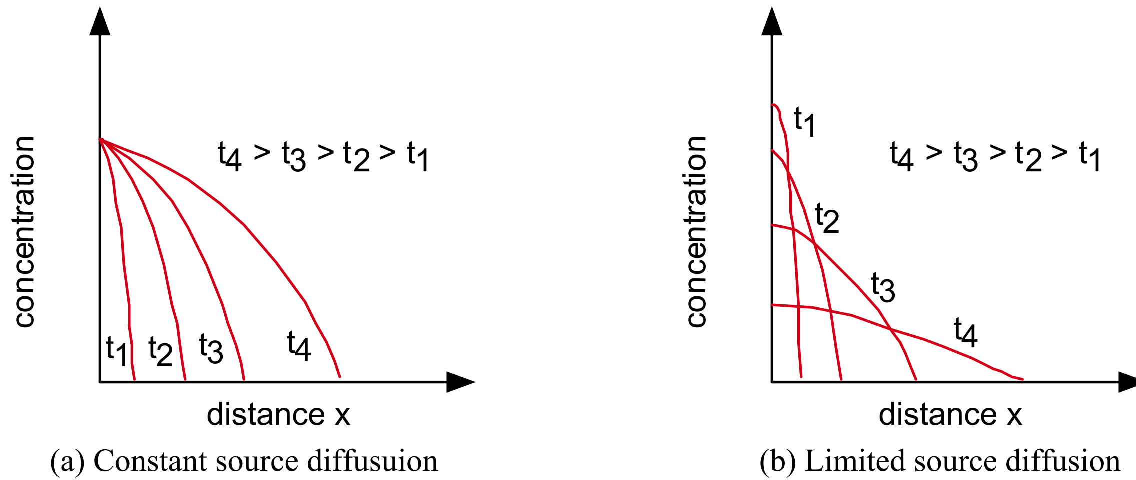
See Figure 20 for comparisons of the erfc and Gaussian curves.

We can see the substantial difference between the predep and drive diffusions by considering Figure 20. Figure 20a shows the constant source predep, and Figure 20b shows the limited source drive. For our furnace conditions, the scale on the x-axis in Figure 20a would be much smaller than on Figure 20b.

It is also possible to relate the sheet resistance, junction depth, impurity type, shape of diffusion profile, impurity surface concentration, and wafer background concentration. These curves are called Irvin curves, and are given on

References

- Ghandhi, Chapter 4.
- Sze, Chapter 5.



(a) Constant source diffusuion (b) Limited source diffusion

Figure 20: Comparison of constant and limited source diffusion profiles.

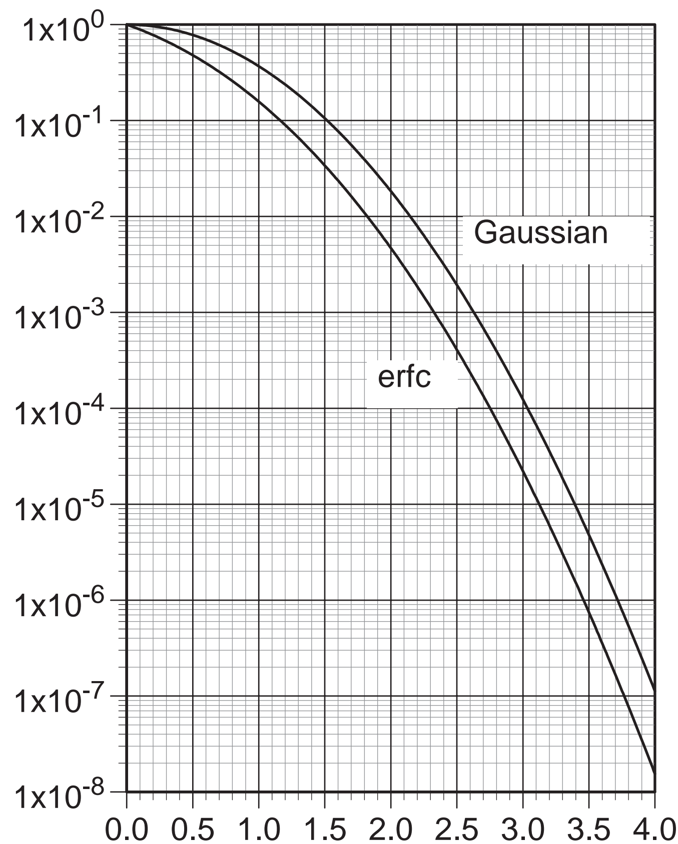


Figure 21: Normalized erfc and gaussian curves.

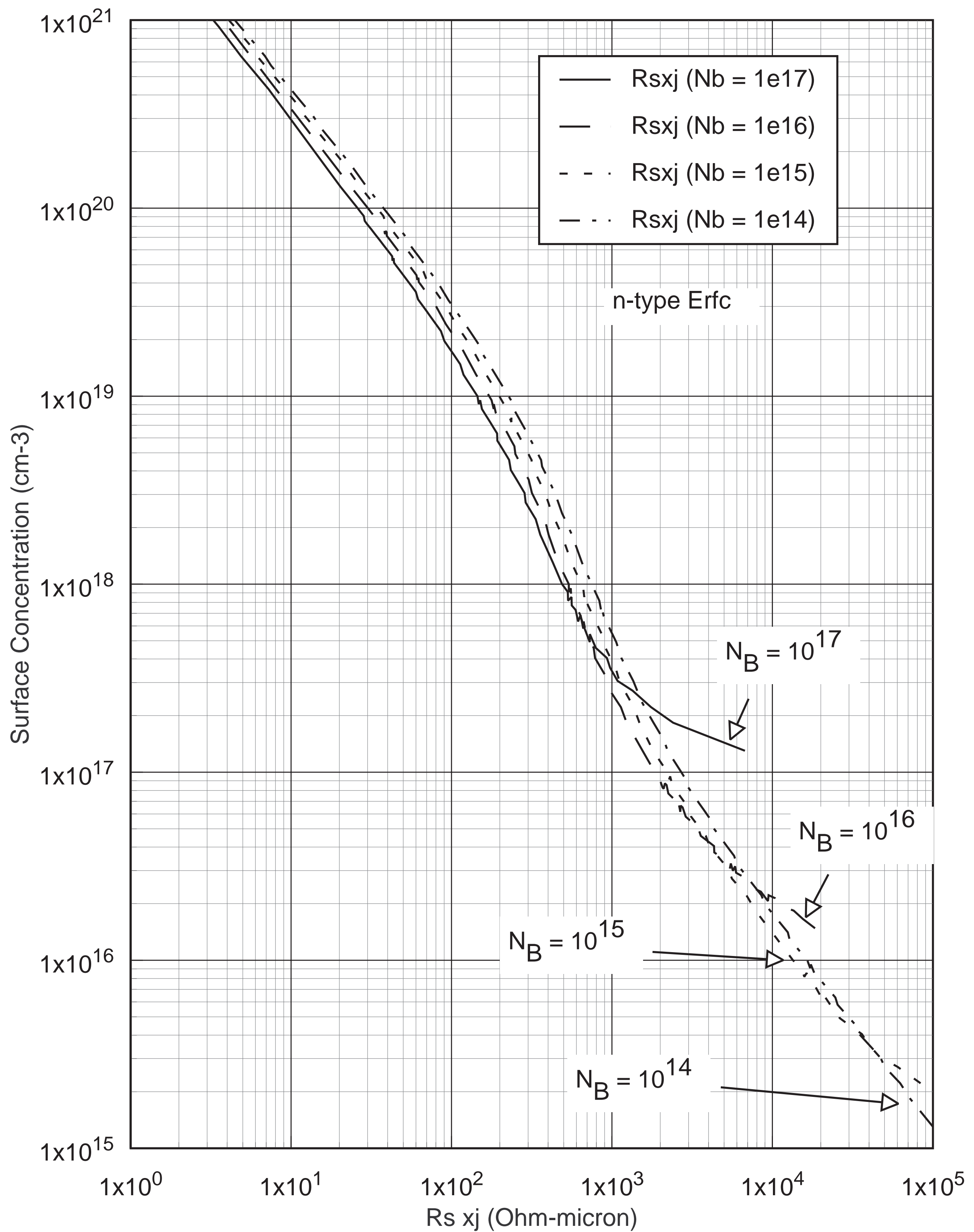


Figure 22: Irvin curve for n-type impurity, erfc profile.

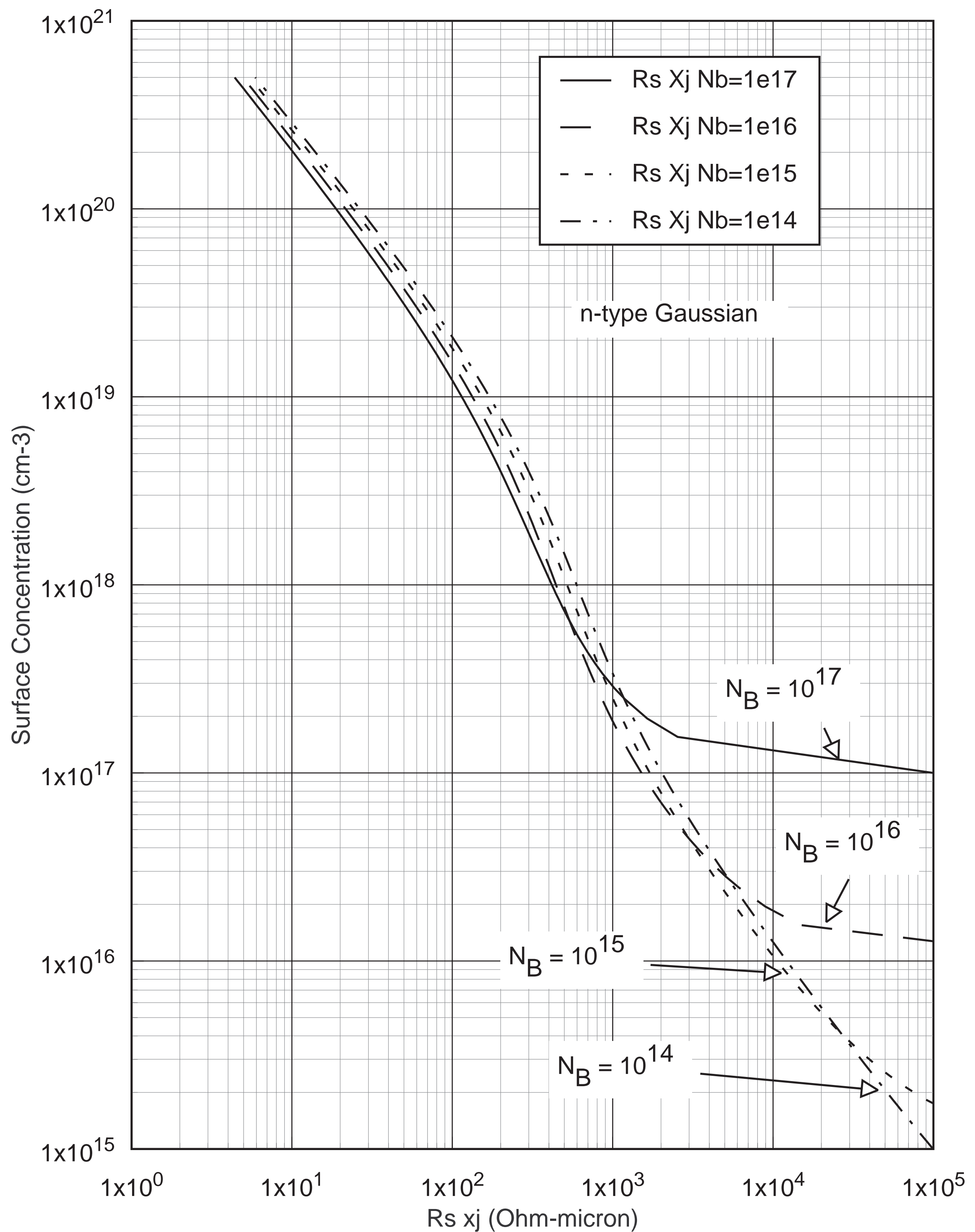


Figure 23: Irvin curve for n-type impurity, gaussian profile.

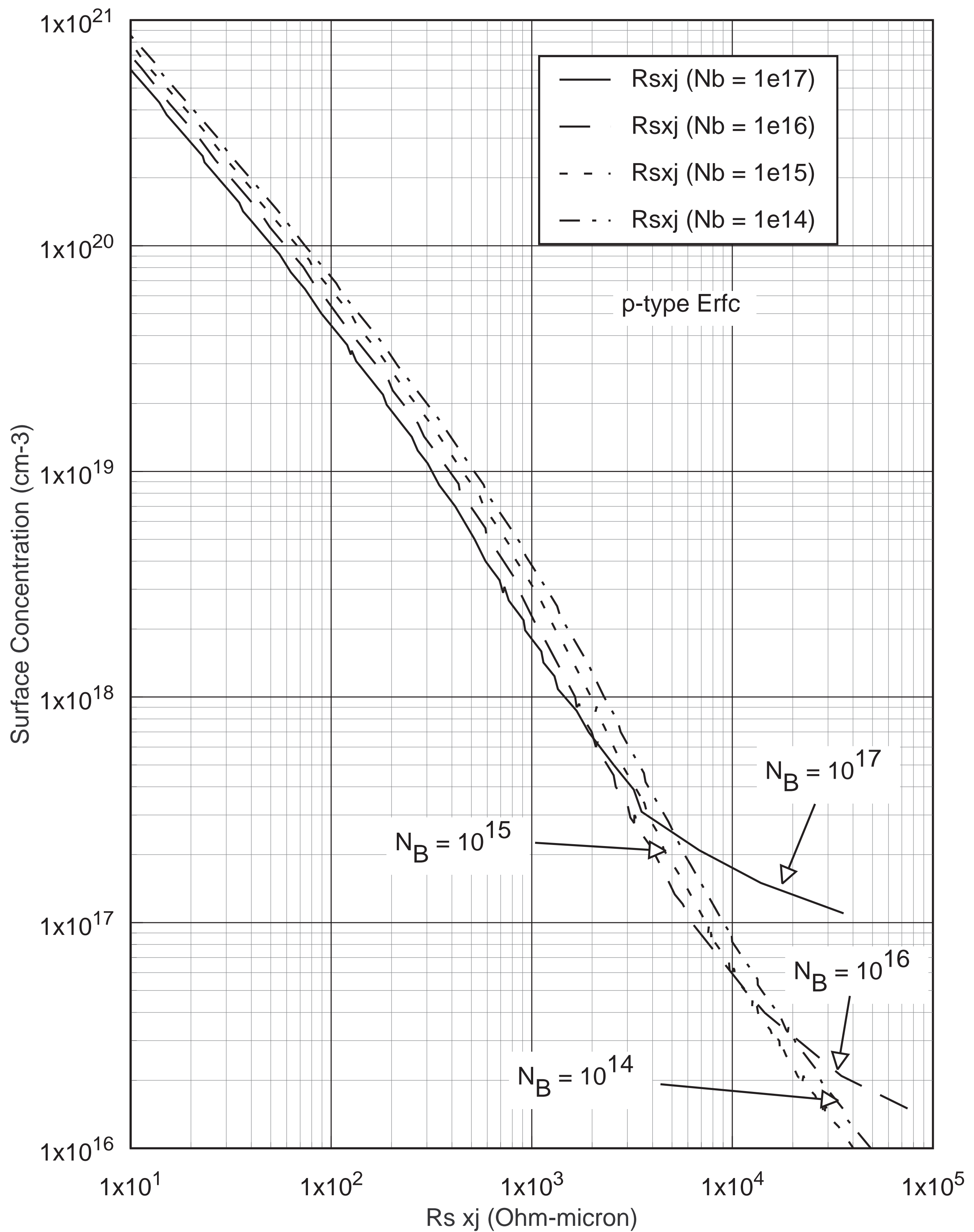


Figure 24: Irvin curve for p-type impurity, erfc profile.

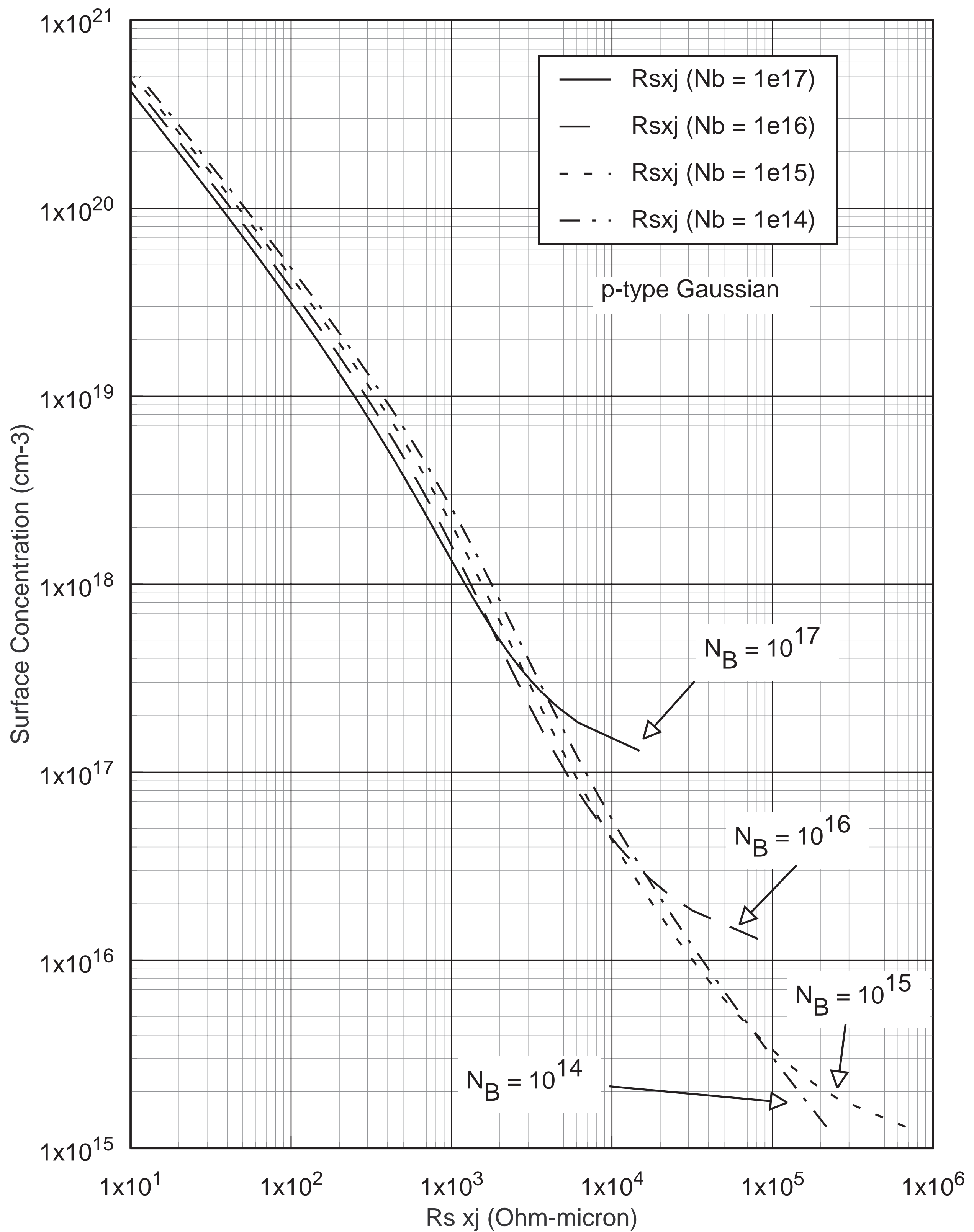


Figure 25: Irvin curve for p-type impurity, gaussian profile.

Drive-in Furnace Operating Procedure

1. Set furnace temperature controller to 100/395/100 on the 900 scale. This will achieve a temperature of 1100˚C in the flat zone. Allow 30 min. for furnace to stabilize.

Step 1 should normally be performed by the lab TA before you arrive.

2. Five (5) minutes before loading wafers turn O2 gas supply ON, set for 66 with glass ball. This is to pre- fill the furnace tube with oxygen.

3. Remove furnace tube end cap and place it behind the furnace load tray. Carefully remove the pull-rod from its storage tube, and pull the wafer boat out onto the load tray. Replace pull-rod and allow 1 min. for the boat to cool.

NOTE: NEVER USE ANY PULL-ROD OTHER THAN THE ONE SPECIFICALLY FOR THE FURNACE YOU ARE USING!

4. LOAD WAFERS: Place clean Si chips in the wafer boat slots. DO NOT TOUCH THE BOAT WITH YOUR TWEEZERS.

5. Using the pull-rod, perform a slow push of the boat into the furnace flat zone. This should take approximately 1 min. The flat zone is reached when the end of the pull- rod reaches the mark on the furnace tray. Replace pull- rod in its storage tube, and loosely replace furnace end cap.

THE PULL-ROD WILL BE VERY HOT: DO NOT TOUCH ANY PORTION WHICH HAS BEEN INSIDE THE FURNACE.

6. Begin timing the drive process at the conclusion of the slow push. For normal drive-ins continue in oxygen for 5 min. At the end of 5 min., turn the O2 OFF, turn N2 ON, set for 66 with the glass ball. Continue for rest of desired drive time.

7. At the end of the drive time remove the furnace end cap and pull the wafer boat out onto the furnace tray. ALLOW BOAT TO COOL FOR 2 MIN. THE PULL-ROD WILL BE VERY HOT: DO NOT TOUCH ANY PORTION WHICH HAS BEEN INSIDE THE FURNACE.

8. Remove samples.

Store boat in furnance neck, replace cap and pull-rod, turn OFF ALL GAS SUPPLIES.

Stand-by (end of lab shut-down)

-Boat should be in the furnace neck.

-All gas supplies OFF.

-Furnace controller: 100/100/100 on the 500 scale.

OP- G: Vacuum Systems and Vacuum Evaporation

filname: VACEVAP

One of the most common pieces of equipment encountered in the semiconductor industry is the vacuum system. Such systems come in many varieties, and are designed to produce low pressures ranging from about 10^{-3} atmospheres to less than 10^{-12} atm. In our laboratory, we use a rotary vane mechanical pump to produce rough vacuums (10^{-2} - 10^{-3} Torr, or 10 to 1 mTorr, where 1 atm = 760 Torr), and an oil diffusion pump to produce high vacuum (10^{-6} Torr). These pumps work in conjunction to evacuate the bell jar which contains our metal evaporation source. Such low pressures are necessary to prevent the evaporating metal from oxidizing. It also allows the metal to go directly from source to chip without undergoing any collisions with residual gas molecules (the mean free path between collisions at 10^{-6} Torr is almost 50 meters, compared to 70 nanometers at 760 Torr). This helps to produce relatively pure, highly conducting metal layers.

The rough pump we use is shown in cross section in Figure 26. The pump consists of a spinning cylinder (the rotor) positioned off-center inside a larger cylinder (the stator). The rotor is precisely machined so it fits very closely against the stator at the top, while spring-loaded vanes make contact with the walls of the stator. When the rotor spins, gas is trapped in the cavity between the vanes, and is swept out the outlet valve. The outlet side of the pump is actually filled with oil so that all parts are covered with a thin layer of oil, which serves as both lubricant and gas seal.

outlet inlet

Figure 26: Rotating-vane two-stage rough pump (from J. O'Hanlon, *A User's Guied to Vacuum Technology*. New York: John Wiley & Sons, 1980, p. 161).

To achieve lower pressures we use an oil diffusion pump, shown schematically in Figure 27. Here a very high purity, low boiling point oil is heated at the bottom of the pump. The hot vapors then rush up the chimney and are ejected downward from the jet assembly. Via collisions between the directed oil molecules and the residual gas molecules, the gas is compressed and swept out the foreline, where it is pumped away by our rotary vane rough pump. The diffusion pump is water cooled to insure that any oil that strikes the pump walls will stick, rather than bouncing off and disturbing the gas flow. In addition, since it is inevitable that some oil will be deflected up towards the

vacuum chamber, we interpose two baffles between the chamber and pump (see Figure 30). These baffles consist of cooled metal chevrons, which do not allow any line-of-sight paths to the chamber. Almost all oil molecules diffusing upward will collide and stick to one of these baffles. It is important to realize diffusion pumps work only at low pressures (below about 10 mTorr) where the mean free paths are fairly large. If the pump intake is exposed to high pressure (≥ 100 mTorr) for any length of time serious damage will result. At these pressures large amounts of oil will be carried into the process chamber, and the oil in the pump will begin to burn. Because of this the pressure in the foreline should never exceed about 500 mTorr (i.e., TC2 ≤ 500 mTorr in Fig. 3 at all times).

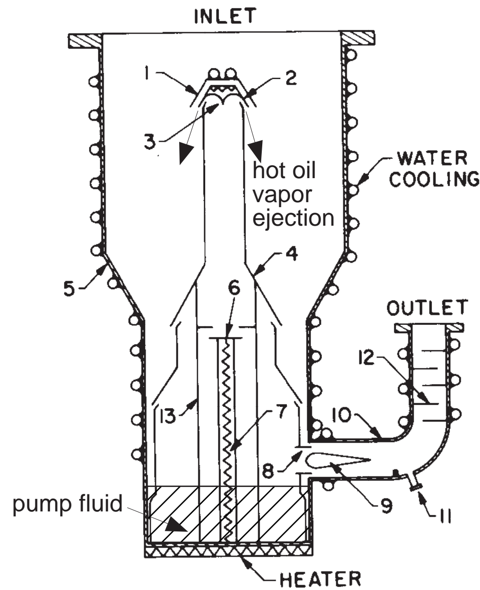


Figure 27: Oil Diffusion Pump

A cross sectional view of a metal-bodied diffusion pump and some of its innovations: (1) Cooled hood for prevention of vapor backstreaming; (2) heater for the nozzle's cap to compensate for loss of heat; (3) streamlined surface to avoid turbulence; (4) multiple stages to obtain low pressures; (5) enlarged casing to give larger pumping aperture; (6) baffle to impede the access to the jet of liquid splashed up from the boiler; (7) heater for superheating the vapor; (8) lateral ejector stage; (9) conical body allowing operation against higher forepressures; (10) hot maintained diffuser for oil purification; (11) catchment and drain-off of highly volatile oil components; (12) baffle to reduce oil loss; (13) concentric chimneys that allow oil fractionation. Adapted from J. O'Hanlon, *A User's Guied to Vacuum Technology*. New York: John Wiley & Sons, 1980, p. 191.

We use two different types of gauges to measure the pressures in our vacuum system. The first is the thermocouple (TC) gauge (Figure 28), used to measure pressures greater than 1 mTorr. There are two TC gauges, one in the foreline (TC2 in Figure 30), and one on the bell jar (TC1 in Figure 30). The operating principle used by these gauges is the relation between gas pressure and gas thermal conductivity. They consist of a hot filament surrounded by a cylinder. A thermocouple is used to measure the temperature of the filament; as gas pressure increases, more heat is transferred from the filament to the cylinder, and the thermocouple gauge output voltage registers the subsequent temperature drop. Thermocouple gauges are quite rugged, and are widely used, although fairly inaccurate.

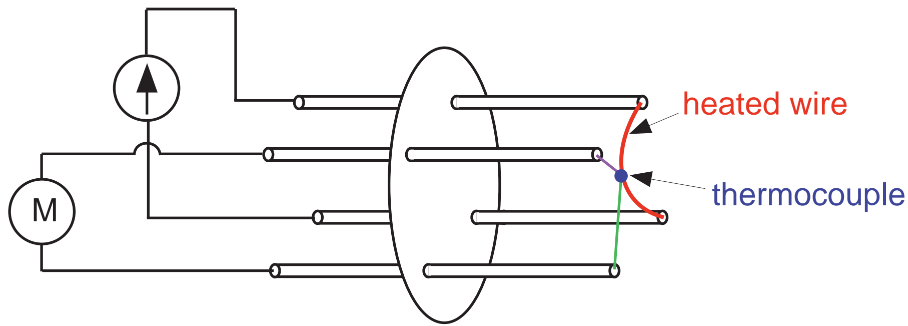


Figure 28: Thermocouple gauge.

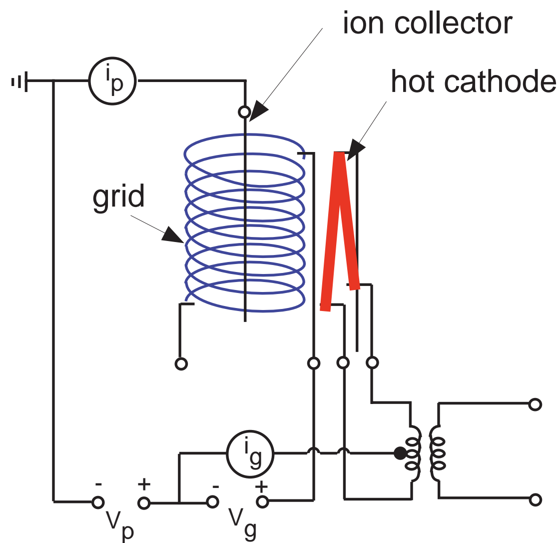


Figure 29: Bayard-Alpert ionization gauge . Adapted from J. O'Hanlon, *A User's Guied to Vacuum Technology*. New York: John Wiley & Sons, 1980, p. 63.

The second type of gauge used in our system is the ionization gauge (Figure 29). These gauges are used to measure pressure from 10^{-10} Torr to 1 mTorr. They use high voltage electron emission to measure pressure. The current which flows between the gauge's anode and cathodes is related to the gas pressure, but not in a linear fashion. These gauges are fairly accurate but are somewhat fragile. Due to the gauge location in our system, the pressure registered is initially higher than that actually in the bell jar.

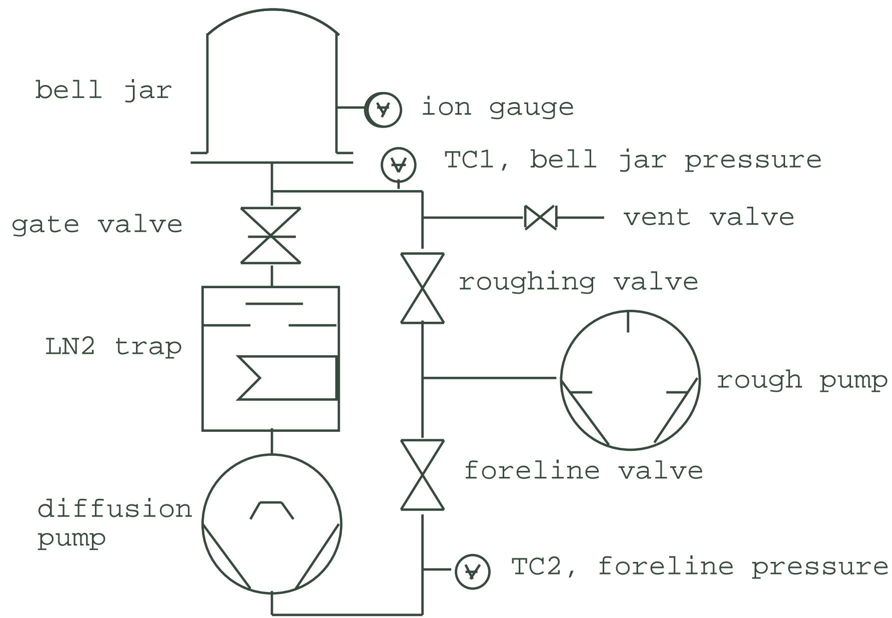


Figure 30: Varian vacuum evaporation system used in our lab.

Once a high vacuum has been established inside the bell jar, the actual metal deposition must still be done. Many different techniques are used in industry, but we use one of the oldest and simplest: resistive heating of the source material. The easiest way of doing this is to use a very high melting point material (such as tungsten) through which a large current is passed. This heater can be in many forms; three of the more common types are shown in Figure 31. The material to be evaporated (see Table 1 for examples) is simply placed in the heater. A variety of problems can be encountered with this technique. When evaporating aluminum, for example, it is found that molten Al is very reactive with the tungsten filament. For this reason we always use a minimum amount of Al, and try to evaporate all of the metal from the filament during each run. Table 1 summarizes many other metal/heater combinations that can be used for evaporations. Nomograph 1 and Table 2 allow the calculation of current necessary in a tungsten filament to achieve various evaporation rates. As a rule of thumb, a vapor pressure of about 10^{-2} Torr is necessary for a moderate evaporation rate of approximately 10 Å per second.

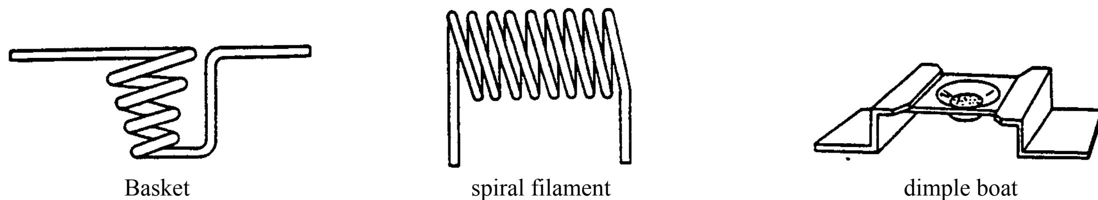


Figure 31: Resistance heated evaporation sources.

Varian Vacuum System Operating Procedure (see Figure 30)

1. SIGN IN on log book. The vacuum sequence controller should be in the AUTO mode, with the STOP light lit.

2. Make sure the FORELINE valve is OPEN, ROUGHING valve CLOSED. Make sure the HIGH VAC valve is CLOSED. TC2 should read less than 10 mTorr.

3. The **TA** will open the BELL JAR VENT VALVE by depressing and holding in the STOP BUTTON on the front panel; continue to hold in the button until the bell jar is fully vented. TC2 should remain at less than 10 mTorr, and TC1 should rise very quickly to 1 atm.

   NOTE: If TC2 rises, IMMEDIATELY close the vent valve by releasing the STOP BUTTON and seek assistance.

4. After venting is complete check to make sure the bell jar is loose, and use the hoist to raise the jar. Remove the evaporation chimney CAREFULLY, and set it aside.

   NOTE: You MUST WEAR GLOVES when handling anything inside a vacuum system. Finger oil is one of the most offensive vacuum contaminates.

5. Load metal into filament: for aluminum, carefully wrap 3" to 4" of aluminum wire around the center of the filament; the wire must be wrapped only in about the central 1/8" of the filament. Check to make sure the filament has not broken: with the evaporation power supply variac set to zero, turn the supply on; then quickly turn up the variac, then turn it back off. The ammeter on the control panel should indicate current flow.

6. Mount chips on the sample holder and then replace chimney and sample holder. Be careful to not hit the Crystal Thickness Monitor, which is used to measure film thickness. Turn the Crystal Thickness Monitor ON, and zero it. Make sure the thickness monitor is working before you begin the pump-down cycle!

7. CAREFULLY lower the bell jar by reversing the hoist. If you hit the chimney while lowering the jar you may dislodge a sample, so be <u>very</u> <u>careful</u>.

8. After the jar is lowered and centered on the base plate make sure the **bell jar VENT VALVE is closed.**

9. Begin vacuum cycle by pressing the START button on the sequencer. The controller will now perform the following steps, while you monitor the items shown in bold-face print:

   a) FORELINE valve CLOSED, pause, ROUGHING valve OPEN.

   b) WATCH TC2 (foreline pressure) - it should remain stable, or rise ONLY VERY SLOWLY. TC2 MUST REMAIN • 200 mTorr.

   c) Watch TC1 (bell jar pressure) ; it should fall to • 200 mTorr in about 2-3 minutes.

   d) When TC1 reaches about 50 mTorr, the ROUGHING valve will CLOSE, and after a pause, the FORELINE valve will OPEN. **TC1 (bell jar pressure) should remain constant or very slowly rise; TC2 (foreline pressure) should drop to less than 10 mTorr very quickly**. After a brief pause, the HIGH VAC VALVE will now open.

   e) Watch TC2: it should jump to about 100 mTorr, and then immediately begin to fall back towards 10 mTorr; TC1 should very quickly drop to zero.

   f) Turn on ION GAUGE.

10. Wait 10-15 minutes. Check to see if LN_2 trap is cold (ask the TA). The ion gauge should read about 10^{-6} Torr.

11. Evaporate metal:

   a) Set current shunt to appropriate feedthroughs. Make sure Crystal Thickness Monitor is ON, and zeroed. Make sure shutter is CLOSED.

   b) Make sure VARIAC is at ZERO, then turn on power supply. While watching through cracks above and below the chimney, turn VARIAC up until you see a glow.

   c) Set CURRENT to evaporation level:
      Aluminum: about 50 Amps
      Gold: about 40 Amps
   Wait about 10 seconds, then open shutter between the chips and the evaporation filament.

   d) Watch the Thickness Monitor display; it should register the depositing metal, at a rate of around 10 Å/sec. After about 2 min. the rate should rapidly drop; you have now evaporated all the aluminum that

was on the filament. NOTE THE THICKNESS DEPOSITED FOR LATER REFERENCE.

e) Close the shutter.

f) TURN VARIAC TO ZERO, power supply off.

12. Let samples cool under vacuum for 5 minutes. Turn ion gauge off.

13. Begin shut-down by pressing the STOP button :

a) The HIGH VAC valve will close.

b) While watching TC2, the TA will open the bell jar vent valve by pressing and holding the STOP button. **TC2 SHOULD NOT CHANGE. If TC2 increases, immediately close the vent valve by releasing the STOP button; check to see if the HIGH VAC VALVE IS CLOSED.**

c) Continue venting by holding in the STOP button until jar is at atmosphere.

d) Remove samples.

14. Vacuum System standby:

Repeat steps 7,8 and 9, but IMMEDIATELY AFTER THE HIGH VAC VALVE OPENS, PRESS STOP. DO NOT VENT THE BELL JAR.

When you leave the system the valves should be set as follows:

HIGH VAC VALVE CLOSED.
FORELINE VALVE OPEN.
BELL JAR VENT VALVE CLOSED.

The gauges should read as follows:

TC2 (foreline pressure) • 10 mTorr
TC1 (bell jar pressure) • 100 mTorr
ION GAUGE OFF.

OP-H: Measurement of Semiconductor Resistivity using a Four Point Probe

filnemame: 4PTPR

The resistivity , ρ, of a sample is an important parameter, since it can be related to impurity concentration (to characterize a doping process, for example), as well as having direct effects on device performance. A simple, nondestructive way of determining ρ utilizes the four point probe, shown schematically in Figure 32. Here four sharply tipped tungsten wires (tungsten is chosen for its hardness) are brought into contact with the semiconductor surface. One immediate problem arises from the contact between the metal and the silicon. At the very least, the Schottky diodes formed there make it impossible to measure resistance using a simple ohm meter and only two connections.

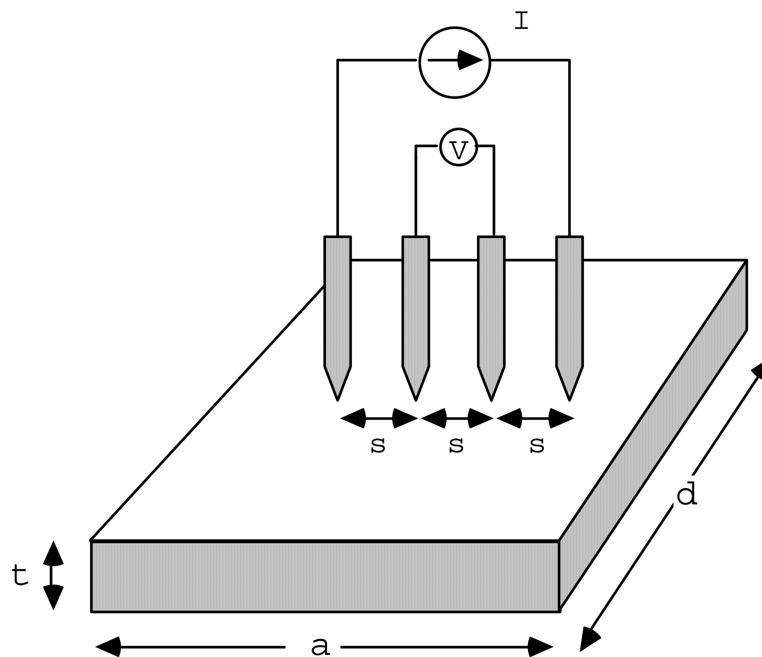


Figure 32: **Four point probe; sample dimensions and orientation of probe refer to Table 13.**

The four point probe avoids this problem by using a row of four equally spaced needles. A known current is passed between the outer needles, while an open-circuit voltage reading is made between the inner needles. Because no (or very little) current flows through the voltage sensing needles, there are no errors introduced due to the contacts. Of course, there are large voltage drops across the outside needle contacts, but we measure only current in this part of the circuit.

We are faced with another difficulty, however, in extracting the resistivity from the measured I and V. Here the current-carrying probes (outer probes) represent a dipole source, which establishes a field distribution inside the specimen under test. We must solve for the potential difference between the two inner probes under various boundary

conditions, set by the sample size and thickness, to derive expressions relating the supplied current, the measured potential difference, and the resistivity of the specimen.

In two limiting cases it is relatively straightforward to find these expressions. For a semi-infinite sample the resistivity is given by

$$\rho = (2\pi s)V/I \qquad (1)$$

where the probes are assumed to be equally spaced by s (ref.1).

The second case is somewhat more useful, the "thin" two- dimensional conducting sheet. Here the current is assumed to be completely confined to a layer t thick, where t is thin, i.e., t << s. For such sheets it is convenient to define the "Sheet Resistance", R_s, in ohms/square, or $\Omega/\square$. This is simply the resistance of a bar of material of unit length and width, with thickness t. Clearly if t is known, then

$$\rho = R_s t \quad (\Omega\text{-cm}) \qquad (2)$$

and for the two-dimensional sheet (ref. 2),

$$R_s = (\bullet/ln2)V/I = 4.53\ V/I \ (\Omega/\square) \qquad (3)$$

In the case of a sample which has been doped by a diffusion process, the resistivity of the diffused layer is much lower than the substrate, which confines almost all the current to this layer (or if the diffusion is of opposite type to the substrate the resulting p-n junction serves to block current from flowing into the substrate), and the requirement t << s is easily satisfied. Also note that since the depth of the diffusion, t, must be determined in some other manner, it is common to give only the sheet resistance, R_s. When t is known eqs 2 and 3 give

$$\rho = 4.53\ t\ V/I \quad (\Omega\text{-cm}) \qquad (4)$$

In the above cases, no edge effects have been considered, and the calculated potential distributions are due to a single dipole source only. For a real sample of finite size, however, the edge effects cannot be ignored. The so-called "diameter" correction factor, CF_d, and "thickness" correction factor, CF_t, have to be considered separately to account for finite sample size. The method of images can be used here to solve for the potential in the presence of finite boundaries. The basic principle is to remove the edges by mirror-imaging the dipole source through the imaginary edge plane, and treat the whole problem in a single medium. As a result, a single dipole source is now replaced by an infinite arrangement of dipoles. Once again, the potential difference between the inner probes due to these infinite dipoles can be solved numerically. The resulting diameter and thickness correction factors are given in tables 1 and 2. The bulk resistivity and sheet resistance for a real sample can thus be expressed in final form as

$$\rho = (V/I)tCF_dCF_t$$

and

$$R_s = (V/I)CF_dCF_t$$

For any epitaxial or diffusion layer in our lab, t/s < 0.5, and CF_t=1. In fact, the thickest conductive layer we encounter is our wafer substrate, t ≤ 0.025". Our probe spacing s = 0.040", so even for a bare wafer, t/s ≤ 0.625, and CF_t ≥ 0.9898. Note, however, that for many of our samples the diameter correction factor, CF_d, cannot be set to its limiting value of 4.53.

MEASURING PROCEDURES

1. Measure dimensions of the specimen. The probe head tip spacing s is 0.040". Estimate correction factors CF_d and CF_t.

2. Turn the HP current source on by setting the *Function Selector* switch to *DC*. Make sure the *Output Switch* is set to the *OFF* position (this is a center off switch). The initial *Range* setting should be 0.1mA, and the *Current Multiplier Dial* should be set at 0.500.

3. Place specimen on insulated vacuum chuck, turn on vacuum, and locate sample under probe head. Lower probe head by pressing front lever down until it stops. **Make sure the current source *Output Switch* is OFF before lowering the probe head onto the wafer.** The probe tips should retract at least 0.040" into the head after contact is made. Lock head down with the locking screw on the left side of the prober.

NOTE: The probe head is a precision made instrument! Care must be exercised--no excessive force should be exerted. Actual contact is maintained via springs internal to the probe head to insure repeatable contact pressures.

NOTE: THE MEASUREMENTS MADE BELOW MAY EXHIBIT SIGNIFICANT DEPENDENCE ON ILLUMINATION. YOU SHOULD TRY TURNING OFF THE ROOM LIGHTS TO DETERMINE IF YOUR SAMPLES ARE SENSITIVE; IF SO, MAKE MEASUREMENTS IN THE DARK.

4. Set current range to obtain a voltage reading of between 15 and 20 mV:

   i) To apply a current to the sample depress and continue to hold down the *Output Selector* switch to the *ON TEST* position (this is a momentary contact switch; when you release it the *Output Selector* switch returns to the *OFF* position).

   ii) Read volt meter; if

      a) V • 2mV, release *Output Selector* switch, change the *Range* selector to the next higher decade, and read volt meter again

      b) V • 2mV, repeat step (i) and (iia) above until

      c) 2mV • V • 15mV, adjust the *Multiplier Dial* until

      d) 15mV • V • 20mV, record V and I.

5. Reverse the polarity of the current by reversing the banana plug connections to the current supply, and

repeat step 4. **Make sure the *Output Selector* is OFF before reversing the polarity.**

6. If the "positive" and "negative" measurements above are within approximately 4% of each other, you can assume confidence in the readings. If not, see your TA.

7. Average readings from 4 and 5, and using correction factors calculate R_S and ρ (if t is known).

8. **Make sure the *Output Selector* is OFF before raising the probe head from the sample. Serious damage to the probe head may result if the current source is still applied to the sample when the head is raised!**

Table 13: Diameter Correction Factor CF_d (after ref. 2).

	CIRCLE	a/d ratio			
d/s		1	2	3	• 4
1.0				0.9988	0.9994
1.25				1.2467	1.2228
1.5			1.4788	1.4893	1.4893
1.75			1.7196	1.7238	1.7238
2.0			1.9454	1.9475	1.9475
2.5			2.3532	2.3541	2.3541
3.0	2.2662	2.4575	2.7000	2.7005	2.7005
4.0	2.9289	3.1137	3.2246	3.2248	3.2248
5.0	3.3625	3.5098	3.5749	3.5750	3.5750
7.5	3.9273	4.0095	4.0361	4.0362	4.0362
10.0	4.1716	4.2209	4.2357	4.2357	4.2357
15.0	4.3646	4.3882	4.3947	4.3947	4.3947
20.0	4.4364	4.4516	4.4553	4.4553	4.4553
40.0	4.5076	4.5120	4.5129	4.5129	4.5129
INF	4.5324	4.5324	4.5324	4.5324	4.5324

Table 14: Thickness Correction Factor (after ref. 1)

t/s	CF_t
0.4	0.9995
0.5	0.9974
0.5555	0.9948
0.6250	0.9898
0.7143	0.9798
0.8333	0.9600
1.0	0.9214
1.1111	0.8907
1.25	0.8490
1.4286	0.7938
1.6666	0.7225
2.0	0.6336

Table 15: 4 point probe current settings (after ref. 3)

Approximate Resistivity (Ω-cm)	Set Current for (mA)
0.012	100
0.008 - 0.6	10
0.4 - 60	1
40 - 1200	0.1

References

1. Valdes, L.G., Proc. I.R.E. Vol. 42, pp. 420-427 (Feb. 1954).

2. Smits, F.M., "Measurements of Sheet Resistivity with the Four-Point Probe," BSTJ, 37, p. 711-718 (1958). (Same as BT Monograph , 3894, Part 2).

3. American Soc. for Testing and Materials, ASTM F 84, Part 43.

OP-J: Wafer Cleaning

filename: CLEAN

One of the most mundane operations performed in silicon integrated circuit processing is wafer cleaning. It is also one of the most important and difficult steps to perform well. There are three broad categories of contamination that must be removed by the cleaning process: organic residue (photoresist, organic solvent residues, synthetic waxes, fatty acids from human contact); inorganic ions (sodium, potassium, calcium); and inorganic atoms (gold, copper, iron). The following cleaning process is an adaptation of the so-called "RCA Clean", named after the work done by Kern and Puotinen at RCA Laboratories in 1970.

1. Gross organic contamination removal:
(note: depending on the level of the contamination certain of the steps below may be omitted).

a) Immersion in hot trichloroethane (TCA) in ultrasonic bath.
b) Immersion in hot acetone in ultrasonic bath.
c) Immersion in ethanol.
d) High purity water (HPH2O) rinse.

This sequence is our standard quick organic strip. Each subsequent rinse is a solvent for the one immediately preceding it. The idea is to finish with a very high purity, non-volatile solvent (i.e. the HPH2O). This can be blown off the wafer. It is important to never allow a cleaning solvent to evaporate directly from the surface of the wafer; if it does any impurities will simply remain behind on the silicon.

2. High purity organic strips:
(note: these two steps may be used in sequence, or separately)

a) Oxygen plasma strip: The O2 plasma is a very efficient way of "burning" off organics (see OP-K). This process, if used for a sufficient time, will remove almost any organic contamination. It may, however, also damage any metal present that is susceptible to oxidation.
b) Caro's Acid (Pirana etch): immersion in a 1:1 solution of concentrated H2SO4 and 30% H2O2. **This is a very vigorous oxidizing solution**, and is commonly used in industry. Bath temperature is typically 95˚ C, immersion for about 15 min. Finish with HPH2O rinse.

3. Trace organic strip (RCA solution 1):

a) Immersion in SC-1 solution, consisting of 5:1:1 to 7:2:1 parts H2O : H2O2 : NH4OH (30% H2O2, 27% NH4OH). All of the preceding organic strips will leave a trace organic film; this is the only process that has been found to be highly effective in removing this final contamination layer. Typical bath temperature is 75 - 85˚ C, immersion time 10-20 min. Care must be exercised since NH4OH will etch bare silicon. In the presence of H2O2 a thin layer of SiO2 is formed which protects the silicon; if insufficient H2O2 is used, or the bath is old

(the H_2O_2 breaks down to H_2O and O in about 40 min) etching will occur. Finish with HPH2O rinse.

b) Removal of the SiO_2 layer formed by SC-1 solution : etch in dilute HF, about 60 sec; finish with HPH2O rinse.

4. Inorganic contamination removal (RCA solution 2):

a) immersion in SC-2 solution, consisting of 5:1:1 to 7:2:1 parts H_2O : H_2O_2 : HCl (30% H_2O_2, 37% HCl). This solution has been found to be highly effective in removing almost all metallic contaminates through acid complexing reactions. Typical bath temperature is 75 - 85˚ C, immersion time 20 min. Finish with HPH2O rinse.

One final note: in our lab we do not follow these cleaning procedures rigidly, mainly for convenience sake. One particular problem is the glassware necessary for very high purity work: the pyrex used in our common beakers is a source of both sodium and boron, which can recontaminate the cleaned wafers. In industry only pure quartz would normally be used for the etching and cleaning tanks.

References

"Optimizing the Cleaning Procedure for Silicon Wafers Prior to High Temperature Operations," D. Burkman, Semiconductor International, July, 1981, 103-116.

"Cleaning Solutions Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology," W. Kern and D.A. Puotinen, RCA Review, June 1970, 187-206.

OP-K: Plasma Ashing

filename: PLASMD

Plasma "ashing" is a very effective technique used to remove trace organic contamination from the surface of a chip. This is accomplished by using a RF plasma discharge to create highly reactive oxygen species (excited molecular O_2, ionized O_2, ionized atomic oxygen, and some excited ozone, O_3) which combine with the organic compounds. The resultant products are mostly the volatile species H_2O, CO_2, and CO. This process of "burning" organic material is one of the oldest uses of plasma processing in the semiconductor industry.

Our plasma asher is a particularly simple example of a barrel reactor. A pyrex clinder is used for the vacuum chamber, and is surrounded by the RF electrode plates. A 13.56 MHz power source drives the plates, creating a plasma inside the chamber. In our unit we use a needle valve to regulate the flow of 0_2 into the reactor so that a pressure of approximately 0.5 Torr is maintained. Between 50 and 100 watts can be delivered to the plasma.

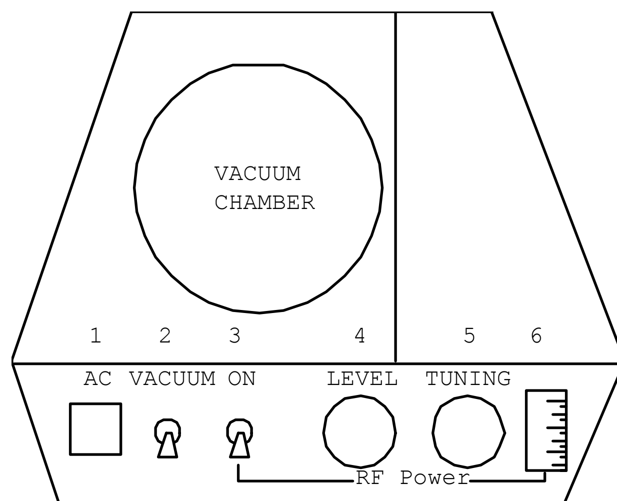


Figure 33: Plasmod Controls and Indicators

Front Panel, Figure 1: Reference Numbers from Left to Right in Figure 1.

1. AC Power On/Off Button:
   Button is lighted when "ON".

2. Vacuum Toggle Switch:
   Controls both solenoid valves (vacuum and atmosphere); in down position reaction chamber is open to atmosphere and closed to vacuum pump. In "up" position chamber is open to vacuum pump and closed to atmosphere.

3. RF Power Toggle Switch:
   "Up" Position RF power is applied to electrodes; "Down" position RF power is "Off".

4. Level Knob:
   Adjusts RF power level 0-100 watts.

5. Tuning Knob:
   Adjusts variable capacitor to tune circuit (indicated by dip in meter reading).

Operating Procedure

1. The Plasmod should be on (AC power) when you arrive. If it is not, turn both it and the vacuum pump ON, and allow 10 minutes for warm-up.

2. Make sure both the VACUUM and RF POWER switches (see fig. l) are OFF, then open the door and carefully slide out the pyrex tunnel. There should be a large petri dish or a slotted wafer boat inside. These are NOT ATTACHED TO THE TUNNEL, SO BE CAREFUL.
Set the tunnel on the table, open end facing you.

3. Set your samples on the petri dish, side-to-be-cleaned up, or in the wafer boat.

4. Close door and turn vacuum switch on. Watch pressure gauge; it should pump down to about 100 mTorr in 30-60 sec.
.pa
5. Turn O_2 Supply ON; use only the toggle value on the gas panel. DO NOT ADJUST NEEDLE VALVES.
The pressure should rise to about 600 mTorr.

6. Make sure RF POWER LEVEL knob is set to minimum (fully ccw). Turn RF power switch ON, then turn POWER LEVEL KNOB cw until the power meter reads approx. 50 W.

7. Immediately adjust the RF TUNING KNOB until the RF POWER METER registers a minimum (tune for a dip). A glow discharge should appear in the chamber as a pale purple glow.

NOTE: IF NO DISCHARGE APPEARS AND YOU CANNOT GET THE POWER METER TO REGISTER A MINIMUM, IMMEDIATELY TURN THE POWER LEVEL DOWN, AND THE RF SWITCH OFF.
ASK FOR ASSISTANCE.

8. Once the discharge appears, increase the power level to maximum (fully cw), and re-tune, again for a minimum. Continue to monitor tuning and discharge throughout the ashing cycle.

9. Ashing time depends on how serious the contamination is. Approximately 5 min. is usually adequate.

SHUT DOWN

10. Turn power level to minimum (fully ccw). Turn RF POWER switch OFF.

11. Turn O_2 supply OFF, THEN turn VACUUM/VENT switch OFF (down). This will disconnect the vacuum pump from the

chamber and also vent the chamber to atmosphere.

12. Open door, carefully remove the tunnel and your sample, then replace the tunnel.
NOTE: THE CHAMBER, PETRI DISH, AND SAMPLE WILL BE QUITE HOT!

DO NOT TURN THE AC POWER OFF. LEAVE PLASMOD ON UNTIL THE END OF THE LAB PERIOD.

End of Lab Shut-down:

1. Turn vacuum pump OFF.

2. With Plasmod still ON, slide the tunnel out slightly, and then turn the Vacuum Toggle Switch ON (i.e. up). This will vent the rough pump to atmosphere, which MUST BE DONE whenever the pump is switched off.

OP-L: Photolithography

filename: LITHO

The fabrication of planar semiconductor devices and integrated circuits requires the formation of patterns on the surface of the circuit substrate. The process most commonly used to form these patterns is called photolithography. This technique uses a thin, photosensitive organic film, called photoresist, to transfer the pattern from a master mask to the IC substrate. Figure 34 illustrates the photolithographic process for two basic kinds of resist material, positive photoresist and negative photoresist. In this example the ultimate objective of the process step is the formation of openings to the silicon surface through a SiO_2 film, which could then serve as either a diffusion mask or a contact pattern. To begin the process the wafer is cleaned and dried, and the photoresist (PR) is applied. The PR is supplied in a viscous liquid form; it can easily be formed into a very thin (about 1 μm) and uniform layer by spinning a liquid-coated substrate at high speed. During the spin most of the solvents in the resist evaporate, but after spinning a pre-bake is performed to further dry and harden the film. As shown in the top segment of Fig. 1, the resist is exposed through a mask with the desired pattern on it. For a negative PR, the exposed areas are rendered insoluble by exposure to light. When immersed in a developer solution the unexposed regions are dissolved, leaving exposed regions covered by the resist. For a positive PR, the exposed regions are rendered soluble by exposure to light, and so after development only areas unexposed are still covered by resist. The resulting patterned substrate must then be placed in an etch (in this example, buffered HF), for which the resist serves as an etch mask. In this OP we are concerned with the application and development of the photoresist.

We use exclusively positive photoresists in our laboratory. There are a number of reasons for this, several of which will be discussed in lecture. Two important reasons are the somewhat simpler developing process (a slightly alkaline solution followed by a water rinse) and more durable film produced by positive resist. The characteristics of the resist we use are given in the data sheet on page IV-3.

Note that for these resists any area exposed to light will wash off in the developer, so care must be taken to avoid accidental exposure. Our Litho Room has yellow lights which do not expose the PR; the regular fluorescent room lights, **as well as an unfiltered microscope illuminator**, will expose the PR. Be careful not to expose a chip to these lights until it has been exposed with the mask aligner and developed.

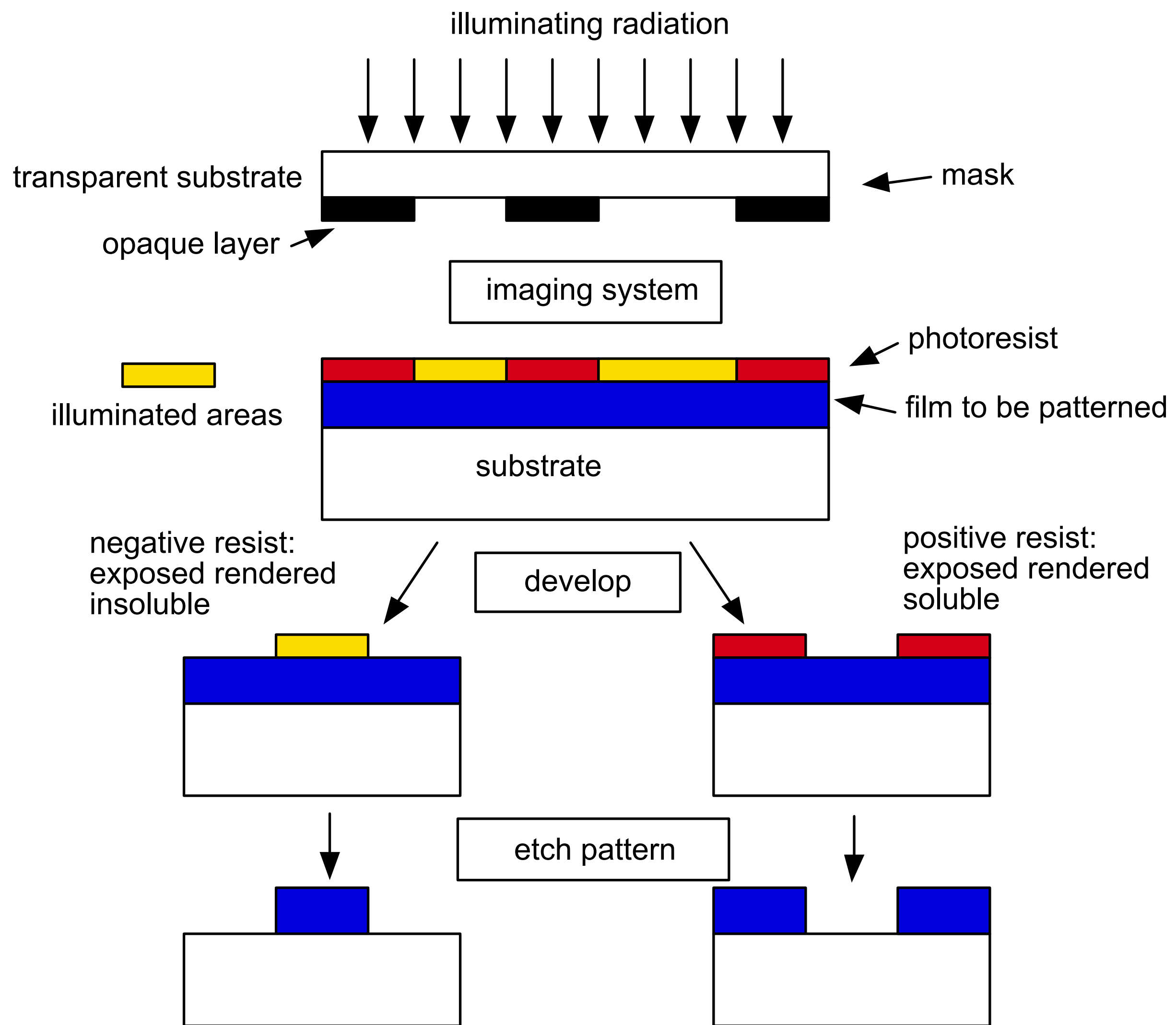


Figure 34: Basic lithographic process (adapted from Introduction to Microlithography, Thompson et al)

The operating procedure for processing the positive resist we use is given on the next page. Several important features should be noted:

- Pre-bake: dries and hardens film; time, temperature, humidity affect photospeed of resist
- Exposure: check Mask Aligner log book for current time
- Development: there is a large development latitude so time is not critical; make sure to fully rinse chips HPH_2O before drying
- Flood Exposure: required to make removal of post-baked resist easier; during exposure positive PR liberates N_2, which if the exposure intensity is too high, can cause resist lift-off from substrate; this is the reason for the 5 sec/pause/5 sec/etc exposure used here
- Post-bake: required to harden PR and to improve adhesion of PR to substrate for later wet etch steps

References

Photoresist: Materials and Processes, W.S. DeForest, McGraw Hill 1975, ISBN 0-07-016230-1

Introduction to Microlithography, eds. L.F. Thompson, C.G. Willson, M.J. Bowden, American Chemical Society, 1983, ISBN 0-8412-0775-5.

Operating Procedure OP-L

1. Dehydration bake: Bake out the sample in the Post-bake oven for 5 mins. (The Post-bake oven is set at a temperature 125˚ C).

2. Place chip on spinner chuck. Carefully open the Adhesion Promoter bottle and using the eyedropper, put a drop or two of Adhesion promoter at approximately the center of the sample. (When replacing the dropper, DO NOT spill any Adhesion fluid on to the threads of the bottle top.) Start the spinner (step on foot pedal). If necessary, adjust controller for spin rate of approximately 4000 rpm. Set timer for 30 sec.

3. Apply Photoresist: At the end of spin-cycle, repeat Step 2 using the positive photoresist (AZ1350J or equivalent). We are using a syringe-like dispenser with a particulate filter to remove any large "boulders" that could contaminate your film. See TA's for instructions on proper use of these dispensers. Don't be afraid to use too much photoresist, since the excess will spin off.

4. Pre-bake: At the end of the spin cycle, remove the sample and do a 10 min pre-bake in the pre-bake oven at 95˚.

5. Expose: The sample is now ready for alignment and exposure: use OP-O, align the sample with the appropriate Mask on the Micro-Tech Mask Aligner. Having aligned the sample with the Mask, do a 15 sec. exposure to UV light. CHECK FOR NEW EXPOSURE TIME IN LOG BOOK. At the end of the exposure, remove the sample, replace the mask in the appropriate container. The sample is now ready for development.

6. Develop: The development station is located on the left side of the sink. The station has 3 beakers marked Developer, H2O, and H2O. (The three beakers should be set up by the T.A.). Using a pair of tweezers, dip the sample into the developer for 60 sec. Remove the sample at the end of the 60 sec. and rinse in the water in the next two beakers. Carefully blow sample dry. Inspect.

7. Flood expose under UV lamp for approx. 5 sec., pause, 5 sec., pause, 5 sec., for a total of 15 sec.

8. Post Bake: in the post bake oven, perform bake at 125˚C for 10 min. The sample is now ready for any subsequent processing.

Resist Developer make-up:

18. AZ Developer:high purity water, in ratio 1 : 1.
19. Approximately 80-100 ml will develop about 4 chips.

Basic Photolithography

1) CLEAN YOUR SUBSTRATE!!!!
Photoresist does NOT like to stick to DIRTY or WET substrates. Immediately prior to PR application a dehydration bake is a good idea: 125o, approx 5-10 min.

2) SPIN ON PHOTORESIST
Make absolutely sure your sample COMPLETELY COVERS THE VACUUM CHUCK. First apply adhesion promoter (a couple of drops) and spin dry (check the spin speed during this step). Now apply a few drops of photoresist in the center of the chip.
Spin: 4,000 to 5,000 rpm, 30 sec.

3) PREBAKE: 95˚C, 10 min.; the time is important.

4) EXPOSE: note: the UV lamps take approx. 15 min to warm up. Microtech aligner: approx. 15 sec. Check log book for current exposure.

Turn the aligners OFF when you finish. DO NOT TURN OFF THE UV LAMP unless everyone is done for the day. THE LAMPS MUST COOL 30 min. AFTER THEY ARE TURNED OFF BEFORE THEY CAN BE RESTARTED.

5) DEVELOP:
AZ Microposit Developer, diluted 1:1 with DI water.
Time: normal process: approx. 60 sec.

DEVELOPER SHOULD BE USED ONLY IN BEAKERS LABELED FOR IT. NEVER PUT DEVELOPER IN BEAKERS LABELED FOR WATER. After use dispose of developer in sink; don't be stingy in how much you use-developer is cheap. RINSE ALL BEAKERS THOROUGHLY AFTER USE.

6) RINSE thoroughly in DI, blow dry.

7) FLOOD EXPOSE: approx. 5 sec., pause, 5 sec.

8) POST BAKE: 125˚C, 30 min.

OP-M: Introduction to Capacitance Measurements

filename: CVMAN

This section is intended as a brief review of semiconductor device physics as they pertain to capacitance-voltage measurements on the devices made in our lab. For more detailed information see, for example, Streetman's Solid State Electronic Devices (Prentice Hall, 1980) and Nicollian and Brews' MOS Physics and Technology (Wiley, 1982).

NOTE: All capacitance measurements are affected by the fact that any real device has finite "leakage current". From a circuit perspective, the real device under test is at best a parallel C - G circuit (i.e., a capacitor in parallel with a conductance G). To interpret measured data it is critical that you either know or can estimate whether the device is dominated by current flowing through the capacitor, or the conductance, or is split between the two with significant contribution from each. For a frequency independent capacitance and conductance, which dominates is clearly frequency dependent since the capacitive admittance has magnitude of ω*C. Hence, for a device dominated by the capacitance, the inequality $G / (\omega C) \ll 1$ should hold. If the measuring instrument used determines the complex admittance at a given frequency, then you should be able to calculate this ratio; to apply the C-V analysis discussed below you must have $G / (\omega C) \ll 1$!

A. p-n Junction Diodes

Due to the differences in Fermi level position relative to the band edges for p-type and n-type semiconductors, at a p-n junction in thermal equilibrium (or under reverse or small forward bias) there exists an electric field across a transition region of width W that straddles the metallurgical boundary. Within this "depletion" region the field sweeps out all free carriers, leaving behind uncovered (exposed) donor and acceptor ions. See Figure 35 for an abrupt junction under zero bias.

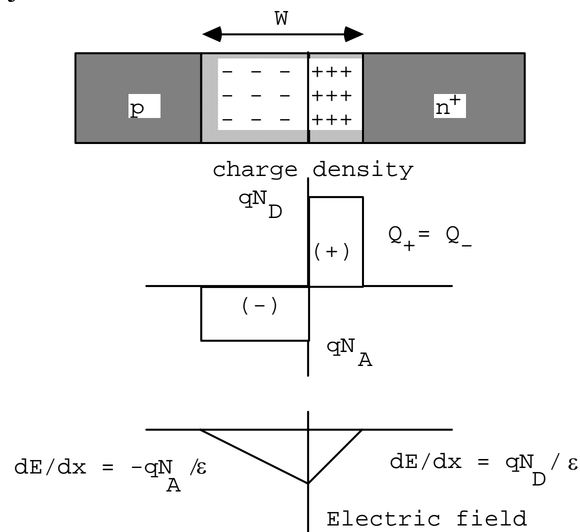


Figure 35: p-n junction capacitance

When a small ac voltage is applied on top of a dc reverse bias (which determines *W*) the width of the transition region varies as fewer or more impurity charges are uncovered at the edges of the region. This variation gives rise to a junction transition capacitance:

$$C = dQ/dV = \varepsilon_s \varepsilon_o A/W \qquad (1)$$

where ε_s is the dielectric constant of the semiconductor, $_o$ is the permittivity of free space, and A is the junction cross-sectional area.

The thickness of the depletion layer *W* will depend on the doping profiles on both sides of the junction, as well as the magnitude and sign of any applied bias. For increasing reverse bias the depletion width increases, so the transition capacitance decreases. Under small forward bias *W* becomes very small, and the transition capacitance reaches a maximum. In general, the relation between junction capacitance (per unit area) C', applied voltage V_a, and doping profiles $N(x_n)$ in the n-type material and $N(x_p)$ in the p-type, is quite complex:

$$N(x_n) = -[(C')^3/\varepsilon_s \varepsilon_o q(dC'/dV_a)][1 + N(x_n)/|N(-x_p)|] \qquad (2)$$

where x_n is the width of the depletion layer on the n-type side of the junction, and x_p the width on the p-type side (so $x_n + x_p = W$). For an abrupt junction with one side much more heavily doped than the other, for example a p^+-n junction, the term on the right side becomes one, and $N(x_n)$ can be determined by measuring the C-V curve of the diode. Also note that for such a diode $W \propto V^{1/2}$, so from eq. 1 we would expect $C \propto V^{-1/2}$. For a linearly graded junction $x_n = |x_p|$, $W \propto V^{1/3}$, and $C \propto V^{-1/3}$.

B. MOS Capacitors

A typical (non-ideal) C-V curve for a metal-oxide-semiconductor capacitor is shown below at both high and low frequency.

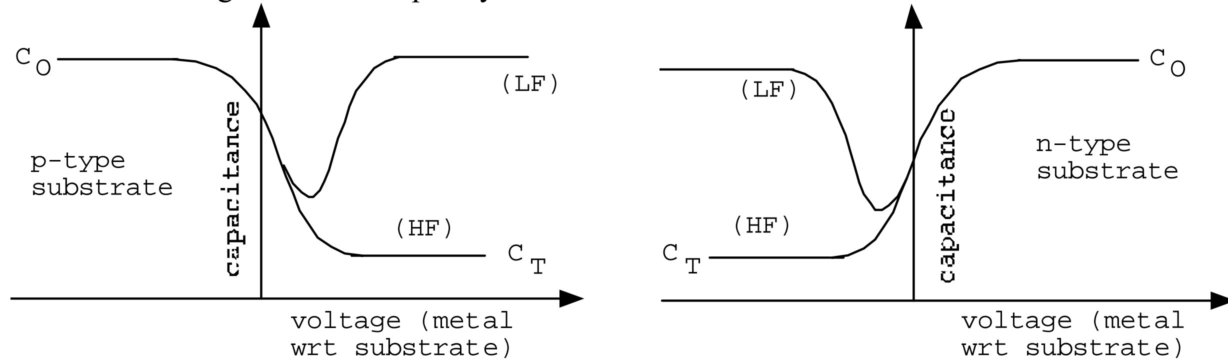


Figure 36

Here C_O is the capacitance per unit area due to the oxide:

$$C_O = \varepsilon_o \varepsilon_{ox}/t$$

where t is the thickness of the oxide. C_T is the series combination of the oxide capacitance and the capacitance due to the depletion layer formed under the oxide:

$$1/C_T = 1/C_O + 1/C_S$$

where C_S is the capacitance per unit area of the depletion layer W_{max} deep

$$C_S = \varepsilon_o \varepsilon_s / W_{max} \; ; \; \varepsilon_s \text{ for silicon} = 12.$$

For an n-type substrate (p-channel) the threshold voltage V_T is given by:

$$V_T = (\phi_{ms} - 2\phi_F)/q - (Q_{SS} + Q_b)/C_o$$

where:

$\phi_{ms} = \phi_m - (\chi_S + E_g/2 - \phi_F)$ n-type substrate

$\phi_F = (kT/q)\ln(N_b/n_i)$, N_b = substrate doping level

$Q_b = qN_bW_{max}$

Q_{SS} = total lumped excess surface states charge density

ϕ_m = 4.25eV for aluminum

χ_S = 4.02eV for silicon

E_g = 1.1eV for silicon

$n_i = 1.5\text{x}10^{10}\text{cm}^{-3}$ at room temperature for silicon

Note that by measuring the C-V curves for our MOS capacitors we can obtain the threshold voltage, and from this estimate the total excess charge density in our oxides. This is process dependent, so this measurement is an important way of evaluating the quality of our grown oxides.

Archive only: Boonton C-V Tracer: **NOTE THIS SYSTEM IS NO LONGER IN USE!!**

Capacitance-voltage measurements in our laboratory are done on a Materials Development Corp. MDC CBAX unit (see p.M-7 for machine control lay-out). The unit consists of:

1) a Boonton 72A Capacitance Meter
2) a Hewlett-Packard 7035B x-y plotter
3) a MDC C-V interface and ramp generator.

The C-V meter supplies a 15mV RMS capacitance measuring signal at 1MHz, while the interface unit ramp generator provides the following dc bias capabilities:

1) maximum ± 150 V bias, adjustable via a ten-turn potentiometer
2) sweep over voltage range set above, at a rate that is adjustable from 0.1V/sec to 10V/sec via a ten-turn potentiometer
3) bias can be sweep from + to -, - to +, or held at any value in the sweep range.

Power-up Procedure and Initial Set-up

1. Turn the AC power switch on the Boonton meter ON; this will also power up the MDC bias supply.

2. Set the front panel controls as follows:
   a) Function: Zero
   b) Sweep Vernier: 10.0
   c) Positive Limit Vernier: fully counter-clockwise (i.e. zero)
   d) Negative Limit Vernier: fully counter-clockwise (i.e. zero)
   e) Sweep: 1 V/sec
   f) Meter Range Switch: 15 V
   g) Right side switches:
      i) Calibrate/Operate: calibrate
      ii) C-V/N-W: C-V

3. On the x-y plotter:
   a) select Pen-Up
   b) AC Power on
   c) set x & y sensitivities to 0.1 V/in
   d) insert graph paper, turn Chart Hold on
   e) turn Servo on

4. Zero the Capacitance Meter:
   With the sample on the probe station and all cables connected, place the probe tip just above the surface of the device to be tested. Select the 3pF range on the Boonton, and **use the Zero Control to set the meter to zero.**

5. Set Capacitance Meter range to 3000pF; carefully lower probe tip onto sample.

6. Set desired + and - limits:
    a) set Function switch to appropriate Set (either +set or -set)
    b) slowly turn the Limit vernier to increase the bias to the desired maximum value (usual in the 10 to 15 V range for MOS capacitor and diode measurements)
    c) re-adjust Capacitance Meter range as necessary.

7. Adjust x-y plotter range to allow full C-V curve to fit graph paper.

8. For sweep from Negative Limit to Positive Limit: select +SWEEP Function.
   For sweep from Positive Limit to Negative Limit: select -SWEEP Function.

9. When C-V measurements are completed, **set Function to ZERO before raising probe tip from device under test!**

10. Power off system when done.

OP-N: Junction Depth Measurements

filename: JUNCTD

The determination of junction depth is an important aspect of semiconductor process evaluation. In our lab the junction is a result of the pre-dep and drive-in processes performed at high temperature. Although there are a variety of models that can be used to estimate the distance over which the impurities diffuse, and thus determine junction depth, there are also many severe assumptions that must be made to apply the models. It is always desirable to actually measure the junction depths; however, when considering that the distances to be measured are only about a micron, and that impurity concentrations to be sensed are perhaps only 10^{-8} of the semiconductor atomic density, such measurement presents a non-trivial challenge.

Fortunately, there is a relatively simple technique for junction depth measurement which makes use of a mechanical grinding process combined with differential chemical staining. The objective of the grinding process is to convert very shallow depth information into large lateral variations. Figure 1 below illustrates the geometrical advantage of grinding a groove into the surface of our doped chip. W_2 and W_1 are measured with a microscope (see OP-S, p. 190 for line width measurements).

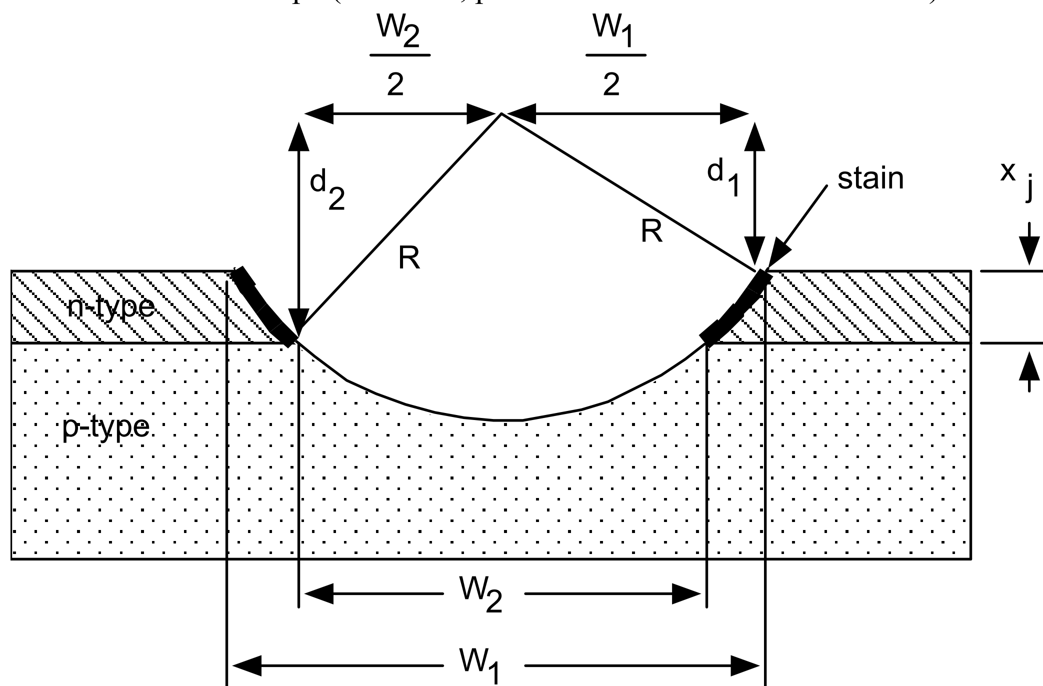


Figure 37: Junction sectioning geometry.

Because of the large radius of the grinding tool, the lateral dimensions which are exposed are quite large. If a chemical stain (consisting of metal salts in an electrolyte) is applied to the exposed p-n junction, and then exposed to light, a preferential staining of the n-type regions will occur. An optical microscope (see OP-S p. 190 for instructions on the

use of our line width measuring equipment) can then be used to measure the two dimensions W_1 and W_2. Applying some geometry yields the relationship:

$$x_j = d_2 - d_1 = \sqrt{R^2 - \left(\frac{W_2}{2}\right)^2} - \sqrt{R^2 - \left(\frac{W_1}{2}\right)^2}$$

At present we use a PHILTEC 2015 Sectioner, with a tool radius R of 19,050 µm. In addition, Philtec has determined that a slight correction factor is necessary to match the results with ASTM standards. Thus, the formula used to determine junction depth is given by:

$$x_j\ (\mu m) = \sqrt{(19{,}050\ \mu m)^2 - \left(\frac{W_2\ (\mu m)}{2} - 9.924\right)^2} - \sqrt{(19{,}050\ \mu m)^2 - \left(\frac{W_1\ (\mu m)}{2} - 9.924\right)^2}$$

Operating Procedure

The basic operation of the Philtec Sectioner is quite simple. The main parameter that must be determined in our application is the sectioning time (see step 8 below). This time is dependent mainly on the type of diamond grinding paste used to dress the spindle (see section 4 below). The operating procedure given on the next pages is a copy of the Philtec instruction sheet. We will give an update on operation in the lab during which you actually perform the junction grooving.

As of Aug. 25, 1988 the following parameters produced acceptable results:

Sectioning time: 10 sec

Staining time: 10 sec

Illumination source: Stereozoom 7 scope, 5X, illuminator power supply setting 3

OP-O: Mask Alignment and the Microtech Mask Aligners

filename: MCROTCH

In order to fabricate IC devices it is necessary to accurately align patterns already present on a chip to the next pattern in the lithography sequence. The instrument used for this purpose is called a Mask Aligner, for the obvious reason that it aligns a mask to a pattern already on the chip; it also exposes this pattern in the photoresist after the alignment is complete. We use a manual alignment procedure, which is probably the most challenging and time-consuming step in our lab processing. The purpose of this OP is to familiarize you with the operation of our Microtech Mask Aligners, and to provide some tips on how to perform your alignments. Fortunately, we have upgraded these aligners significantly, and you should now find them somewhat easier to use.

A mask aligner must serve two purposes: first, it must provide a means to align a pattern on a chip to the pattern on a mask; and second, it must then expose this pattern. Our aligners use a rigid frame which holds the mask that moves (ideally) only in the vertical direction (z-axis), and a separate wafer chuck which holds the chip that can rotate about the z-axis (θ axis)and move in the horizontal plane (x-y plane). A very small gap is set between the chip and mask, and a microscope is used to examine the mask pattern and alignment marks on the chip simultaneously. The x-y and θ adjustments are then used to bring the two patterns into alignment. After alignment, the mask and chip are pressed together by using a vacuum to apply about 14 pounds per square inch of pressure to them. A timer is used to open a shutter, allowing a UV lamp to expose the photoresist.

The most difficult step in this process is the alignment of chip to mask. In industry special alignment marks and automated pattern recognition are used to perform this step. We must perform the process manually, however. The technique that will allow you to achieve precise alignment in a relatively short time is called split-field alignment. The mask aligner microscope actually has two objective lenses, side-by-side. When in the split-field mode, the image you see is split in half, with the left image corresponding to one location on the chip, and the right half corresponding to another location about one inch away. By adjusting the separation of the objective lenses you will be able to see the same type of alignment marks at two widely separated points on the chip. When the θ and x-y translators are used to move the chip it will be very easy to tell when the whole chip is aligned, since you can see both of these areas. With this technique we can achieve alignment tolerances of better than ±5 μm, which is adequate for our minimum critical dimension of about 20 μm.

Tips on Using the Microtech Mask Aligners

One of the most important factors in aligning is maintaining the smallest possible separation between mask and substrate during alignment. With these aligners the best technique is to initially place the mask and chip in hard vacuum contact. You should then focus the microscope on the chip and mask patterns. While watching through the microscope, slowly pull out the z-axis separation lever; as the mask rises away from the chip it will go slightly out of focus. You should then use the x-y translation micrometers to check for adequate separation: if there is not enough gap to completely separate mask and chip, when you try to move the chip the mask will be dragged along with it, which is clearly visible through the microscope. There is no substitute for practice in this process, so be patient until you develop a feeling for how the machines operate.

Please be careful while using the mask aligners: it is relatively easy to scratch both masks and your chips if you use the aligners improperly.

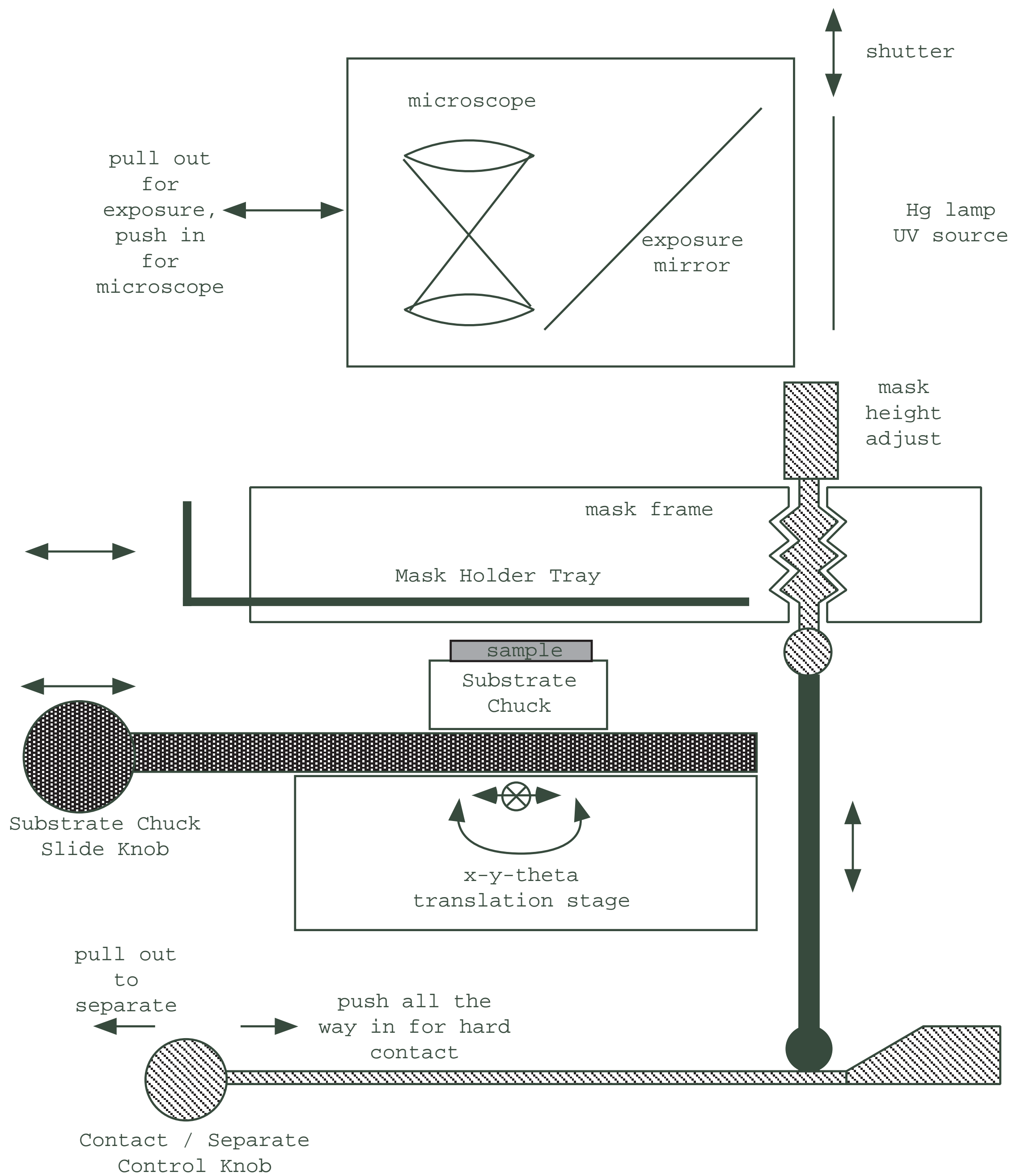


Figure 38: Schematic diagram of the Microtech Mask Aligner

Mask Aligner Operating Procedure

1. Start the U.V. lamp:

   Turn the U.V. Lamp Power Supply on, and then depress the START BUTTON for approximately 1 sec. The lamp should start immediately. Allow a MINIMUM 15 MINUTE WARM-UP PERIOD.

Step 1 should normally be performed by the Lab TA before you arrive.

2. Turn the Aligner ON. Pull the Contact/Separate Control Knob all the way **OUT** (full separation position between substrate and mask).

3. Load the Mask:
   a) Slide the Substrate Chuck all the way forward by pulling on the Substrate Chuck Slide Knob.
   b) Slide out the Mask-Holder Tray.
   c) Load mask, pattern side **down**.
   d) Slide Mask-Holder Tray back into the Mask Frame.

4. Load the Substrate:
   a) The Substrate Chuck should still be out from step 3a.
   b) Place your sample on the center of the chuck; orient it so it will be roughly aligned with the mask pattern.
   c) Turn the Substrate Vacuum ON.
   d) Slide the Substrate Chuck all the way back under the Mask Frame.

5. Check for Coarse Alignment:
   Check the rotational alignment visually; if necessary, slide chuck back out (step 3a) and rotate the chuck manually.

6. Planarize Substrate to Mask:
   a) Turn the Substrate Vacuum OFF.
   b) Slowly push the Contact/Separate Control Knob back in; the Mask Frame should drop down towards the substrate, rapidly at first, and then more gradually.
   c) When the Contact/Separate Control Knob is all the way in (full vacuum contact position) the substrate and mask should be in hard vacuum contact. Sample is now planarized.
   d) Turn the Substrate Vacuum back ON.

7. Align:
   a) To move the chip relative to the mask the Contact/Separate Control Knob <u>MUST</u> be in the <u>SEPARATE</u>

Position: from fully-in position (hard vacuum contact) slowly pull the knob toward you. The Mask Frame will rise slightly, allowing free motion of the substrate stage. Watch for it through microscope, mask image will blur.

b) Use the rotation micrometer to achieve θ-axis alignment; check opposite corners of your chip with the microscope to determine θ-axis.

c) Use the Fine Translation Micrometers to align in x-y plane. Check several locations on the wafer with microscope.

USE OF SPLIT-FIELD ALIGNMENT:

Put microscope in split-field mode; the image seen through the microscope should now appear cut in half, the left side corresponds to the right microscope objective lens, and the right side of the image to the left objective. Locate an alignment mark in one field; turn the Objective Lens Separation Adjustment (located to the right of the two objective lenses) until both fields show the same alignment mark. It should now be possible to simultaneously perform θ and x-y alignment.

d) Push the Contact/Separate Control Knob all the way in (hard contact position).

e) Check alignment again with microscope; if necessary repeat steps a-d. When alignment is satisfactory, make sure the Contact/Separate Control is in the contact position.

8. Expose:

a) Pull the microscope head all the way forward to bring the mirror over the sample.

b) Set timer for desired exposure time.

c) Press Expose button.

9. Remove your sample:

a) After the expose cycle is complete, pull Contact/Separate Control all the way out to the fully separated position.

b) Slide the Substrate Chuck all the way out, turn the substrate vacuum off, and remove your sample.

10. Remove mask:

a) The substrate chuck should still be out from step 9b.

b) Slide out the Mask-Holder Tray. Carefully remove the mask, and replace it in its storage box.

c) Slide the Mask-Holder Tray back in; slide the Substrate Chuck back in. Turn the Mask Aligner Power switch off.

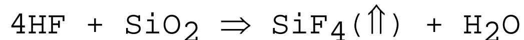
DO <u>NOT</u> TURN THE UV LAMP POWER SUPPLY OFF.

OP-P: Hydrofluoric Acid Etching

filename: HFETCH

As discussed in the Safety section of the Lab Manual Introduction (p. 10), hydrofluoric (HF) acid can be very dangerous if mishandled. It is, however, a very useful etch for silicon dioxide, SiO_2. It has a number of advantages over other techniques when patterning SiO_2 over silicon: it has very high selectivity over silicon, i.e. the etch rate of SiO_2 in HF is much greater than the etch rate of Si; HF can easily be masked by photoresist; the etch rate is quite repeatable, and remains constant even after a large number of samples have been etched; and the equipment required to etch with HF is relatively simple and inexpensive.

The actual etchant we use is a solution of concentrated HF (49%), water, and a buffering salt, NH_4F, in about the ratio 1:6:4. This solution is referred to as buffered HF, or BHF. The buffering agent is added to maintain a constant pH as the HF is consumed in its reaction with SiO_2:



$$4HF + SiO_2 \Rightarrow SiF_4(\Uparrow) + H_2O$$

Since the etch rate is a function of the solution pH, BHF has a much more controlled etch rate (about 1000Å/min at room temperature) over the life of the etchant.

In order to safely handle our BHF etching a special etch station has been designed for our lab. Figure 39 shows a top view of our station, and Figure 1b shows the plumbing arrangement for the station.

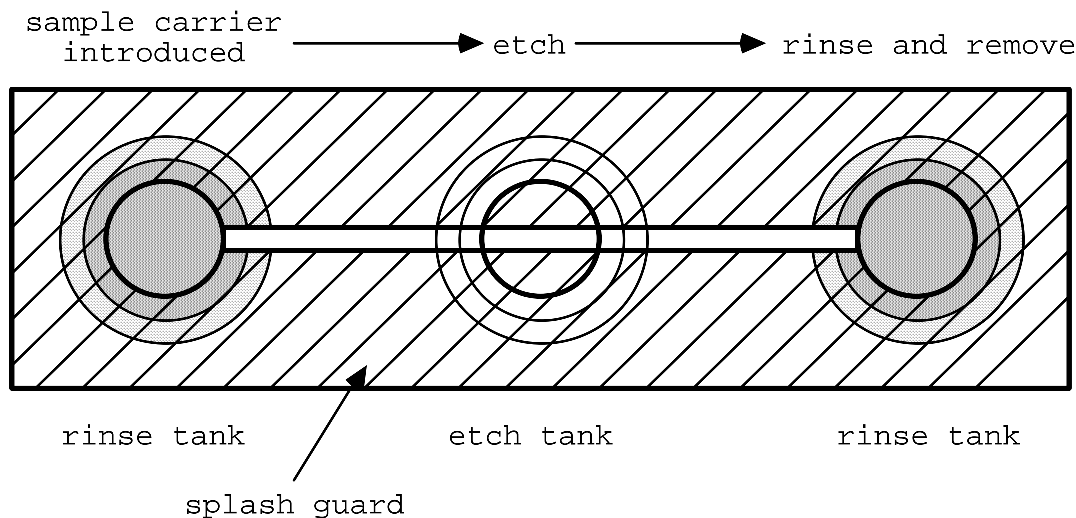


Figure 39: top view of BHF etch station.

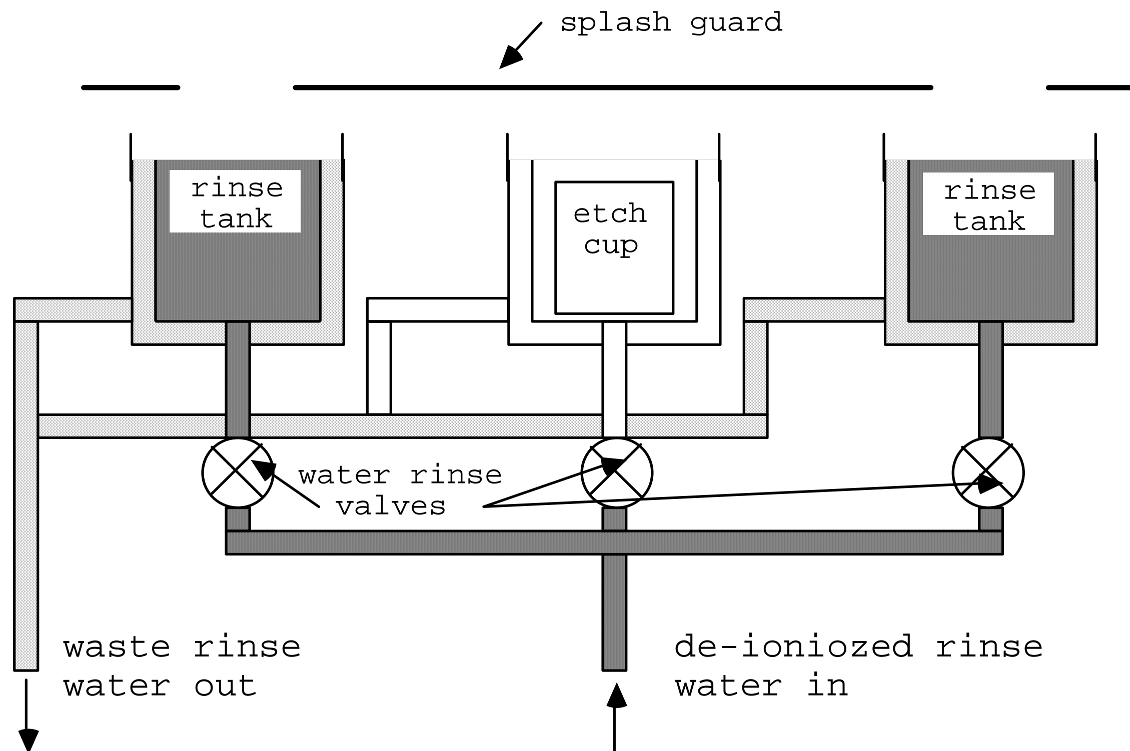


Figure 40: Plumbing diagram for BHF etch station.

Our system consists of three dump-type rinse tanks installed in the work top of a fume hood. Each tank has a DI water supply, controlled by a water valve in front of the station. The tanks are made up of an inner cup to which the water is supplied; this cup fills until it overflows into the outer portion of the dump tank, which is connected to an acid drain. We use the first tank on the left for an introduction rinse to wet the samples to be etched; the middle tank holds a teflon etchant cup, which actually contains the BHF; the last tank on the right is used for a water rinse to remove the BHF.

In addition to the dump tanks we use a special splash guard to prevent accidental acid spills. This consists of a plexiglass cover with large openings above the two end rinse tanks. These openings are connected by a narrow slot which passes over the etch cup (see Fig. 1a). To begin an etch step, the substrates to be etched are placed in a teflon chip carrier with a long handle attached. This carrier is then lowered into DI water through the opening over the first rinse tank. After wetting the samples the carrier is raised and transferred to the etch cup. The slot in the splash guard is large enough to allow the handle to pass through, but is not large enough to allow the chip carrier to be removed. When the etch is finished, the carrier is raised clear of the etch cup, and is transferred to the final rinse tank. After a suitable rinse time the chip carrier can be removed through the large hole in the splash guard over this tank. We have found this system will prevent HF splashing in almost all circumstances.

BHF ETCH PROCEDURE

1. Place samples to be etched in the teflon carriers located on the bench to the left of the etch station. Make sure a long teflon handle is inserted into the carrier.

2. Turn on the water supply to the two end dump tanks; make sure the two regular water faucets are on and running into the sink.

3. **Put on a pair of acid resistant gloves (the green gloves next to the hood) and a pair of protective eye glasses. DO NOT LEAVE THE HOOD AREA ONCE YOU START THIS PROCEDURE!**

4. Carefully lower the sample carrier through the splash guard into the left-most rinse tank. Leave immersed for approximately 15 sec.

5. Lift the carrier out of the rinse water, and carefully shake off any excess water. Now slide the handle down the slot to position the wafer carrier over the BHF cup. **Very carefully lower the carrier into the cup.** Be sure not to splash any HF out of the cup.

6. Use the running water in the sink to thoroughly rinse your gloves. DO NOT REMOVE YOUR GLOVED HANDS FROM THE HOOD DURING THE ETCH TIME: REMAIN AT THE ETCH STATION UNTIL THE PROCESS IS COMPLETE.

7. At the end of the desired etch time carefully lift the carrier out of the etch cup, and gently shake any drops of BHF off the carrier back into the cup. Now transfer to and immerse the carrier in the right side rinse tank. RINSE FOR AT LEAST 1 MIN.

8. Use the HP H_2O dispenser to rinse the handle of the carrier, as well as your gloves. MAKE SURE ANY SURFACES THAT MAY HAVE BEEN CONTAMINATED WITH HF ARE RINSED IN WATER.

9. Remove the carrier from the rinse tank, and finish with at least two HP H_2O rinses in the teflon beaker in front of the etch station.

10. After completing the rinse remove the carrier from the hood, and transfer to the wafer spinner. Go back to the hood and thoroughly rinse your gloves in running water in the sink. Remove acid gloves, leaving them at the hood.

11. Remove your clean gloves, throw them away, and go to the large sink in the Litho Room for final wash up. Be careful to rinse your hands and arms thoroughly, especially under the fingernails.

OP-Q: Tektronix Curve Tracer

filename: TEKCT

This section is intended as an introduction to the use of our Tektronix Curve Tracer. This is a very versatile instrument, capable of both two-and three-terminal measurements. Section I describes the operation of the curve tracer for two-terminal measurements (i.e. diode, capacitor, or resistor characteristics) and Section II for three-terminal measurements (bi-polar transistor or MOSFET characteristics).

Section I: Two-Terminal Devices

In this mode the device-under-test (DUT) is connected between the C and E terminals of the curve tracer. The Collector Supply section (see Figure 41) will then apply a voltage at the C terminal, Vc. Note the Max Peak Volts selector and its concentric knob, the Series Resistor selector. The Max Peak Volts selects the maximum voltage that can be applied to the DUT, while the Variable Collector % knob is a multiplier of this peak voltage, determining the actual max voltage applied. The Series Resistor selects the value of series resistance between the voltage source and the DUT, serving as a current limiter. The Collector Supply Polarity selector allows you to choose between a plus and minus Vc sweep, plus only sweep, minus only sweep, and DC applied voltage (either minus or plus) controlled by the Variable Collector % knob and the Max Peak Volts selector.

The display will now show the voltage across the C and E terminals (and therefore across the DUT) on its horizontal axis, scale set by the Horizontal section; and the current through the DUT on the vertical axis, scale set by the Vertical section. Also note directly above the Vertical current selector the Terminal Selector. This setting allows various Base and Emitter or Collector settings. We usually use the Emitter Grounded selections. For the Base setting, see section II.

Warnings:

1) Always make sure the Variable Collector % knob is set at 0% before making any electrical connections, or changing the Max Peak Volts or Series Resistor.

2) Normally start with Max Peak Volts set low (25 Volts) and the Series Resistor set high (> 10K). After making electrical connections, slowly increase the Variable Collector % setting until you obtain a curve trace. Then, if necessary increase Max Peak Volts and reset the Series Resistor.

3) When measuring reverse characteristics of diodes, the large diode capacitance may make the curve trace appear as a loop. To make accurate measurements, switch Collector Supply Polarity to appropriate DC setting, and sweep the trace manually at a slow rate. You can use the storage scope settings to record the trace.

4) The curve tracer can produce HAZARDOUS HIGH VOLTAGES. You will normally only need large voltages for diode breakdown measurements, but these may well be greater that 100

Volts. BE VERY CAREFUL NOT TO TOUCH ANY OF THE PROBES OR THE INSULATED SUBSTRATE CHUCK WHEN HIGH VOLTAGES ARE APPLIED.

Section II: Three-Terminal Devices

The display and E and C controls behave in an identical way to that described in Section I, but we now have an additional variable, the Base setting. This curve tracer can either inject current (for bipolar measurements) or apply voltage (for FET measurements), and can step this parameter from its maximum value to lower values in fixed steps, in order to produce the whole family of curves characteizing the DUT. The following is a description of the Step Generator secton which controls the base parameter:

Step Family: determines whether only one value of the base term is generated, or whether multiple terms are.

Step Rate: sets rate at which base term is stepped.

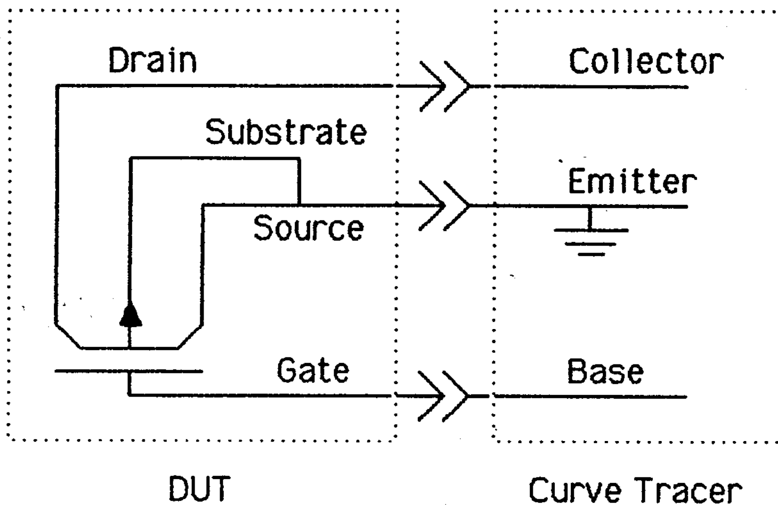
Polarity: sets the step voltage polarity of base term relative to ground; for the voltage mode, applies same polarity as collector sweep volts relative to ground in Normal mode, opposite in Invert mode.

Step/Offset Ampl: determines whether current or voltage is applied to B terminal. In conjunction with the Offset Multi control, sets the maximum current/voltage applied. Also sets the size of the steps used for changing the B parameter when Step Family is set to Rep position.
Note: the X.1 button decreases the step size by a factor of 10, BUT DOES NOT DECREASE THE MAX BASE PARAMETER: see Offset Multi.

Number of Steps: sets number of steps applied to B parameter.

Offset Multi: multiplies (0 to 10x) normal step amplitude set by step/offset Ampl. control to determine the starting value of the base parameter. Note this value is set by multiplying the Offset Multi setting by the normal (i.e., the value the dial pointer indicates, regardless of whether the X.1 button is depressed) Step/Offset Ampl setting. Also note this dial is a vernier tenturn indicator, and reads to three significant figures.

Measuring Procedure for MOSFETs
Normal circuit configuration:



p-channel (n-type substrate):
The following Collector Settings allow us to apply a voltage VDS of up to negative 25 Volts to the drain:

Variable Collector: 0%
Max Peak Volts: 25
Series Resistor: 2 k
Collector Supply Polarity to -

Now we must set up to apply negative gate voltages from the Step/Offset amplifier:

Step/Offset Ampli: 1V, Step X.1 button out (i.e. on)

Step Family: Rep on (in)
Step Rate: Norm on (in)

Step/Offset Polarity: inverted (out)
(this adds positive gate bias steps to the starting value set by the Offset Multi dial)

Number of Steps: 1 (fully counter-clockwise)

Offset Multi: 0
Zero button below Offset Multi: offset (out)
Aid button: oppose (out)

These settings allow us to apply a series of negative gate voltages for the drain-source IV curves. The first gate voltage is fixed by the offset multiplier setting times the normal step/offset

amplitude: i.e., (0 to 10) x 1 Volt, where we have initially set the multiplier dial to zero (0). The gate voltage steps are added to this max in steps of +0.1 volt (since the X.1 button is active). We have initially set the number of steps to one.

We now would adjust the horizontal and vertical scales, along with the position of the zero-zero dot, to obtain the desired display:

Horizontal Collector Volts: 1 V/div
Filter: normal (in)
Mag buttons on horizontal and vertical positions: off (in)
Vertical Collector current: 0.1mA/div
Terminal Selector: Emitter grounded, Step generator

With the offset multiplier set to zero, for an enhancement mode MOSFET, as the collector voltage % is increased no current should flow. Set this control for approximately 5 V collector voltage. Now SLOWLY increase the offset multiplyer to apply a negative voltage (negative because the collector supply polarity is -)to the gate; when the threshold voltage is reached the MOSFET will turn on, and current will flow. Once the maximum current desired is reached by continuing to increase the offset multiplyer, increase the number of steps control to obtain the complete family of curves.

n-Channel Settings:

For an enhancement mode n-channel device we need to apply positive voltage to the drain, and a positive gate bias to turn the device on:

The following Collector Settings allow us to apply a voltage VDS of up to positive 25 Volts to the drain:
Variable Collector: 0%
Max Peak Volts: 25
Series Resistor: 2 k
Collector Supply Polarity to +

Now we must set up to apply positive gate voltages from the Step/Offset amplifier:
Step/Offset Ampli: 1V, Step X.1 button out (i.e. on)
Step Family: Rep on (in)
Step Rate: Norm on (in)
Step/Offset Polarity: inverted (out)
(this adds negative gate bias steps to the starting value set by the Offset Multi dial)
Number of Steps: 1 (fully counter-clockwise)
Offset Multi: 0
Zero button below Offset Multi: offset (out)
Aid button: oppose (out)

These settings allow us to apply a series of positive gate voltages for the drain-source IV curves. The first gate voltage is fixed by the offset multiplier setting times the normal step/offset amplitude: i.e., (0 to 10) x 1 Volt, where we have initially set the multiplier dial to zero (0). The gate voltage steps are added from this max in steps of -0.1 V (since the X.1 button is active). We have initially set the number of steps to one.

We now would adjust the horizontal and vertical scales, along with the position of the zero-zero dot, to obtain the desired display:

Horizontal Collector Volts: 1 V/div
Filter: normal (in)
Mag buttons on horizontal and vertical positions: off (in)
Vertical Collector current: 0.1mA/div
Terminal Selector: Emitter grounded, Step generator

With the offset multiplier set to zero, for an enhancement mode MOSFET, as the collector voltage % is increased no current should flow. Set this control for approximately 5 V collector voltage. Now SLOWLY increase the offset multiplyer to apply a positive voltage (positive because the collector supply polarity is +) to the gate; when the threshold voltage is reached the MOSFET will turn on, and current will flow. Once the maximum current desired is reached by continuing to increase the offset multiplyer, increase the number of steps control to obtain the complete family of curves.

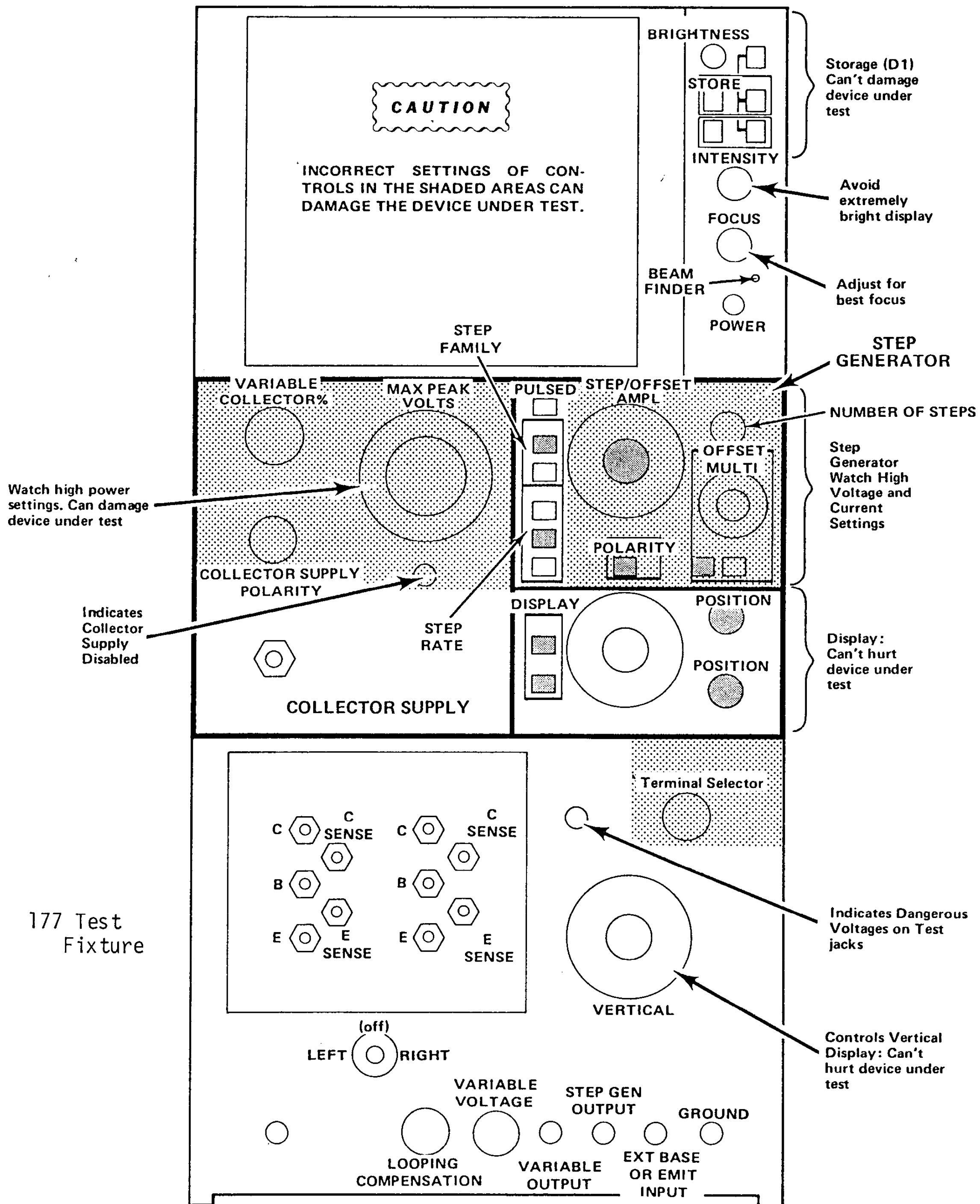


Figure 41: Front panel of Tektronix 577 Curve Tracer

Table 16: FUNCTIONS OF CONTROLS AND CONNECTORS for Tektronix Model 577 Curve Tracer

Display Units	
INTENSITY	Controls non-stored display bright-ness.
FOCUS	Provides adjustment to obtain a well-defined display.
POWER	Used to turn instrument power on and off.
BEAM FINDER	Brings beam on-screen; limits dis-play to the area inside the graticule.
TRACE ROTATION(rear panel)	Permits alignment of the trace to the horizontal graticule lines.

Dl Only (Storage)	
UPPER and LOWER STORE	Selects storage or non-storage operation.
UPPER and LOWER ERASE	Complementary cancelling switches select the screen to be erased. Both buttons pushed selects both screens.
BRIGHTNESS	Provides continuously variable flood-gun current duty cycle from about 10% to 100% (when the collector sweep is turned down or disabled), permitting extended retention of displayed information. Also controls the degree of spot dimming vvhen the collector sweep is turned down or disabled.

Collector Sweep	
COLLECTOR SUPPLY POLARITY (Automatic trace position with polarity change is maintained in all switch positions.)	*NOTE: The normal step generator polarity is positive-going in+DC, +, and AC, and negative going in - and -DC. Step generator polarity can be inverted by either the STEP/OFFSET POLARITY switch or the test fixture Terminal Selector switching.*
+DC	Applies positive DC to the collector terminals of the test fixture. Useful when the device under test exhibits excessive looping in sweep modes or when a DC supply is desired.
+	Applies positive sweeping voltage at 2X line rate to

	collector terminals of the test fixture. When the step generator is in PULSED mode, the supply is automatically switched to DC unless the operator desires to maintain the sweep voltage (see PULSED 300 μs).
AC	Applies AC at power line frequency to the test fixture collector terminals (use SLOW step rate).
-	Applies negative sweeping voltage at 2X line rate to the test fixture collector terminals. When the step generator is in PULSED mode, the supply is automatically switched to DC unless the operator desires to maintain the sweep voltage (see PULSED 300 μs).
-DC	Applies negative DC to the test fixture collector terminals. Useful when the device under test exhibits excessive looping in sweep mode, or when a DC supply is desired.
VARIABLE COLLECTOR %	Provides uncalibrated, continuously variable control of collector supply amplitude from 0% to 100% of the voltage selected with the MAX PEAK VOLTS switch.
MAX PEAK VOLTS Switch	Selects one of five collector supply voltages.
SERIES RESISTORS and PEAK POWER WATTS Switches	
	Fourteen resistor values coupled to the MAX PEAK VOLTS switch to maintain one of six labeled peak-power limits. The SERIES RESISTORS and PEAK POWER WATTS switch pulls out to unlock from the MAX PEAK VOLTS switch to change the power setting. Lower power settings are available on all except the highest voltage range.
	The maximum peak power indicated by the MAX PEAK POWER WATTS can be delivered only if the VARIABLE COLLECTOR % control is set to 100 and the impedance of the "device under test" exactly matches the series resistor selected with the SERIES RESISTORS switch.
	The MAX PEAK POWER WATTS switch usually can be safely set above the maximum power rating of the device under test.

COLLECTORSUPPLY DISABLED(Indicator lamp)	The yellow lamp is lighted when the test fixture protective lid is not closed over the test terminals (unless modified by a wiring option in the test fixture) whenever the MAX PEAK VOLTS switch is in the 100 V, 400 V, or 1600 V position. The yellow lamp pulses (on and off) if the vertical current limiting circuit disables the collector sweep (when the device under test current causes 2.5 times full-screen deflection for a short time).
COLLECTOR SUPPLY CIRCUIT BREAKER	Protects the collector supply from excessive power dissipation. Push to reset breaker after circuit interruption.

Step Generator	
PULSED 300 μs (Pushbutton)	With the 300 us pushbutton in the in position (Pulsed mode), the step. generator produces 300 us wide pulses at 1 or 2 times line frequency, depending on the Step Rate selected. For these two step rates (SLOW and NORM) the collector supply is automatically switched to DC unless the COLLECTOR SUPPLY POLARITY is in AC. If the FAST Step Rate is selected, the generator step rate is twice the line frequency, but the collector supply is not switched.
STEP FAMILY	
REP	With this pushbutton in the "in" position, up to ten steps per family are generated, depending on the position of the NUMBER OF STEPS control. When the push-push button, STEP X.1, concentric with the STEP/OFFSET AMPL switch, is in the "out" position, the NUMBER OF STEPS control provides from about 1 to 95 steps.
SINGLE	Each time the SINGLE button is pressed, a single family is generated. Upon release, the step generator is turned off. Single family is useful for low-current, two terminal measurements.
SLOW (1X LINE Frequency)	When the SLOW pushbutton is in the "in" position, the generator stepping rate is at power line frequency.
NORM (2X LINE Frequency)	When the NORM pushbutton is in the "in" position, the generator stepping rate is twice the power line frequency.
FAST (4X LINE Frequency)	When the FAST pushbutton is in the "in" position, the

	generator stepping rate is four times the power line frequency.
	NOTE: Step transitions occur at the start of the collector supply sweep in SLOW and NORM modes. Transitions occur at both the start and the peak of the collector supply sweep in the FAST mode.
FAST and SLOW	When FAST and SLOW buttons are in the "in" position simultaneously, the generator stepping rate is twice the power line frequency, (NORM), but the step transitions occur at the peaks of the collector supply sweeps.
NUMBER OF STEPS	Continuously variable control selects the number of steps per display.
STEP/OFFSET AMPL	Selects from 21 current steps, from 50 nA/Step to 200 mA/Step, or six voltage steps, from .05 V/Step to 2 V/Step, in a 1-2-5 sequence.
STEP X.1	Push-push knob concentric with STEP/OFFSET AMPL knob. When this knob is released ("out" position), the Step Amplitude is reduced to .1X the previous amplitude and is indicated by the illuminated area of the STEP/OFFSET AMPL knob skirt. The OFFSET MULT range is not affected, resulting in small steps on large offset capability. The number of steps available changes (from the 1 to 10 range to approximatelv 1 to 95 steps), making the display appear as a ramp rather than discrete steps at the high rate.
STEP/OFFSET POLARITY	When the NORM pushbutton is in the "in" position, the step voltage is the same polarity as the collector sweep unless inverted by the test fixture. When the NORM button is in the "out" position, the step voltage is opposite the collector sweep polarity unless inverted by the test fixture. The Offset polarity is determined by the position of the OFFSET/AID/OPPOSE button.
OFFSET MULT	Multiturn control providing DC offset from 0 to 10 times the STEP/ OFFSET AMPL switch setting with the STEP X.1 knob in the "in" position, or 0 to 100 times the STEP/OFFSET AMPL setting with the STEP X.1 knob in the "out" position.
OFFSET	In the "out" position, the offset voltage is determined by

	the OFFSET MULT control. When the ZERO button is in the in position, offset is disabled.
OPPOSE	In the "in" position, the offset voltage aids the step generator signal. When the OPPOSE button is in the "out" position, the offset voltage opposes the step generator signal.

Horizontal	
HORIZ VOLTS/DIV(knob)	Selects from 12 calibrated collector deflection factors from .05 V/DIV to 200 V/DIV or from 6 calibrated base deflection factors from 50 mV/DIV to 2V/DIV with X10 HORIZ MAG PULL in the "in" position. With the X10 HORIZ MAG PULL in the "out" position, the deflection factors are 5 mV/ DIV to 20 V/DIV or 5 mV/DIV to .2 V/DIV. All steps follow a 1-2-5 sequence.
Horis POSITION(knob)	Provides uncalibrated horizontal positioning over at least +-10 graticule divisions.
X1O HORIZ MAG PULL	Pulling the Horiz POSITION knob to the "out" position provides ten times magnification of the horzontal display, extending the horizontal positioning to +- 100 divisions. Sensitivity change is indicated by a change in the area of illumination of the HORIZ VOLTS/DIV knob skirt.

Display	
DISPLAY INVERT	When the NORM pushbutton is in the "in" position, a normal display is presented. When the NORM button is in the out position, the display is inverted, both horizontally and vertically.
DISPLAY FILTER	Full vertical bandwidth is obtained with the NORM pushbutton in the in position. When the NORM pushbutton is in the "out" position, vertical bandwidth is limited to reduce noise on the trace. Band-width limit is useful in the most sensitive CURRENT/DIV positions, DC positions of the collector sweep, and with base steps turned off. When sweeping manually with filter in use, sweep very slowly.

Vertical	
Vertical POSITION(knob)	Provides uncalibrated vertical positioning over at least +-8

	divisions.
X1O VERT MAG PULL	Pulling the Vert POSITION knob to the "out" position provides ten times magnification of the vertical display, extending the vertical positioning to +-80 divisions. Sensitivity change is indicated by a change in the area of illumination of the VERTICAL SENSITIVITY (Test Fixture) knob skirt.

177 Test Fixture Terminal Selector	
EMITTER GROUNDED	
BASE TERM	
STEP GEN	Applies step generator output to the test fixture base connections.
OPEN (OR EXT)	Disconnects the test fixture base terminal from the step generator output and connects the base terminal to the front-panel EXT BASE OR EMIT INPUT connector.
SHORT	Disconnects the test fixture base terminal from the step generator output and grounds the base terminal.
BASE GROUNDED	
EMITTER TERM	
STEP GEN	Applies step generator output to the test fixture emitter terminal and inverts the step generator polarity.
OPEN (OR EXT)	Disconnects the emitter terminal from the step generator and connects the emitter terminal to the front-panel EXT BASE OR EMIT INPUT terminal.
	NOTE: In BASE-GROUNDED mode, the step generator signal at the front-panel STEP GEN OUT is inverted.
EMITTER-BASE BREAKDOWN	Grounds the test fixture base terminal and applies collector sweep voltage (only those supply voltages that are not interlocked) to the emitter terminal. The collector terminal is open in this mode.

VERTICAL SENSITIVITY (CURRENT/ DIV)	Selects from 26 calibrated vertical deflection factors from 2 nA/DIV to 2A/DIV with mainframe X10 VERT MAG PULL in the "in" position and .2 nA/DIV to 200 mA/DIV with the VERT MAG PULL in the "out" position. All steps follow a 1-2-5 sequence.
LEFT-RIGHT	Three-position toggle switch for applying test signal to either the left or right set of terminal connectors (center position disconnects the terminal connectors). The emitter terminals are connected together and to either ground, step generator, or collector, depending on the position of the Terminal Selector switch.
Interlock Defeat	In normal operation, collector sweep voltages that are controlled by the interlock are removed from the device under test if the protective cover is open. Pushing the Interlock Defeat button applies sweep voltage with the protective cover open, as long as the button is pressed.
LOOPING COMPENSATION	Permits compensation of the internal and adapter stray capacitance and for some "device under test" capacitance.
VARIABLE VOLTAGE, VARIABLE OUTPUT	Provides +12, 0-12 continuously variable voltage (referred to ground) to the VARIABLE OUT-PUT connector. Impedance is approximately 10 kohm.
STEP GEN OUTPUT Connector	Provides external access to the step generator output.
EXT BASE OR EMIT INPUT	Provides external access to the base or emitter terminals, depending on the position of the Terminal Selector switch. Also provides a means of connecting an external resistor between the step generator output and base of the device under test.
GROUND	External ground connection.

Table 17: Tektronix Curve Tracer gate Bias Polarity Table

Collector Supply Polarity	Step/Offset Polarity button	polarity of gate steps	AID button	Polarity of gate offset initial value
+	in (normal)	+	in (aid)	+
			out (oppose)	-
	out (invert)	-	in (aid)	-
			out (oppose)	+

<table>
<tr><td rowspan="4">-</td><td rowspan="2">in (normal)</td><td rowspan="2">-</td><td>in (aid)</td><td>-</td></tr>
<tr><td>out (oppose)</td><td>+</td></tr>
<tr><td rowspan="2">out (invert)</td><td rowspan="2">+</td><td>in (aid)</td><td>+</td></tr>
<tr><td>out (oppose)</td><td>-</td></tr>
</table>

Gate offset initial value is the magnitude of the first voltage applied. The actual applied gate bias is:

$V = Vo + nVs$

where Vo is the offset voltage, n is the step (0 to 100), and Vs is the step size. The signs of these voltages are determined by the table above.

OP-R: Optical Thin Film Measurement

filename: ELLIP_NEW

Interference-based measurement of semi-transparent thin film thickness

(Adapted from product literature Filmetrics F20 Thin Film Measurement System, copyright 1998 Filmetrics, Inc., San Diego, CA. The F20 measurement system in our lab was donated by Filmetrics through the generosity of Dr. Scott Chalmers.)

Introduction

Very thin layers of material that are deposited on the surface of another material (thin films) are extremely important to many technology-based industries. Thin films are widely used, for example, to provide passivation, insulating layers between conductors, diffusion barriers, and hardness coatings for scratch and wear resistance. The fabrication of integrated circuits consists primarily of the deposition and selective removal of a series of thin films.

Films typically used in thin-film applications range from a few atoms (<10Å or 0.001 μm) to 100 μm thick (the width of a human hair.) They can be formed by many different processes, including spin coating, vacuum evaporation, sputtering, vapor deposition, and dip coating.

To perform the functions for which they were designed, thin films must have the proper thickness, composition, roughness, and other characteristics important to the particular application. These characteristics must often be measured, both during and after thin-film fabrication.

The two main classes of thin-film measurement are optical and stylus based techniques. Stylus measurements measure thickness and roughness by monitoring the deflections of a fine-tipped stylus as it is dragged along the surface of the film. Stylus instruments are limited in speed and accuracy, and they require a "step" in the film to measure thickness. They are often the preferred method when measuring opaque films, such as metals.

Optical techniques determine thin-film characteristics by measuring how the films interact with light. Optical techniques can measure the thickness, roughness, and optical constants of a film. Optical constants describe how light propagates through and reflects from a material. Once known, optical constants may be related to other material parameters, such as composition and band gap.

Optical techniques are usually the preferred method for measuring thin films because they are accurate, nondestructive, and require little or no sample preparation. The two most common optical measurement types are spectral reflectance and ellipsometry Spectral reflectance measures the amount of light reflected from a thin film over a range of wavelengths, with the incident light normal (perpendicular) to the sample surface. Ellipsometry is similar, except that it measures reflectance at non-normal incidence and at two different polarizations. In general, spectral reflectance is much simpler and less expensive than ellipsometry, but it is restricted to measuring less complex structures.

n and k Definitions

Optical constants ***(n** and *k)* describe how light propagates through a film. In simple terms, the electromagnetic field that describes light traveling through a material at a fixed time is given by:

$$A\bullet \mathbf{cos}\left(n\frac{2\pi}{\lambda}x\right)\bullet \mathbf{exp}\left(-k\frac{2\pi}{\lambda}x\right),$$

where x is distance, lamda is the wavelength of light, and ***n*** and *k* are the film's refractive index and extinction coefficient, respectively The refractive index is defined as the ratio of the speed of light in a vacuum to the speed of light in the material. The extinction coefficient is a measure of how much light is absorbed in the material.

Single Interface

Reflection occurs whenever light crosses the interface between different materials. The fraction of light that is reflected by an interface is determined by the discontinuity in ***n*** and ***k*. .** For light reflected off of a material in air, $R=\frac{(n-1)^2+k^2}{(n+1)^2+k^2}$ .To see how spectral reflectance can be used to measure optical constants, consider the simple case of light reflected by a single nonabsorbing material (k=0). Then:

$$R=\left|\frac{n-1}{n+1}\right|^2$$

Clearly, ***n*** of the material can be determined from a measurement of R. In real materials, ***n*** varies with wavelength (that is to say, real materials exhibit dispersion), but since the reflectance is known at many wavelengths, ***n*** at each of thesewavelengths is also known, as shown here.

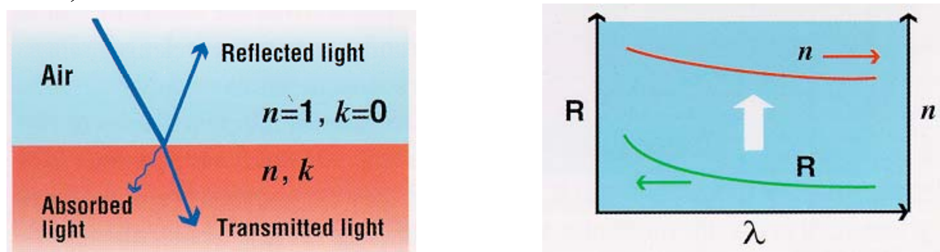


Figure 42: Single interface reflection.

Multiple Interfaces

Consider now a thin film on top of another material. In this case both the top and bottom of the film reflect light. The total amount of reflected light is the sum of these two individual reflections. Because of the wavelike nature of light, the reflections from the two interfaces may add together either constructively (intensities add) or destructively (intensities subtract), depending upon their phase relationship. Their phase relationship is determined by the difference in optical path lengths of the two reflections, which in turn is determined by thickness of the film, its optical constants, and the wavelength of the light. Reflections are in-phase and therefore add constructively when the light path is equal to one integral multiple of the wavelength of light. For light perpendicularly incident on a transparent film, this occurs when 2nd = iλ where ***d*** is the thickness of the film and i is an integer (the factor of two is due to the fact that the light passes through

the film twice.) Conversely, reflections are out of phase and add destructively when the light path is one half of a wavelength different from the in-phase condition, or when ***2nd*** = (i+1/2)λ. The qualitative aspects of these reflections may be combined into a single equation:

From this, we can see that

$$R \approx A + B\mathbf{cos}\left(\frac{2\pi}{\lambda}\,nd\right)$$

the reflectance of a thin film will vary periodically with 1/wavelength, which is illustrated below. Also, thicker films will exhibit a greater number of oscillations over a given wavelength range, while thinner films will exhibit fewer oscillations, and oftentimes only part of an oscillation, over the same range.

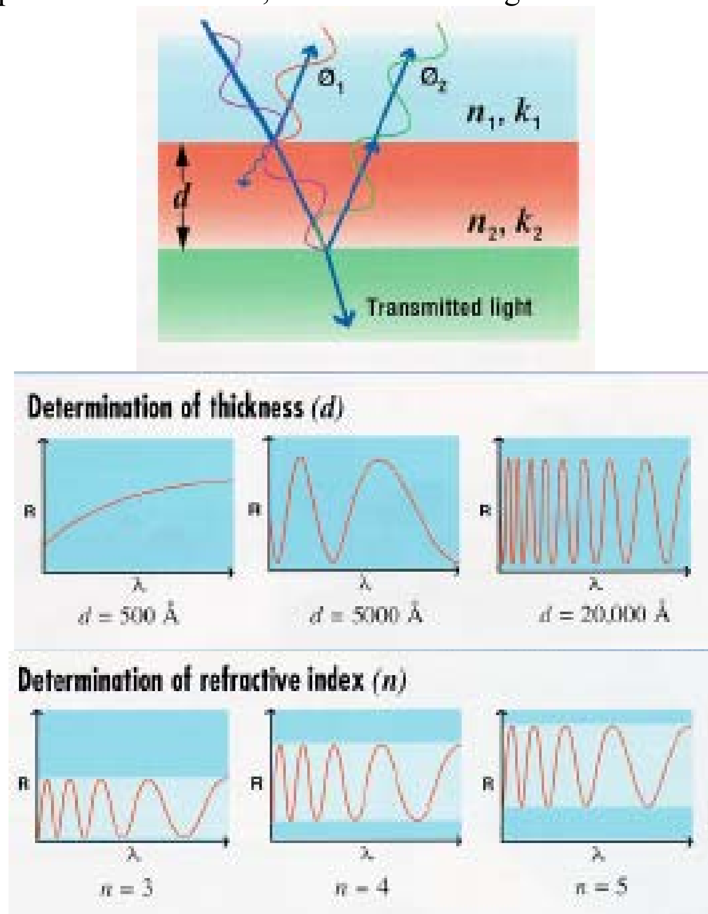


Figure 43: Multi-interface reflections.

Determining Film Properties from Spectral Reflectance

The amplitude and periodicity of the reflectance of a thin film is determined by the film's thickness optical constants, and other properties such as interface roughness. In cases where there is more than one interface, **it** is not possible to solve for film properties in closed form, nor is **it** possible to solve for ***n*** and ***k*** at each wavelength individually. In practice, mathematical models are used that describe ***n*** and ***k*** over a range of wavelengths using only a few adjustable parameters. A film's properties are determined by calculating reflectance spectra based on trial values of thickness and the ***n*** and ***k*** model parameters,

and then adjusting these values until the calculated reflectance matches the measured reflectance.

Models for *n* and *k*

There are many models for describing ***n*** and ***k*** as a function of wavelength. When choosing a model for a particular film, **it** is important that the model be able to accurately describe ***n*** and ***k*** over the wavelength range of interest using as few parameters as possible. In general, the optical constants of different classes of materials (e.g., dielectrics, semiconductors, metals, and amorphous materials) vary quite differently with wavelength, and require different models to describe them (see below.) Models for dielectrics (k=0) generally have three parameters, while nondielectrics generally have five or more parameters. Therefore, as an example, to model the two-layer structure shown below, a total of 18 adjustable parameters must be considered in the solution.

Number of Variables, Limitations of Spectroscopic Reflectance

Spectral reflectance can measure the thickness, roughness, and optical constants of a broad range of thin films. However, if there is less than one reflectance oscillation (ie. the film is very thin), there is less information available to determine the adjustable model parameters. Therefore, the number of film properties that may be determined decreases for very thin films. If one attempts to solve for too many parameters, a unique solution cannot be found; more than one possible combination of parameter values may result in a calculated reflectance that matches the measured reflectance.

An example of the reflectance from a very thin film, 50Å of SiO_2 on silicon is shown below, where it is compared to the reflectance from a bare silicon substrate. In this case, measuring the thickness, roughness, and ***n*** of the SiO_2 requires five parameters to be determined. Clearly, the change in the spectra caused by adding 50Å of SiO_2 does not require five parameters to describe, and a unique solution cannot be found unless some additional assumptions are made.

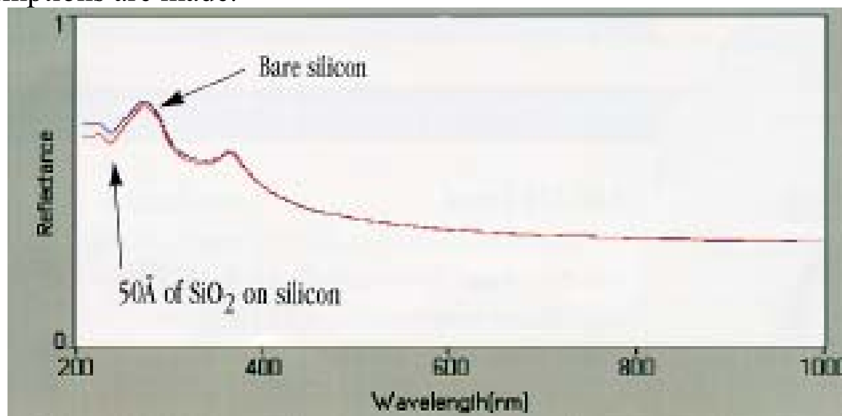


Figure 44: Sample reflectance trace.

Depending upon the film and the wavelength range of the measurement, the minimum single-film thickness that can be measured using spectral reflectance is in the 30Å to 300Å range. If one is trying to measure optical constants as well, the minimum thickness increases to between 100Å and 2000Å, unless minimal parameterization

models can used. When solving for the optical properties of more than one film, the minimum thicknesses are increased even further.

Spectroscopic Reflectance versus Ellipsometry

Given the restrictions listed above, spectral reflectance can be used to measure a large percentage of technologically important films. However, when films are too thin, too numerous, or too complicated to be measured with spectral reflectance, oftentimes they can be measured with the generally more powerful technique of spectroscopic ellipsometry By measuring reflectance at non-normal incidence (typically around 75° from normal) ellipsometry is more sensitive to very thin layers, and the two different polarization measurements provide twice as much information for analysis. To carry the idea even further, variable-angle ellipsometry can be used to take reflectance measurements at many different incidence angles, thereby increasing the amount of information available for analysis.

The following pages of this brochure describe spectral reflectance systems available from Filmetrics. If you are uncertain whether spectral reflectance or ellipsometry is appropriate for your film measurements, please call us to discuss your application. If spectral reflectance cannot satisfy your needs, we will be happy to refer you to a reputable source for ellipsometry

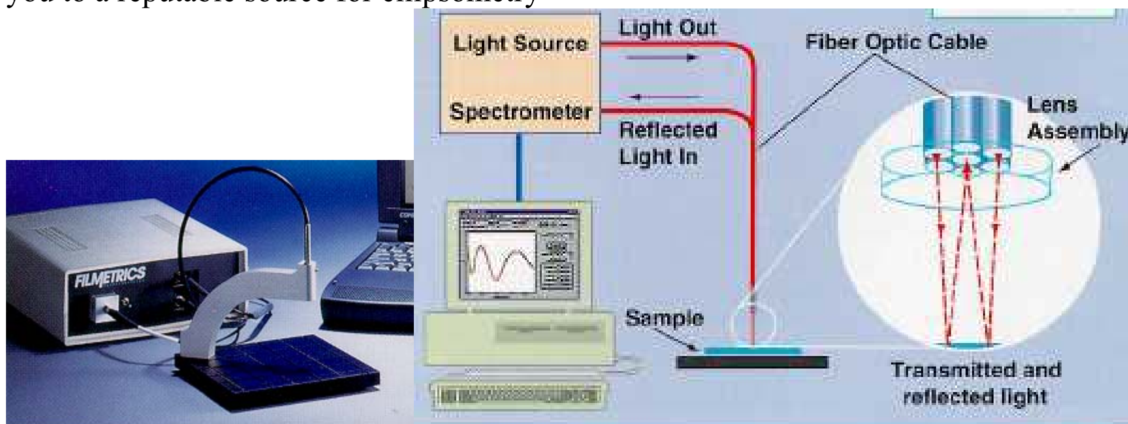


Figure 45: Filmetrics system.

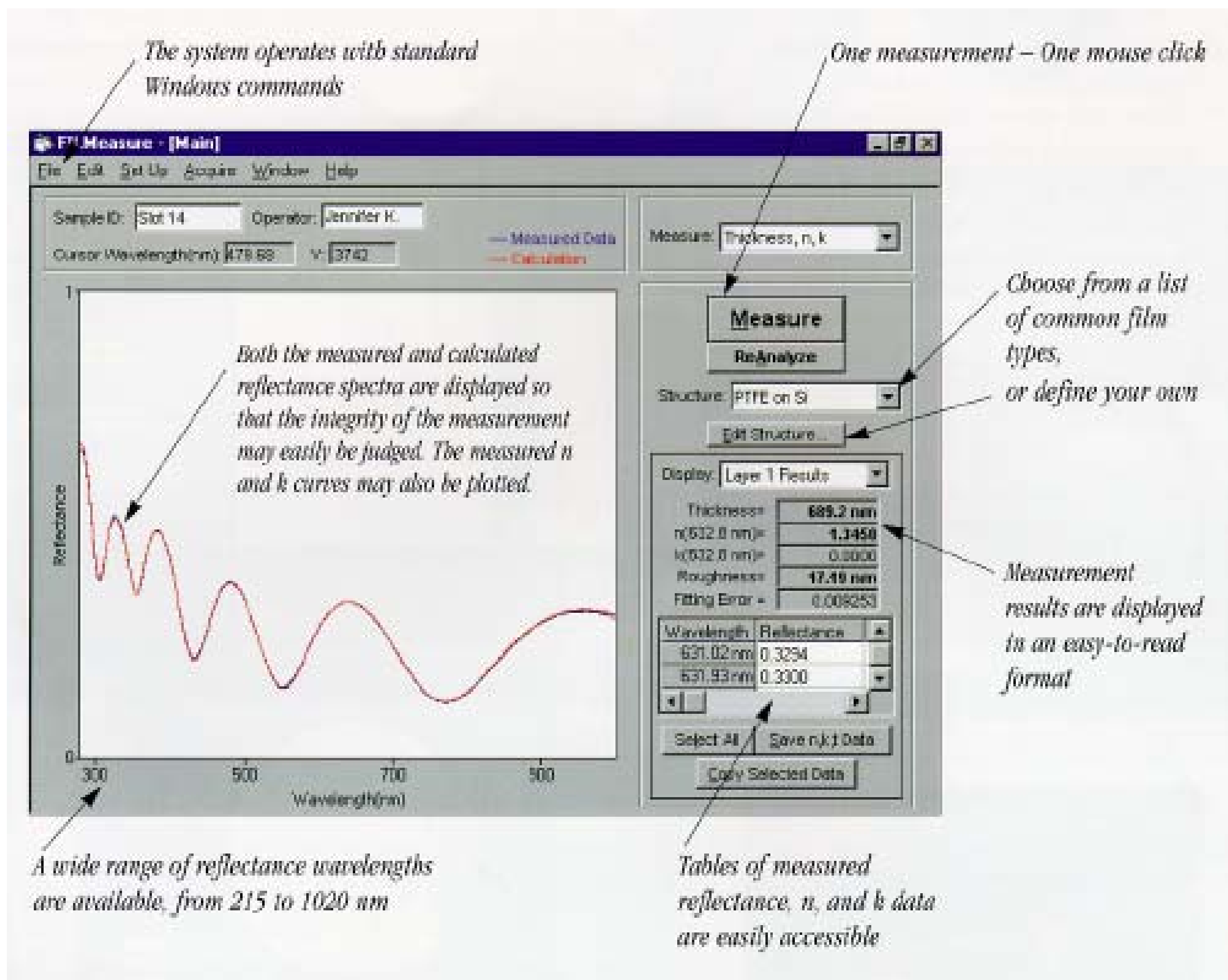


Figure 46: Main Filmetrics data analysis window.

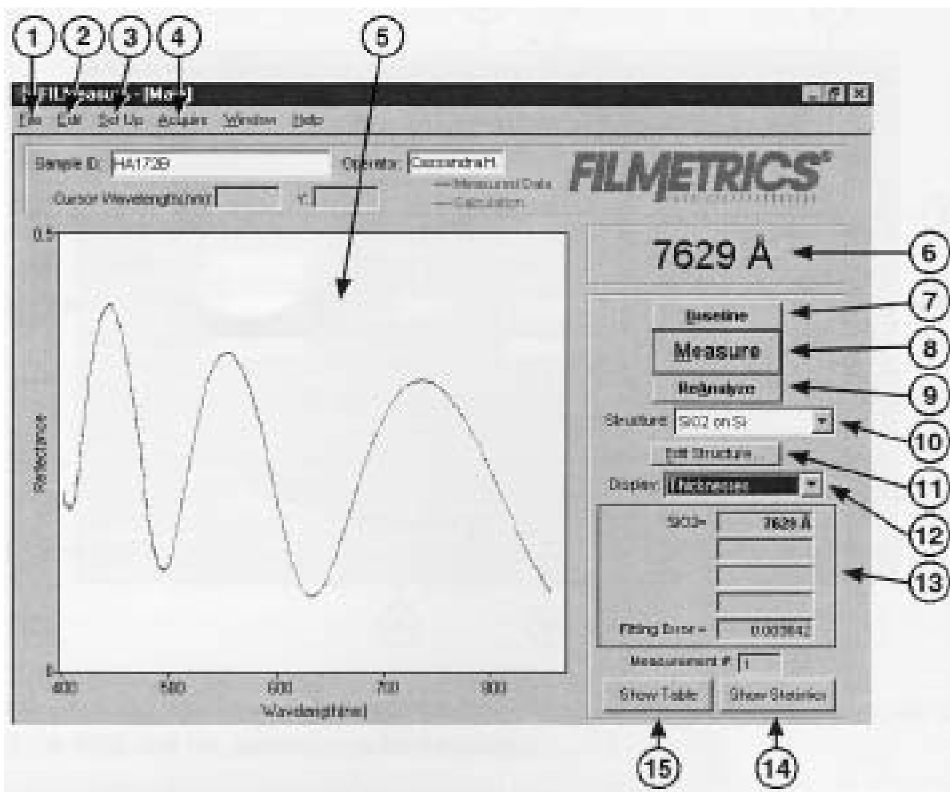


Figure 47: FILMeasure Main Window:

1. Standard Windows File menu for saving and retrieving data, printing, etc.
2. The Edit menu is used for copying measured spectra and measurement results, as well as selecting thickness units and editing the material library.
3. Used to setup reflectance acquisition parameters and the graphic display.
4. For starting and stopping continuous reflectance acquisition. Convenient for setting up hardware.
5. Graphical display for measured and calculated reflectance, as well as measured optical constants. Change display limits by double-clicking in the display area.
6. The measured film thickness is displayed here.
7. The baseline measurement sequence, which is required before measurements are made, is initiated by pressing the Baseline button.
8. This button causes a reflectance spectrum to be acquired and then analyzed in one step.
9. Analysis only on the displayed reflectance spectrum. Usually used when trying different analysis settings on a previously acquired spectrum.
10. Used to select the film structure that is to be measured.
11. This is where the selected film structure is described, and the analysis parameters are set.
12. Used to select the information displayed in the Results Box below.
13. The Results Box summarizes the most recent measurement results.
14. Statistical tabulation of all measurement results are accessed by pushing this button.
15. Complete results of the most recent measurement are accessed by pushing this button.

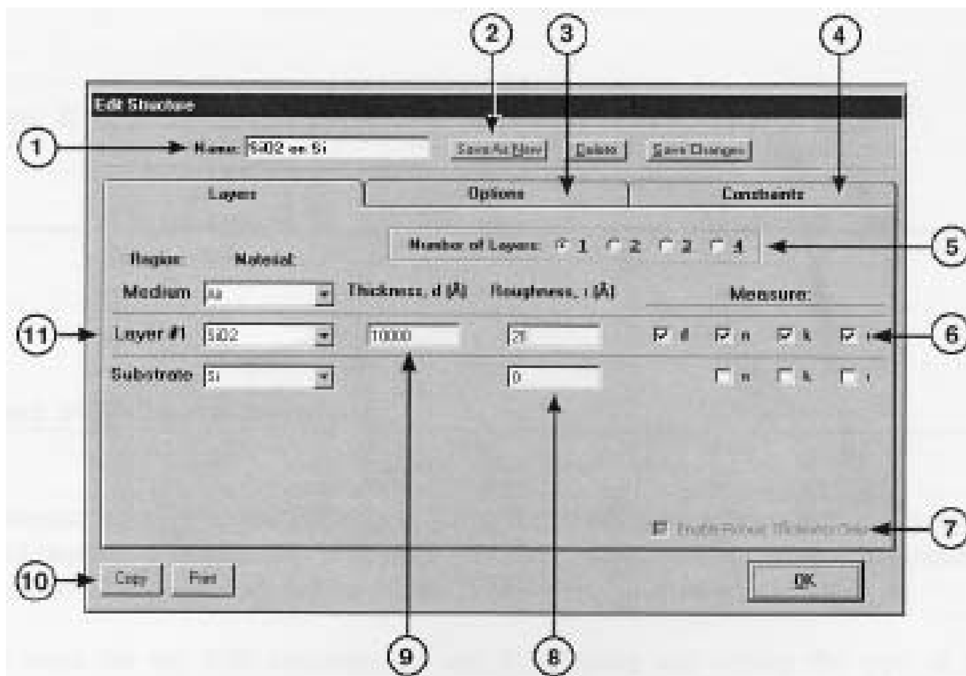


Figure 48: Edit Structure Window

A structure defines the film to be measured, the substrate and any underlying films, the approximate thickness of the film, and the quantities to be measured:

1. The name of the film structure is listed/edited here.

2. The structure can be saved as a new structure, deleted, or changes can be saved.

3. Advanced measurement parameters can be accessed by clicking on the Options tab.

4. Constraints on the possible measured values are selected here.
5. The number of film layers is chosen here.
6. The values to be measured are selected by checking the appropriate boxes.
7. A very robust thickness measurement routine is enabled by selecting this box.
8. Known film roughness for films not being measured, and the initial guess for the film(s) being measured are entered in this column.
9. Known film thicknesses for films not being measured, and the initial guess for the film(s) being measured are entered here.
10. All of the Edit Structure parameters can be copied or printed. This is convenient for remembering temporary setups, setting up multiple F20s, or sending measurement parameters to Filmetrics for troubleshooting.
11. The film layers are listed here. Common films can be selected from the pull-down menus.

Example: Thickness and Optical Constants of Films on Opaque Substrates: $Si0_2$ on Silicon

For this example we will demonstrate only the measurement of SiO_2 on silicon, but this type of measurement has an extremely broad range of applications, including the measurement of nitrides, polysilicon, and optical coatings.

Hardware: Any standard or rotating sample stage should work fine. The sample frontside must be flat. If the sample backside is not flat and parallel with the frontside, then the contact stage must be used.

Step 1: Select the film structure

Select the film structure to be measured, in this case "Si02 on Si", from the "Structure:" selection box on the main screen. If the structure to be measured does not exist, a new structure must be defined.

Step 2: Edit the film structure

Figure 49: Example Edit Structure:Layers window for measuring the thickness, *n,* and *k* of films on an opaque substrate.

For this example the film structure will probably not require editing, unless a different film is being measured. To edit the structure, click on "Edit Structure" to open the dialog box. Check to see that the film sequence matches that of the actual sample. If not, different films can be selected. Also enter your best guess for the thickness of the film to

be measured. Also check that thickness, n, and k of the SiO_2, layer are selected to be measured.

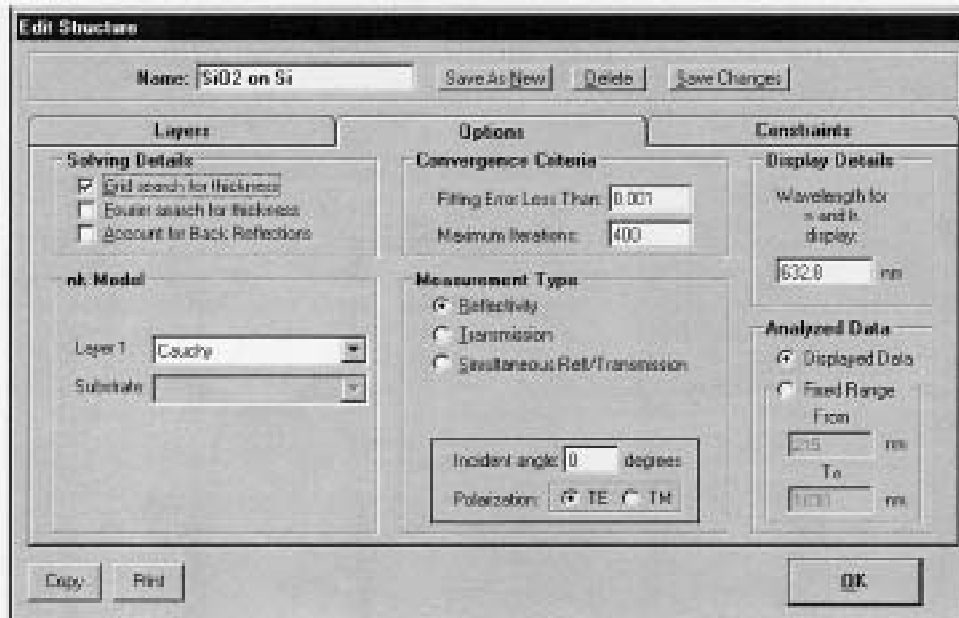


Figure 50: Example Edit Structure:Options window for measuring the thickness, *n,* and k of films on an opaque substrate.

Step 3: Take a Baseline Measurement

Take a Baseline measurement by first clicking on the Baseline button on the main screen. On the Take Baseline dialog box, make certain the "Autoscale Integration Time" option is selected, and choose the Baseline Sample that will be used (Si in this case). Then put the Silicon Baseline sample on the measurement stage and click on "Take Baseline". Then remove the Baseline sample from the stage and click "Take Zero". (In the case of a contact probe, place the probe on the Baseline sample and click on "Take Baseline", and then remove the probe from the sample and click "Take Zero".)

Step 4: Make the Measurement

Make the measurement by placing your sample on the stage (or the contact probe on your sample) and click on the "Measure" button. FlLMeasure will then acquire the reflectance spectrum and calculate the corresponding thickness. If the measurement was successful, the calculated reflectance (the red line on the graph) will coincide with the measured reflectance (the blue line on the graph.)

If the measured and calculated spectra do not fall on top of each other, the resulting thickness, n, and k values are incorrect. If the mismatch between measured data and calculation is only slight, the results reported will only be off by a small amount. If the

measured and calculated spectra match, but the results are implausible, there may be a problem with the sample positioning and light collection. Causes and corrective actions to improve the measurements are listed in cases #5 and #6 in the troubleshooting section.

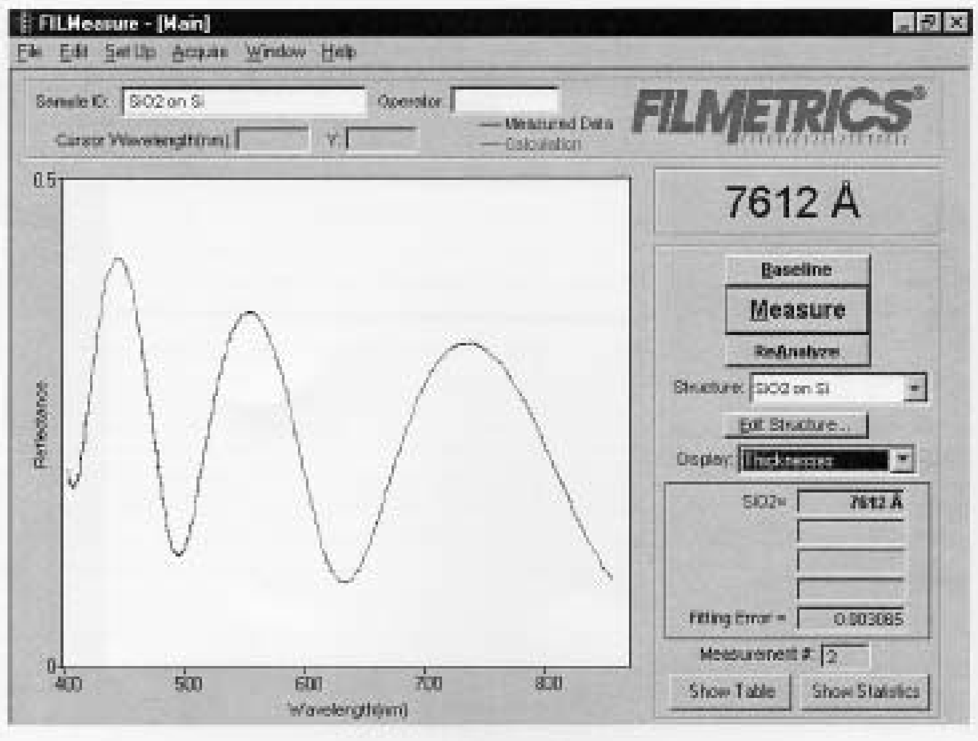


Figure 51: Measured and calculated reflectance spectra when measuring the thickness, n, k, and roughness of SiO_2 on silicon.

If the calculated (red) and measured (blue) minima and maxima do not coincide, then the measurement was not successful. There are several possible causes of an unsuccessful measurement. The most common for this type of measurement are described in cases #1, #2, #3, and #4 in the troubleshooting section of the Filmetrics manual.

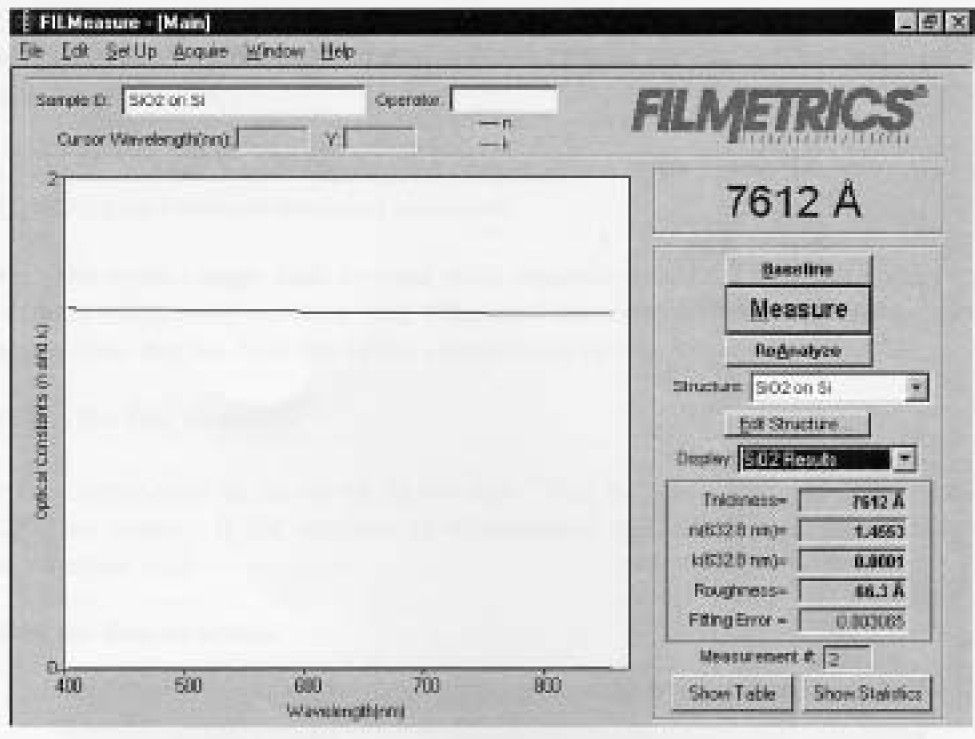


Figure 52: Calculated n and k spectra when measuring the thickness, n, k, and roughness of $Si0_2$ on silicon.

Ellipsometry:

(adapted from literature provided by Gaertner Scientific Co., bulletin EG)

Ellipsometry, that branch of optics concerned with the analysis, measurement and application of elliptically polarized light, is becoming widely known in the measurement of thin films. It is an exceedingly powerful yet sensitive method, and is applicable in a wide variety of situations.

The basis of ellipsometry is the fact that the state of polarization is altered upon reflection from both plain and coated surfaces. From a clean, film-free surface, the analysis of the elliptically polarized reflection can be used to determine the optical constants of the surface, namely the refractive index (n) and the extinction index (k). If, on the other hand, the surface is coated, ellipsometry can provide the refractive index and the thickness of the coating layer.

A brief explanation of the underlying theory of ellipsometry is given below. The nature and characteristics of polarized light are not discussed here, but are detailed in many general Physics and Optics texts. The bibliography listed on page provides a list of sources for a more in-depth description of the theory and application of ellipsometry.

The elliptical state of a polarized light beam is defined by the angular position of the ellipse (azimuth), its shape (ellipticity), and the sense of rotation of the light vector. Two parameters are required to determine the state of polarization; these are the amplitude ratio, psi (ψ), and the phase difference, delta (Δ). At the end of the last century Paul Drude stated the relationship between thickness of the film and the optical constants of the surface (or substrate) upon which the film was deposited. This relationship is mathematically stated as the fundamental equation of ellipsometry for an air/film/substrate stack:

$$\tan\left(\psi \cdot e^{i\Delta}\right) = \frac{\left(r_{p01} + r_{p12}\, e^{-2ix}\right)\cdot\left(1 + r_{s01}\cdot r_{s12}\, e^{-2ix}\right)}{\left(1 + r_{p01}\cdot r_{p12}\, e^{-2ix}\right)\left(r_{s01} + r_{s12}\, e^{-2ix}\right)}$$

where: $x = \frac{2\pi}{\lambda}\cdot d\cdot\left[(n_1)^2 - (n_0)^2 \sin^2\phi_0\right]^{1/2}$

and: $r_{p,s01}$ = the Fresnel reflection coefficient for the ambient medium-film interface,

$$r_{p01} = \frac{n_1\cos\phi_0 - n_0\cos\phi_1}{n_1\cos\phi_0 + n_0\cos\phi_1} \qquad r_{s01} = \frac{n_0\cos\phi_0 - n_1\cos\phi_1}{n_0\cos\phi_0 + n_1\cos\phi_1}$$

$r_{p,s12}$ = the Fresnel reflection coefficient for the film-substrate interface,

$$r_{p12} = \frac{n_2\cos\phi_1 - n_1\cos\phi_2}{n_2\cos\phi_1 + n_1\cos\phi_2} \qquad r_{s12} = \frac{n_1\cos\phi_1 - n_2\cos\phi_2}{n_1\cos\phi_1 + n_2\cos\phi_2}$$

where the angles are found from Snell's Law:

$$n_0\sin(\phi_0) = n_1\sin(\phi_1) = n_2\sin(\phi_2)$$

The subscript "p" indicates linearly polarized light, electric field vector parallel to plane of incidence; subscript "s" is for electric field vector normal to plane of incidence; n_0 = refractive index of ambient medium, n_1 = refractive index of film, d = thickness of film, λ = wavelength of light, ϕ_0 = angle of incidence from the air.

The ellipsometer is used to measure ψ and Δ, and thus the film thickness and index can be calculated. Since the equation contains complex quantities its solution is usually done by a computer or programmed calculator.

In essence, the instrument used for ellipsometric measurements is a polarizing spectrometer. The name ellipsometer was introduced in 1944 by Alexandre Rothen who became involved in the field while at the Rockfeller Institute for Medical Research. A typical ellipsometer (Figure 1) consists of a collimated monochromatic light source (sometimes a laser), a rotatable polarizer (GlanThompson prism), a compensator (usually a quarter-wave plate, either rotatable or fixed with its fast axis at 45° to the plane of incidence), a specimen stage or holder, a rotatable analyzer (Glan-Thompson prism) and a photodetector. In most cases the ellipsometer can be preset for different angles of incidence.

Description

The main components of the Gaertner L117 Production Ellipsometer are shown in Figure 53 and Figure 54.

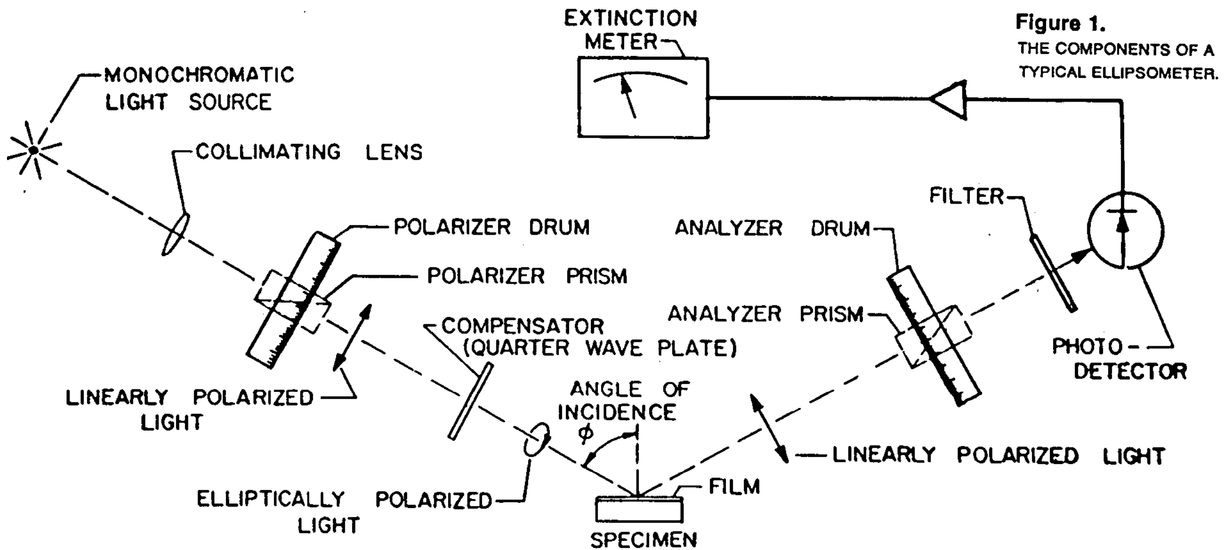


Figure 53: Main components of an ellipsometer.

The light from the helium-neon laser is first linearly polarized by passing through the polarizer and then elliptically polarized by passing through the compensator. When the light reflects from the specimen under measurement, the polarization of the light changes in accordance with the specimen film thickness and optical characteristics of the film and substrate.

This light then passes through the analyzer and is sensed by the photo detector. A filter mounted in front of the photo detector eliminates unwanted background light so that measurements can be made in normal room conditions. The amount of laser light reaching the photo detector is indicated by the extinction meter.

There are certain settings of the polarizer that cause the laser light reflecting from the specimen to become completely linearly polarized. When the polarizer is at one of these settings the analyzer can be rotated to a position where almost no light reaches the photo detector. The extinction meter then moves to its lowest reading. This is the

condition for measurement so this polarizer and analyzer drum setting is recorded. The measurement procedure described below uses two of these conditions. The second polarizer setting and corresponding analyzer position gives the second values. These four drum readings (A_1A_2 for the analyzer drum and P_1P_2 for the polarizer) complete the ellipsometric measurement. The ellipsometric parameters ψ and Δ are given by

$$\psi = \frac{180^o - (A_2 - A_1)}{2} \qquad \Delta = 360^o - (P_2 + P_1)$$

We can then use tables, graphs, or the computer program provided to find the film thickness and refractive index (assuming we already know the index of the substrate).

References

"Ellipsometry: Technique for the Characterization of Surfaces in Light-transmitting Ambients," Azzam and Bashara,
J. Vac. Sci. Tech. 12 #4, 1975.
Ellipsometry and Polarized Light, by Azzam and Bashara, North-Holland Publishing Co., N.J., 1976.

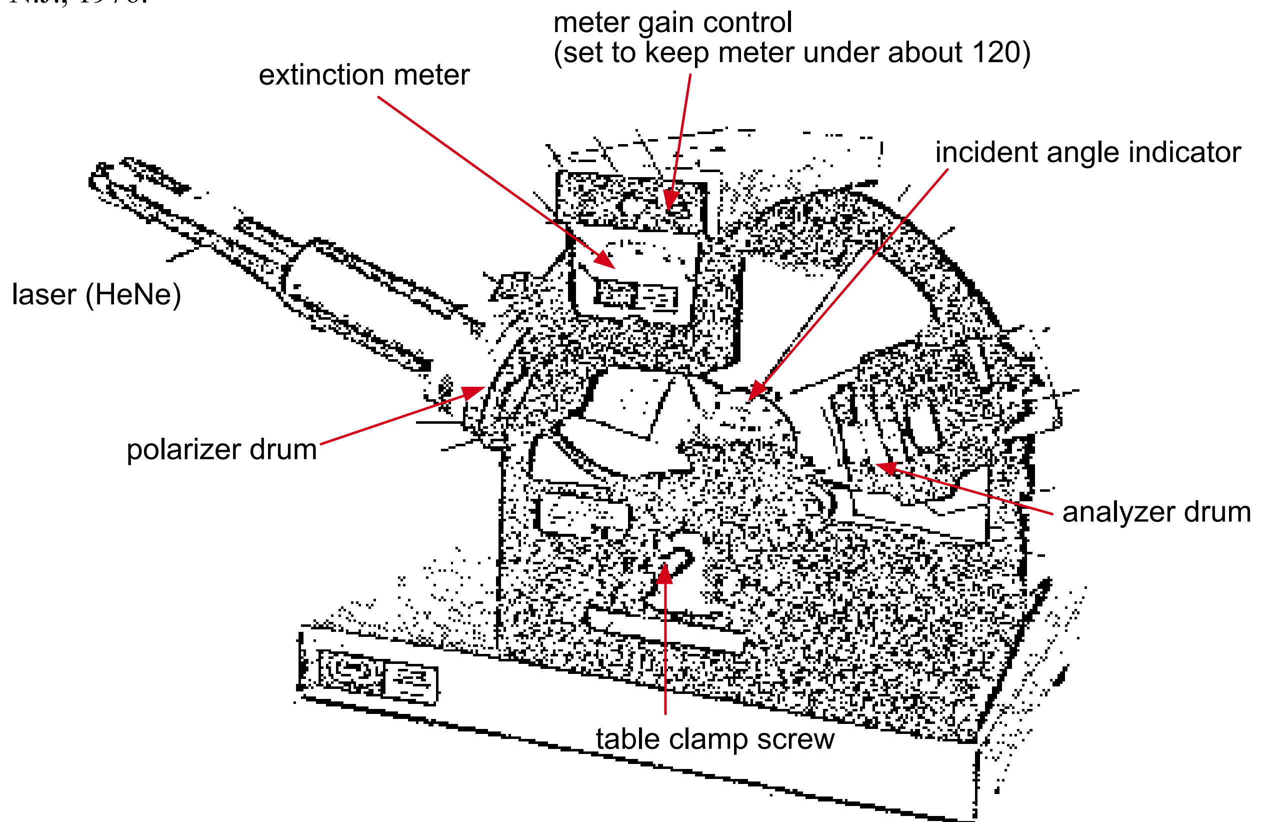
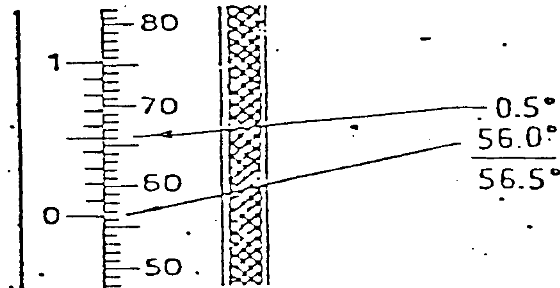


Figure 54: Gaertner L117 Ellipsometer

Note on Reading the Analyzer and Polarizer Drums

The polarizer and analyzer contain high quality Glan Thompson prisms. Each prism is rotated within the divided drum and its position read at the zero (0) line

mark. To read the angular value of the drum note the number of whole degrees that occur just below the 0 line mark, then add to it the fraction of a single degree that is determined by the vernier. To determine this fraction observe which of the ten lines of the vernier aligns with an adjacent drum line (See sketch).



Operating Procedure for Gaertner L117 Ellipsometer

1. With the specimen table set at the correct height (this should already be set) and both drums set midway in the red numbers, adjust gain control until meter reads midway between 3/4 and full scale (150 to 200; try to stay under 150 since the response time of the circuit is slower when set above 150).
2. Rotate analyzer (right hand drum) slowly in the red numbered segment (0˚ to 90˚) and set this drum to give lowest reading on the extinction meter. NOTE: It is recommended that the operator rest both elbows on the table surface to minimize fatigue and improve setting accuracy.
3. Now rotate polarizer (left hand drum) slowly within the segment from 315˚ to 135˚ (again in the red numbers) and set this drum to give a new and even lower meter reading. If meter reading exceeds 110, readjust gain control to bring maximum reading below 100. The numerical value on the meter is not important, only the settings of the polarizer and analyzer drums which give the least reading on extinction meter.
4. Go back to the analyzer (right hand drum) and rotate slowly to drive the meter pointer to a new and still lower position. The analyzer must be within the red numbered segment (0˚ to 90˚). If it isn't, rotate the polarizer to a different setting within the red segment 315˚ to 135˚. If the meter reading falls below 25 (1/8 full scale), use the gain control to bring the meter indicator reading to between 50 and 100. **Note as the gain control gets above the "12 noon" position the sensitivity to rotation of the drums becomes VERY high!!! At gains over this you will probably not even feel the drums rotate; you will just apply torque, using only the motion of the meter as feedback.**

5. Go back to the polarizer (left hand drum) and rotate slowly to drive the meter pointer to a still lower position. **Work back and forth between analyzer and polarizer drums until the lowest possible meter reading is obtained.** These drum settings correspond to true extinction. **Note the gain setting: for "good" samples you should be able to get the gain to above the "2 o'clock" position with a meter reading of not more than about 100; the higher the gain and the lower the meter reading, the more confidence you have that you have really found the "null".**
6. Record the first analyzer reading A1 (right drum) and the first polarizer reading P1 (left drum) at extinction.

You are now ready to obtain the second set of drum readings A2 and P2.

7. Add 90˚ to the first polarizer drum reading P1, i.e., (P1 + 90˚). Rotate the polarizer drum to this approximately this sum. This is NOT an exact setting, it just gets you in the ball-park. You will again have to go through the interative procedure you followed above to find the final value of P2.
8. From 180˚ subtract the first analyzer drum reading A1 i.e: (180˚ - A1). Rotate the analyzer drum to this difference. Again, this is NOT an exact setting, it just gets you in the ball-park.
9. Now start the interative procedure: Slowly rotate polarizer drum to obtain lowest reading on the meter. It will not be necessary to rotate the drum more than a few degrees.
10. Slowly rotate analyzer drum to obtain a still lower meter reading. Adjust meter gain control to bring meter pointer around 50 if necessary.
11. Go back to polarizer drum and attempt to drive the meter pointer still lower. Set analyzer drum at lowest meter reading.
12. Now go to analyzer drum and attempt to drive the meter pointer to a lower reading. Set analyzer drum at lowest meter reading.
13. Work back and forth between analyzer and polarizer drums to obtain final lowest reading on the meter. **Again note the gain setting: for "good" samples you should be able to get the gain to above the "2 o'clock" position with a meter reading of not more than about 100; the higher the gain and the lower the meter reading, the more confidence you have that you have really found the "null".**
14. Record analyzer and polarizer readings (A2 and P2). The second set of values will vary slightly from the calculated (P1 + 90˚) and (180˚ - A1) values but should not differ by more than 4˚ for accurate measurements; they really should be within about 0.1˚

of (P1 + 90˚) and (180˚ - A1). This is again a "confidence test" of your data.

15. To determine the film thickness using ψ and Δ, use the relations:

$$\psi = \frac{180^o - (A_2 - A_1)}{2} \qquad \Delta = 360^o - (P_2 + P_1)$$

If (P1 + P2) is greater than or equal to 360˚, subtract 360˚ from it to find the correct value of (P1 + P2).

16. If time permits, measure several different locations on the chip to check for thickness variations and measurement errors.
17. To find the thickness and index of refraction of the film, use the computer program in lab or the tables below (Table 18). Note we assume the substrate index of refraction is n = 3.85 - 0.002i for silicon. We also expect the index of an $Si0_2$ film to be about 1.46.
18. If the thickness determined from the table is much lower than the expected thickness, proceed as follows: Refer to the graph of thickness periods (ω) (Figure 55) and determine the period for the given film index at the proper angle of incidence. Add the original value of film thickness to a multiple of film period to obtain the sum which comes closer to the expected film thickness.

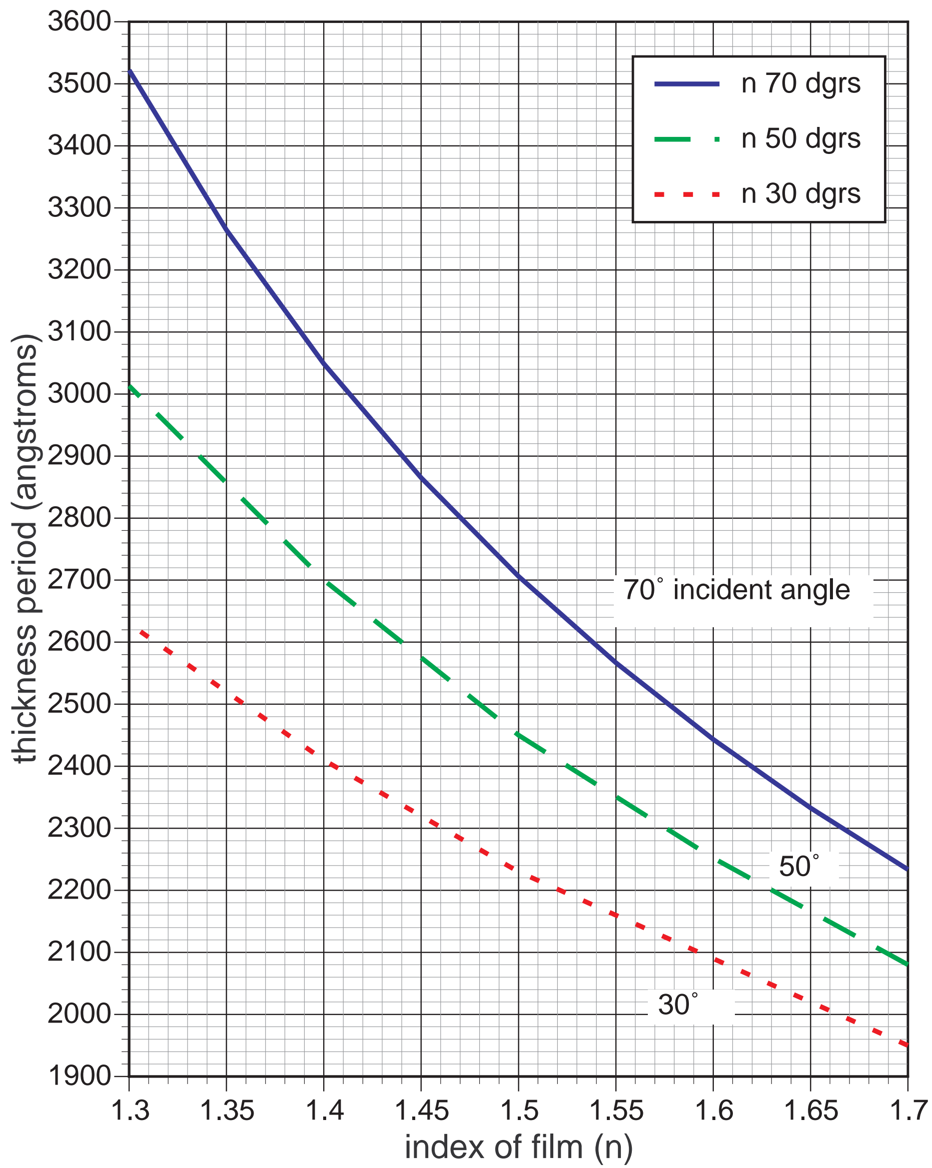


Figure 55: Thickness periods for silicon.

Table 18: Ellipsometric parameters Psi/Delta versus thickness & index

thickness	psi, 1.44	delta, 1.44	psi, 1.45	delta, 1.45	psi, 1.46	depta, 1.46	psi, 1.47	delta, 1.47
0	10.34	179.16	10.34	179.16	10.34	179.16	10.34	179.16
10	10.35	176.31	10.35	176.28	10.35	176.25	10.35	176.22
20	10.38	173.46	10.38	173.40	10.38	173.34	10.39	173.29
30	10.43	170.64	10.43	170.55	10.44	170.46	10.44	170.38
40	10.50	167.84	10.50	167.73	10.50	167.61	10.51	167.50
50	10.58	165.08	10.59	164.94	10.59	164.80	10.59	164.66
60	10.68	162.37	10.69	162.20	10.69	162.03	10.70	161.87
70	10.80	159.70	10.81	159.50	10.81	159.31	10.82	159.13
80	10.93	157.09	10.94	156.87	10.95	156.65	10.96	156.44
90	11.08	154.53	11.09	154.29	11.10	154.05	11.11	153.82
100	11.24	152.04	11.25	151.78	11.27	151.52	11.28	151.27
110	11.41	149.62	11.43	149.33	11.44	149.05	11.46	148.78
120	11.60	147.26	11.62	146.95	11.63	146.66	11.65	146.37
130	11.79	144.97	11.82	144.65	11.84	144.33	11.86	144.03
140	12.00	142.75	12.03	142.41	12.05	142.08	12.08	141.76
150	12.22	140.60	12.25	140.24	12.28	139.90	12.30	139.56
160	12.45	138.52	12.48	138.15	12.51	137.79	12.54	137.44
170	12.69	136.50	12.72	136.12	12.76	135.74	12.79	135.38
180	12.93	134.56	12.97	134.16	13.01	133.77	13.04	133.40
190	13.19	132.67	13.23	132.26	13.27	131.86	13.30	131.48
200	13.45	130.85	13.49	130.43	13.53	130.02	13.57	129.63
210	13.71	129.09	13.76	128.66	13.80	128.24	13.85	127.84
220	13.98	127.40	14.03	126.95	14.08	126.52	14.13	126.11
230	14.26	125.75	14.31	125.30	14.37	124.86	14.42	124.44
240	14.54	124.17	14.60	123.71	14.65	123.26	14.71	122.82
250	14.83	122.63	14.89	122.16	14.95	121.71	15.00	121.27
260	15.12	121.15	15.18	120.67	15.24	120.21	15.30	119.76
270	15.41	119.72	15.48	119.23	15.54	118.76	15.60	118.30
280	15.71	118.33	15.78	117.84	15.84	117.36	15.91	116.89
290	16.01	116.99	16.08	116.49	16.15	116.00	16.21	115.53
300	16.31	115.69	16.38	115.18	16.46	114.69	16.52	114.21
310	16.61	114.43	16.69	113.92	16.76	113.42	16.84	112.93
320	16.91	113.21	17.00	112.69	17.07	112.19	17.15	111.69
330	17.22	112.03	17.31	111.50	17.39	110.99	17.47	110.49
340	17.53	110.89	17.62	110.35	17.70	109.84	17.78	109.33

Assumed: λ = 6328 Angstroms; n_{Si} = 3.850 - i*0.02; incident angle = 70˚

thickness	psi, 1.44	delta, 1.44	psi, 1.45	delta, 1.45	psi, 1.46	depta, 1.46	psi, 1.47	delta, 1.47
350	17.84	109.78	17.93	109.24	18.02	108.72	18.10	108.21
360	18.15	108.70	18.24	108.16	18.33	107.63	18.42	107.11
370	18.46	107.66	18.55	107.11	18.65	106.57	18.74	106.05
380	18.77	106.64	18.87	106.09	18.96	105.55	19.05	105.02
390	19.08	105.66	19.18	105.10	19.28	104.55	19.37	104.02
400	19.39	104.70	19.50	104.14	19.60	103.59	19.69	103.05
410	19.70	103.78	19.81	103.21	19.91	102.65	20.01	102.11
420	20.01	102.88	20.13	102.30	20.23	101.74	20.33	101.19
430	20.33	102.00	20.44	101.42	20.55	100.85	20.65	100.30
440	20.64	101.15	20.75	100.56	20.87	99.99	20.97	99.43
450	20.95	100.32	21.07	99.73	21.18	99.15	21.29	98.59
460	21.26	99.52	21.38	98.92	21.50	98.34	21.61	97.77
470	21.57	98.74	21.70	98.14	21.81	97.55	21.93	96.97
480	21.88	97.98	22.01	97.37	22.13	96.78	22.25	96.20
490	22.19	97.24	22.32	96.63	22.45	96.03	22.57	95.44
500	22.50	96.52	22.63	95.90	22.76	95.30	22.88	94.71
510	22.81	95.82	22.95	95.20	23.08	94.59	23.20	94.00
520	23.12	95.14	23.26	94.52	23.39	93.90	23.52	93.31
530	23.43	94.48	23.57	93.85	23.71	93.23	23.84	92.63
540	23.74	93.84	23.88	93.20	24.02	92.58	24.15	91.98
550	24.05	93.21	24.19	92.57	24.34	91.95	24.47	91.34
560	24.36	92.60	24.51	91.96	24.65	91.34	24.79	90.72
570	24.66	92.01	24.82	91.37	24.96	90.74	25.11	90.12
580	24.97	91.44	25.13	90.79	25.28	90.16	25.42	89.53
590	25.28	90.89	25.44	90.23	25.59	89.59	25.74	88.96
600	25.59	90.35	25.75	89.69	25.91	89.04	26.06	88.41
610	25.90	89.82	26.06	89.16	26.22	88.51	26.38	87.87
620	26.20	89.31	26.37	88.65	26.54	88.00	26.69	87.35
630	26.51	88.82	26.69	88.15	26.85	87.50	27.01	86.85
640	26.82	88.34	27.00	87.67	27.17	87.01	27.33	86.36
650	27.13	87.88	27.31	87.21	27.49	86.54	27.66	85.89
660	27.44	87.44	27.63	86.76	27.81	86.09	27.98	85.43
670	27.75	87.00	27.94	86.32	28.13	85.65	28.30	84.99
680	28.07	86.59	28.26	85.90	28.45	85.22	28.63	84.56
690	28.38	86.18	28.58	85.49	28.77	84.82	28.96	84.14
700	28.69	85.79	28.90	85.10	29.09	84.42	29.28	83.75
710	29.01	85.42	29.22	84.73	29.42	84.04	29.62	83.36
720	29.33	85.06	29.54	84.36	29.75	83.67	29.95	82.99

Assumed: λ = 6328 Angstroms; n_{Si} = 3.850 - i*0.02; incident angle = 70˚

thickness	psi, 1.44	delta, 1.44	psi, 1.45	delta, 1.45	psi, 1.46	depta, 1.46	psi, 1.47	delta, 1.47
730	29.65	84.71	29.87	84.01	30.08	83.32	30.29	82.64
740	29.97	84.38	30.19	83.68	30.41	82.98	30.63	82.29
750	30.29	84.07	30.52	83.36	30.75	82.66	30.97	81.97
760	30.62	83.76	30.86	83.05	31.09	82.35	31.31	81.65
770	30.95	83.47	31.19	82.76	31.43	82.06	31.66	81.36
780	31.28	83.20	31.53	82.48	31.78	81.77	32.02	81.07
790	31.62	82.94	31.88	82.22	32.13	81.51	32.38	80.80
800	31.96	82.69	32.22	81.97	32.48	81.26	32.74	80.54
810	32.30	82.46	32.57	81.73	32.84	81.02	33.11	80.30
820	32.65	82.24	32.93	81.51	33.21	80.79	33.48	80.07
830	33.00	82.03	33.29	81.31	33.58	80.58	33.86	79.86
840	33.36	81.84	33.66	81.11	33.95	80.39	34.25	79.66
850	33.72	81.67	34.03	80.93	34.33	80.20	34.64	79.48
860	34.09	81.50	34.40	80.77	34.72	80.04	35.04	79.30
870	34.46	81.36	34.79	80.62	35.12	79.88	35.45	79.15
880	34.84	81.22	35.18	80.48	35.52	79.74	35.86	79.00
890	35.22	81.10	35.58	80.36	35.93	79.62	36.29	78.87
900	35.62	81.00	35.99	80.25	36.35	79.51	36.72	78.76
910	36.02	80.91	36.40	80.16	36.78	79.41	37.17	78.66
920	36.43	80.84	36.82	80.09	37.22	79.33	37.63	78.57
930	36.84	80.78	37.26	80.02	37.67	79.27	38.09	78.50
940	37.27	80.73	37.70	79.98	38.13	79.21	38.57	78.45
950	37.71	80.70	38.15	79.94	38.61	79.18	39.06	78.40
960	38.15	80.69	38.62	79.93	39.09	79.16	39.57	78.37
970	38.61	80.69	39.10	79.92	39.59	79.15	40.09	78.36
980	39.08	80.71	39.59	79.94	40.10	79.16	40.62	78.36
990	39.56	80.74	40.09	79.97	40.63	79.18	41.18	78.38
1000	40.06	80.79	40.61	80.01	41.17	79.22	41.74	78.41
1010	40.56	80.85	41.14	80.07	41.73	79.27	42.33	78.45
1020	41.09	80.94	41.69	80.15	42.31	79.34	42.94	78.51
1030	41.63	81.04	42.26	80.24	42.90	79.43	43.56	78.59
1040	42.18	81.15	42.84	80.35	43.52	79.53	44.21	78.67
1050	42.75	81.28	43.44	80.48	44.15	79.65	44.88	78.78
1060	43.34	81.43	44.06	80.62	44.81	79.78	45.57	78.89
1070	43.95	81.60	44.71	80.78	45.49	79.93	46.29	79.03
1080	44.58	81.79	45.37	80.96	46.19	80.09	47.04	79.17
1090	45.22	81.99	46.06	81.16	46.92	80.27	47.81	79.33
1100	45.90	82.22	46.77	81.37	47.68	80.47	48.61	79.51

Assumed: λ = 6328 Angstroms; n_{Si} = 3.850 - i*0.02; incident angle = 70˚

thickness	psi, 1.44	delta, 1.44	psi, 1.45	delta, 1.45	psi, 1.46	depta, 1.46	psi, 1.47	delta, 1.47
1110	46.59	82.46	47.51	81.60	48.46	80.68	49.44	79.69
1120	47.31	82.72	48.27	81.85	49.27	80.91	50.31	79.90
1130	48.05	83.01	49.06	82.12	50.12	81.16	51.20	80.11
1140	48.82	83.31	49.89	82.41	50.99	81.42	52.13	80.34
1150	49.62	83.64	50.74	82.71	51.90	81.70	53.10	80.59
1160	50.44	83.98	51.62	83.04	52.84	82.00	54.10	80.84
1170	51.30	84.35	52.53	83.39	53.82	82.32	55.15	81.11
1180	52.19	84.75	53.48	83.76	54.83	82.65	56.23	81.39
1190	53.11	85.17	54.47	84.15	55.89	83.00	57.35	81.69
1200	54.06	85.61	55.49	84.57	56.98	83.37	58.52	81.99
1210	55.05	86.09	56.55	85.01	58.11	83.76	59.73	82.31
1220	56.08	86.59	57.65	85.48	59.29	84.18	60.98	82.63
1230	57.14	87.13	58.79	85.98	60.51	84.61	62.28	82.97
1240	58.24	87.70	59.97	86.50	61.77	85.07	63.63	83.32
1250	59.37	88.31	61.19	87.06	63.07	85.55	65.02	83.68
1260	60.55	88.96	62.45	87.66	64.42	86.06	66.45	84.05
1270	61.77	89.65	63.76	88.30	65.82	86.60	67.93	84.42
1280	63.03	90.40	65.10	88.99	67.25	87.17	69.46	84.80
1290	64.32	91.21	66.49	89.73	68.74	87.79	71.03	85.19
1300	65.66	92.09	67.92	90.54	70.26	88.45	72.64	85.58
1310	67.03	93.05	69.40	91.43	71.82	89.18	74.29	85.98
1320	68.45	94.11	70.90	92.41	73.43	89.98	75.98	86.38
1330	69.90	95.29	72.45	93.52	75.07	90.88	77.70	86.79
1340	71.38	96.61	74.03	94.78	76.74	91.91	79.46	87.18
1350	72.90	98.13	75.64	96.25	78.44	93.14	81.24	87.57
1360	74.44	99.89	77.28	98.02	80.17	94.67	83.04	87.95
1370	76.01	101.98	78.94	100.22	81.92	96.69	84.87	88.27
1380	77.59	104.52	80.61	103.08	83.68	99.62	86.70	88.48
1390	79.17	107.72	82.28	107.02	85.44	104.49	88.55	88.08
1400	80.75	111.92	83.92	112.92	87.14	114.83	89.60	275.39
1410	82.28	117.68	85.48	122.77	88.55	148.17	87.75	271.42
1420	83.74	126.06	86.81	141.43	88.37	221.04	85.90	271.43
1430	85.01	138.90	87.48	176.00	86.86	247.52	84.07	271.71
1440	85.92	158.65	87.00	213.19	85.14	256.40	82.25	272.06
1450	86.17	184.67	85.76	234.43	83.38	260.82	80.46	272.44
1460	85.66	209.05	84.23	245.45	81.62	263.54	78.69	272.83
1470	84.59	226.14	82.59	251.89	79.88	265.46	76.95	273.23
1480	83.24	237.13	80.93	256.12	78.15	266.93	75.24	273.64

Assumed: λ = 6328 Angstroms; n_{Si} = 3.850 - i*0.02; incident angle = 70°

thic knes s	psi, 1.44	delta, 1.44	psi, 1.45	delta, 1.45	psi, 1.46	depta, 1.46	psi, 1.47	delta, 1.47
1490	81.75	244.43	79.26	259.14	76.45	268.12	73.56	274.04
1500	80.19	249.55	77.59	261.44	74.78	269.13	71.93	274.43
1510	78.61	253.34	75.95	263.28	73.15	270.01	70.34	274.82
1520	77.03	256.28	74.33	264.80	71.55	270.79	68.79	275.21
1530	75.45	258.65	72.75	266.10	69.99	271.50	67.28	275.59
1540	73.89	260.61	71.19	267.23	68.48	272.16	65.82	275.96
1550	72.36	262.27	69.67	268.23	67.00	272.77	64.40	276.32
1560	70.85	263.71	68.20	269.14	65.57	273.34	63.03	276.68
1570	69.38	264.98	66.76	269.96	64.18	273.87	61.70	277.02
1580	67.94	266.11	65.36	270.71	62.84	274.38	60.42	277.35
1590	66.54	267.14	64.00	271.41	61.54	274.85	59.19	277.67
1600	65.18	268.06	62.69	272.06	60.29	275.31	58.00	277.99
1610	63.85	268.92	61.42	272.66	59.08	275.74	56.85	278.29
1620	62.57	269.70	60.19	273.23	57.91	276.14	55.74	278.57
1630	61.33	270.43	59.00	273.77	56.78	276.53	54.68	278.85
1640	60.12	271.11	57.85	274.27	55.69	276.90	53.65	279.11
1650	58.96	271.75	56.75	274.74	54.65	277.25	52.66	279.36
1660	57.83	272.34	55.68	275.19	53.64	277.58	51.71	279.60
1670	56.75	272.90	54.65	275.61	52.66	277.89	50.79	279.82
1680	55.70	273.43	53.66	276.01	51.73	278.18	49.91	280.03
1690	54.69	273.92	52.70	276.38	50.82	278.46	49.06	280.23
1700	53.71	274.38	51.78	276.73	49.95	278.72	48.24	280.41
1710	52.77	274.82	50.89	277.06	49.12	278.97	47.45	280.58
1720	51.86	275.23	50.03	277.37	48.31	279.19	46.69	280.73
1730	50.98	275.61	49.20	277.66	47.53	279.40	45.96	280.87
1740	50.13	275.98	48.40	277.94	46.78	279.60	45.25	280.99
1750	49.32	276.31	47.63	278.19	46.05	279.77	44.57	281.11
1760	48.53	276.63	46.89	278.42	45.35	279.93	43.91	281.20
1770	47.77	276.93	46.17	278.64	44.68	280.08	43.27	281.28
1780	47.03	277.20	45.48	278.84	44.02	280.21	42.65	281.35
1790	46.32	277.46	44.81	279.02	43.39	280.32	42.05	281.40
1800	45.64	277.69	44.16	279.18	42.78	280.42	41.47	281.44
1810	44.97	277.91	43.54	279.32	42.19	280.50	40.91	281.46
1820	44.33	278.11	42.93	279.45	41.61	280.57	40.36	281.47
1830	43.71	278.29	42.34	279.57	41.05	280.62	39.84	281.46
1840	43.11	278.45	41.77	279.66	40.51	280.65	39.32	281.44
1850	42.52	278.59	41.22	279.74	39.99	280.67	38.82	281.41
1860	41.96	278.72	40.68	279.80	39.48	280.68	38.33	281.36

Assumed: λ = 6328 Angstroms; n_{Si} = 3.850 - i*0.02; incident angle = 70˚

thickness	psi, 1.44	delta, 1.44	psi, 1.45	delta, 1.45	psi, 1.46	depta, 1.46	psi, 1.47	delta, 1.47
1870	41.41	278.83	40.16	279.85	38.98	280.67	37.86	281.29
1880	40.88	278.92	39.66	279.88	38.50	280.64	37.40	281.22
1890	40.36	278.99	39.16	279.90	38.03	280.60	36.95	281.12
1900	39.85	279.05	38.68	279.90	37.57	280.55	36.50	281.02
1910	39.36	279.10	38.21	279.88	37.12	280.48	36.07	280.89
1920	38.89	279.12	37.76	279.85	36.68	280.39	35.65	280.76
1930	38.42	279.13	37.31	279.81	36.25	280.29	35.24	280.61
1940	37.97	279.13	36.87	279.75	35.83	280.18	34.83	280.44
1950	37.52	279.11	36.45	279.67	35.42	280.05	34.43	280.26
1960	37.09	279.07	36.03	279.58	35.02	279.91	34.04	280.07
1970	36.66	279.02	35.62	279.48	34.62	279.75	33.66	279.86
1980	36.25	278.96	35.22	279.36	34.23	279.58	33.28	279.64
1990	35.84	278.88	34.83	279.22	33.85	279.40	32.91	279.41
2000	35.44	278.78	34.44	279.07	33.48	279.20	32.54	279.16
2010	35.05	278.67	34.06	278.91	33.11	278.98	32.18	278.89
2020	34.67	278.54	33.69	278.73	32.74	278.75	31.83	278.62
2030	34.29	278.40	33.32	278.54	32.38	278.51	31.47	278.32
2040	33.92	278.25	32.96	278.34	32.03	278.26	31.12	278.02
2050	33.55	278.08	32.60	278.12	31.68	277.99	30.78	277.70
2060	33.19	277.90	32.25	277.88	31.33	277.70	30.44	277.36
2070	32.84	277.70	31.90	277.63	30.99	277.40	30.10	277.01
2080	32.49	277.49	31.56	277.37	30.65	277.09	29.76	276.65
2090	32.14	277.27	31.22	277.09	30.31	276.76	29.43	276.27
2100	31.80	277.03	30.88	276.80	29.98	276.42	29.10	275.88
2110	31.46	276.77	30.55	276.50	29.65	276.06	28.77	275.47
2120	31.12	276.51	30.21	276.18	29.32	275.69	28.44	275.05
2130	30.79	276.22	29.88	275.85	28.99	275.31	28.12	274.61
2140	30.46	275.93	29.56	275.50	28.67	274.91	27.79	274.16
2150	30.14	275.62	29.23	275.14	28.35	274.49	27.47	273.70
2160	29.81	275.29	28.91	274.76	28.02	274.07	27.15	273.21
2170	29.49	274.96	28.59	274.37	27.70	273.62	26.83	272.72
2180	29.17	274.60	28.27	273.96	27.39	273.16	26.51	272.20
2190	28.85	274.24	27.95	273.54	27.07	272.69	26.19	271.67
2200	28.54	273.86	27.64	273.11	26.75	272.20	25.87	271.13
2210	28.22	273.46	27.32	272.66	26.43	271.69	25.55	270.57
2220	27.91	273.05	27.01	272.19	26.12	271.17	25.23	269.99
2230	27.59	272.63	26.69	271.71	25.80	270.64	24.91	269.39
2240	27.28	272.19	26.38	271.22	25.49	270.08	24.60	268.78

Assumed: λ = 6328 Angstroms; n_{Si} = 3.850 - i*0.02; incident angle = 70˚

thickness	psi, 1.44	delta, 1.44	psi, 1.45	delta, 1.45	psi, 1.46	depta, 1.46	psi, 1.47	delta, 1.47
2250	26.97	271.73	26.07	270.71	25.17	269.51	24.28	268.15
2260	26.66	271.26	25.76	270.18	24.86	268.93	23.96	267.50
2270	26.35	270.78	25.44	269.64	24.54	268.32	23.64	266.83
2280	26.04	270.28	25.13	269.08	24.23	267.70	23.33	266.15
2290	25.73	269.76	24.82	268.50	23.91	267.06	23.01	265.44
2300	25.42	269.23	24.51	267.91	23.60	266.41	22.69	264.72
2310	25.12	268.68	24.20	267.30	23.28	265.73	22.37	263.97
2320	24.81	268.12	23.89	266.67	22.97	265.03	22.05	263.21
2330	24.50	267.53	23.57	266.02	22.65	264.32	21.73	262.42
2340	24.19	266.94	23.26	265.36	22.33	263.58	21.41	261.61
2350	23.88	266.32	22.95	264.67	22.02	262.83	21.09	260.77
2360	23.57	265.69	22.64	263.97	21.70	262.05	20.77	259.92
2370	23.26	265.03	22.32	263.25	21.39	261.25	20.45	259.04
2380	22.95	264.36	22.01	262.50	21.07	260.43	20.13	258.13
2390	22.64	263.67	21.69	261.74	20.75	259.58	19.81	257.19
2400	22.33	262.96	21.38	260.95	20.43	258.71	19.49	256.23
2410	22.02	262.23	21.07	260.14	20.12	257.82	19.17	255.24
2420	21.71	261.48	20.75	259.31	19.80	256.90	18.85	254.23
2430	21.40	260.71	20.44	258.45	19.48	255.95	18.53	253.18
2440	21.09	259.92	20.12	257.57	19.16	254.97	18.22	252.09
2450	20.78	259.10	19.81	256.67	18.85	253.97	17.90	250.98
2460	20.46	258.26	19.49	255.73	18.53	252.93	17.58	249.83
2470	20.15	257.39	19.18	254.77	18.21	251.86	17.27	248.64
2480	19.84	256.50	18.86	253.78	17.90	250.76	16.95	247.42
2490	19.53	255.59	18.55	252.76	17.58	249.63	16.64	246.16
2500	19.22	254.65	18.24	251.71	17.27	248.46	16.33	244.85
2510	18.90	253.67	17.92	250.63	16.96	247.25	16.02	243.51
2520	18.59	252.67	17.61	249.52	16.65	246.01	15.71	242.11
2530	18.28	251.64	17.30	248.36	16.34	244.72	15.41	240.67
2540	17.97	250.58	16.99	247.18	16.03	243.39	15.11	239.19
2550	17.66	249.49	16.68	245.95	15.73	242.02	14.81	237.65
2560	17.35	248.36	16.38	244.69	15.43	240.60	14.52	236.05
2570	17.05	247.19	16.07	243.38	15.13	239.13	14.23	234.40
2580	16.74	245.99	15.77	242.03	14.83	237.61	13.95	232.69
2590	16.44	244.75	15.47	240.63	14.54	236.04	13.67	230.93
2600	16.13	243.47	15.17	239.19	14.26	234.41	13.40	229.10
2610	15.83	242.15	14.88	237.70	13.98	232.73	13.13	227.20
2620	15.54	240.78	14.59	236.15	13.70	230.99	12.88	225.24

Assumed: λ = 6328 Angstroms; n_{Si} = 3.850 - i*0.02; incident angle = 70˚

thickness	psi, 1.44	delta, 1.44	psi, 1.45	delta, 1.45	psi, 1.46	depta, 1.46	psi, 1.47	delta, 1.47
2630	15.24	239.36	14.31	234.56	13.43	229.19	12.63	223.21
2640	14.95	237.90	14.03	232.90	13.17	227.32	12.39	221.11
2650	14.66	236.39	13.75	231.19	12.91	225.39	12.16	218.94
2660	14.38	234.83	13.48	229.42	12.66	223.39	11.93	216.69
2670	14.10	233.21	13.22	227.59	12.42	221.32	11.72	214.38
2680	13.83	231.53	12.96	225.69	12.19	219.18	11.53	211.99
2690	13.56	229.80	12.72	223.73	11.97	216.97	11.34	209.53
2700	13.30	228.00	12.47	221.70	11.76	214.69	11.17	207.00
2710	13.04	226.15	12.24	219.60	11.56	212.34	11.01	204.40
2720	12.79	224.23	12.02	217.43	11.37	209.91	10.87	201.74
2730	12.55	222.24	11.81	215.19	11.20	207.42	10.74	199.02
2740	12.32	220.19	11.61	212.88	11.04	204.86	10.63	196.24
2750	12.09	218.06	11.42	210.50	10.90	202.24	10.54	193.42
2760	11.88	215.87	11.25	208.05	10.77	199.56	10.46	190.55
2770	11.68	213.61	11.08	205.54	10.65	196.82	10.40	187.65
2780	11.49	211.28	10.94	202.96	10.56	194.03	10.36	184.73
2790	11.31	208.89	10.80	200.32	10.48	191.20	10.34	181.79
2800	11.14	206.42	10.69	197.62	10.41	188.34	10.34	178.85
2810	10.99	203.90	10.58	194.88	10.37	185.45	10.35	175.90
2820	10.85	201.31	10.50	192.09	10.34	182.54	10.39	172.98
2830	10.73	198.66	10.43	189.27	10.34	179.62	10.44	170.07
2840	10.62	195.97	10.38	186.41	10.35	176.71	10.52	167.20
2850	10.53	193.22	10.35	183.54	10.38	173.80	10.60	164.36
2860	10.46	190.44	10.34	180.65	10.43	170.92	10.71	161.57
2870	10.40	187.63	10.34	177.77	10.49	168.06	10.83	158.84
2880	10.36	184.79	10.36	174.88	10.58	165.24	10.97	156.16
2890	10.34	181.94	10.41	172.02	10.68	162.46	11.13	153.55
2900	10.34	179.08	10.46	169.18	10.79	159.74	11.30	151.00
2910	10.35	176.23	10.54	166.37	10.93	157.07	11.48	148.52
2920	10.38	173.39	10.63	163.61	11.08	154.46	11.67	146.12
2930	10.43	170.56	10.74	160.89	11.24	151.91	11.88	143.78
2940	10.50	167.77	10.87	158.22	11.41	149.44	12.10	141.52
2950	10.59	165.01	11.01	155.61	11.60	147.03	12.33	139.33
2960	10.69	162.29	11.17	153.07	11.81	144.70	12.57	137.21
2970	10.80	159.63	11.34	150.59	12.02	142.43	12.81	135.17
2980	10.94	157.02	11.52	148.17	12.24	140.24	13.07	133.19
2990	11.08	154.47	11.71	145.83	12.47	138.11	13.33	131.28
3000	11.24	151.98	11.92	143.56	12.72	136.06	13.60	129.43

Computer Implementation of Ellipsometric Analysis: PCASP Program IR

by Doug Miller

The subroutine IR provides for a comprehensive ellipsometric analysis of highly reflecting substrates, with or without a deposited or grown thin film. Options are included to determine the complex index of refraction of the substrate, the index of refraction and thickness of a deposited film, and the thickness of a very thin film. Other options are available to modify current ellipsometric parameters, such as the wavelength of the light or the angle of incidence onto the sample. The routine makes use of the ellipsometric theory outlined in earlier. Numerous support subroutines have also been written that accept input from the keyboard of ellipsometric variables, check this data for validity, and output computed values to the CRT or printer.

Two libraries, IRLIB and IRSCRN, comprise the ellipsometric analysis routines. IRSCRN provides the means by which screens are presented to the user and the data are input and verified. These subroutines extensively use the IBM Applications Display Management System (ADMS) to format and display the screens. The library IRLIB contains the general ellipsometric analysis subroutines needed to perform all of the above stated functions. A brief functional description of these two libraries is provided in Appendix A of the MS Thesis "Microcomputer Implementation of a Comprhensive Process Characterization Test Station and Program," by Doug R. Miller, UT Austin, 1988.

When the subprogram IR is entered, all available options are displayed in the IR Options Menu as shown in Figure 4-2. Functions are selected by entering the corresponding number located next to the menu item. The input screens for options 1, 2, 3, 4, and 5 of Figure 4-2 are shown in Figures 4-3, 4-4, 4-5, 4-6, and 4-7 respectively.

Menu items 1 thru 3, when selected, display the appropriate data input screen which requires input of the polarizer and analyzer values. The user has the option of performing a one null analysis, in which only the specification of P1 and A1 are required. The default wave plate retarder characteristics are then used. A two null analysis requires all four values, P1, A1, P2, and A2, by which the quarter wave plate retarder characteristics are

then calculated. The result is then used to calculate Ψ and Δ.

Once the data has been entered, the data analysis is initiated by depressing the F2 function key. The input values are then checked for validity. If an error is detected, a message is displayed on the screen and input is again requested.

The computation of the film thickness and index of refraction (Option 1) begins with calculating the Ψ, Δ, and possibly, the wave plate correction factors. Once Ψ and Δ are determined, an initial guess for the film thickness and index is made using a generated reference table. The secant method is utilized to solve the governing equations. Hence, the values for the film thickness and index are obtained. Convergence is accepted when the imaginary thickness component is .001% that of the real component of the thickness. Results have been verified to five significant digits with published ellipsometric data.

Figure 4-2. Ellipsometric Options Menu Screen

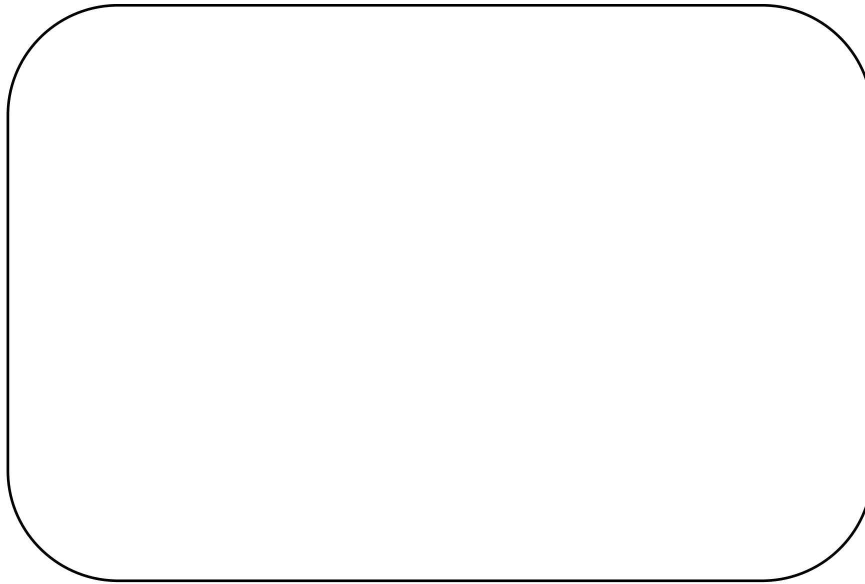


Figure 4-3. Input screen for calculating both the thickness and the index of a lossless film (Option 1).

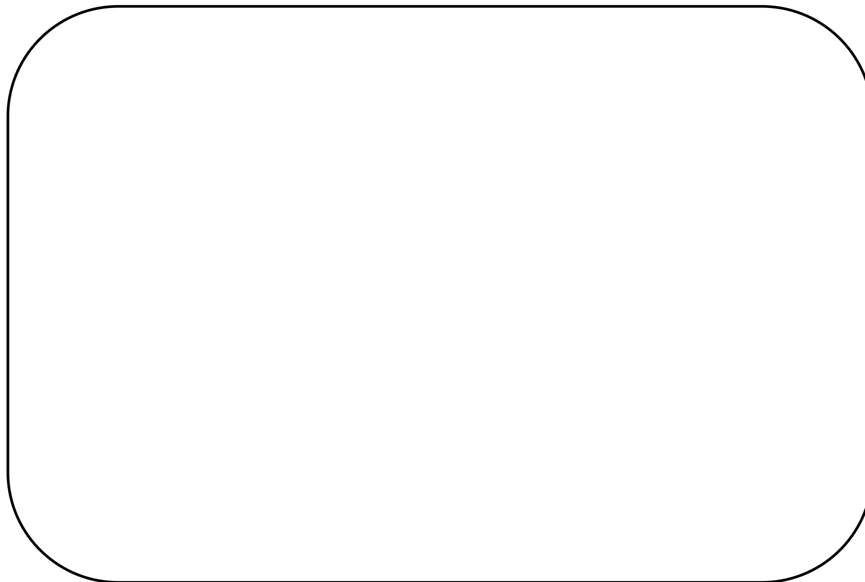


Figure 4-4. Input screen for calculating the thickness given the index of a lossless film (Option 2).

Calculating the thickness of a very thin film (Option 2) and the substrate index (Option 3) are both implementations of analytic expressions as discussed earlier. The associated subroutines are outlined in Appendix A. Results have also been verified using published ellipsometric data.

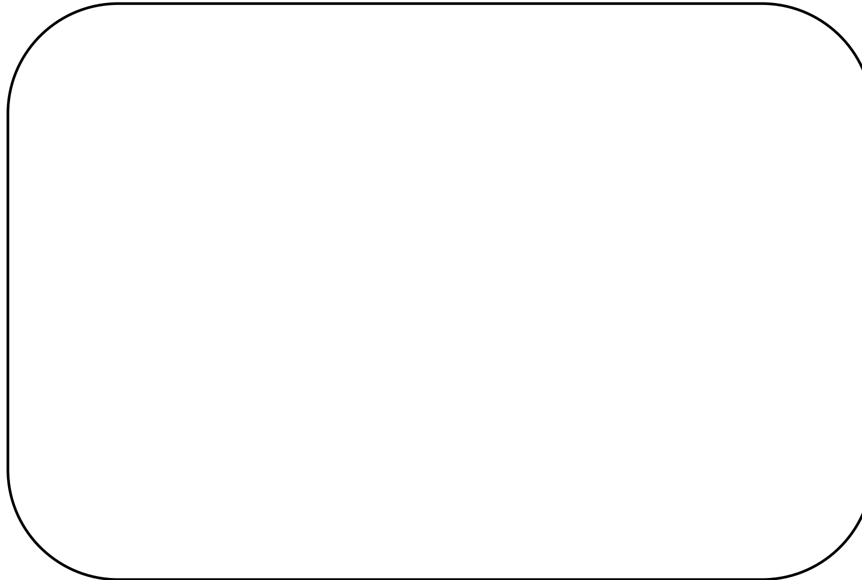


Figure 4-5. Input screen for calculating the complex index of refraction for a substrate (Option 3).

For both Options 1 and 2, a repeat distance of the lossless film is calculated using equation (3-19). From the repeated distance and the computed thickness, results are displayed for nine possible thickness values, all of which would give the same values for P_1, A_1, P_2, and A_2.

Option 4 of the Ellipsometric Options Menu, Change Ellipsometric Parameters, allows the user to conveniently change the default values of the substrate index, the angle of incidence, the wave plate retarder characteristics, and the light source wavelength. The updated parameters are then stored in the system by depressing the F2 function key.

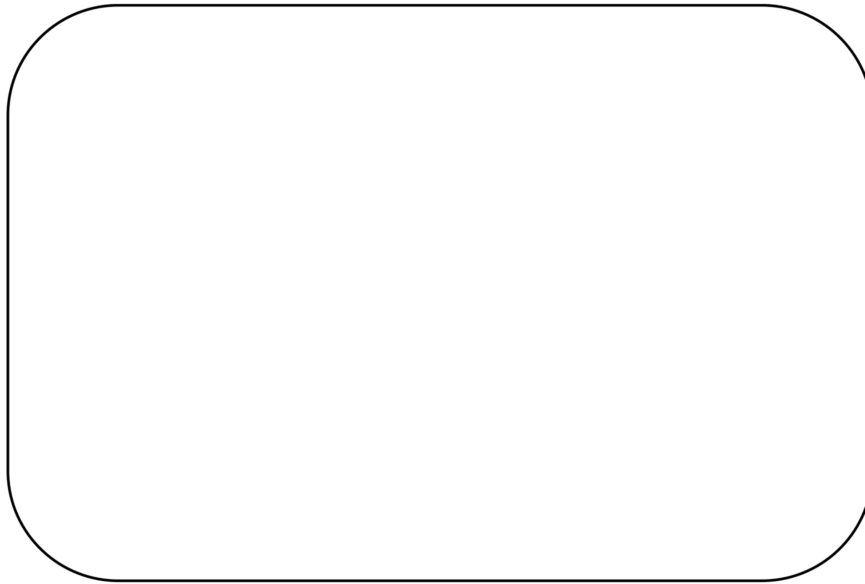


Figure 4-6. Input screen for updating the default ellipsometric parameters (Option 4).

The program also provides an option (Option 5) for printing the Ψ and Δ table of a specified thickness range and complex film index. A sample output of SiO_2 (N_{film}=1.45+i 0) on silicon (N_{sub} = 3.850 - i .02) is shown in Figure 4-8.

Figure 4-7. Input screen used in printing a (Ψ,Δ) versus film thickness table (Option 5).

OP - S: Microscope operation and Line Width Measurements

filename: MCSCRP

We use a variety of microscopes in our lab to allow us to examine the small features made using the photolithography equipment. The primary inspection microscope used is the Nikon metallurgical scope connected to the color video monitor. A Polaroid camera can also be attached to the microscope for photography, but this switch should **only** be performed by a TA. Other instructions related to the use of the microscope are given on the following pages.

The primary tool used to measure line widths is a video micrometer. Once properly calibrated, this instrument can make measurements accurate to about the third significant digit (mainly limited by the resolution of the video scan lines). You will use this instrument to measure photoresist lines, and the resulting etched features, as well as junction groove parameters. The micrometer display is controlled by the joystick; the various menu options are accessed by depressing the red button next to the joystick. Feature measurements are made by positioning the lines displayed on the monitor at the edges of the feature. The actual dimensions are then displayed as the distance between the horizontal lines (the "y" value) and the distance between the vertical lines (the "x" value). In addition, the diagonal length of the rectangle formed by the lines is also displayed (the "d" value). To convert from arbitrary units to microns, a calibration factor is used; the cal set (1 through 4) is displayed as a number after the x, y and d display. **It is critical that the cal set you use matches the objective lens selected on the microscope.** See posted information in lab. Also note that due to image blooming with the CCD camera, the level of illumination affects the apparent image size; thus it is very important to set the illumination so the brightness of the calibration slide and the chip to be measured are approximately the same.

The menu selections you will use the most are described below. To open the menu depress the red button, then use the joystick to move up or down to the menu item desired. Depress the red button again to activate the selection.

Menu Item	Description
SPAN	under joystick control, moves the right and top lines
DATUM	under joystick control, moves the left and bottom lines
BLANK	turns video micrometer display completely off
LINE TYPE	sets either dashed lines or solid lines
MATT	sets line color: joystick up for white, down for black

The other menu items should be used only with the supervision of a TA.

page

IV. Material Safety Data Sheets

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Photoresist	VI-10
HMDS (used in PR adhesion promoter)	VI-12
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Sulfuric Acid	VI-18
Concentrated Hydrofluoric Acid	VI-20
Buffered Hydrofluoric Acid	VI-22
Aluminum Etch, Transene type A	VI-25

Introduction: Material Safety Data Sheets

filename: MSDS

The on-line version of this section contains a (hopefully) useful set of links to some of the vast information related to safety available through the World Wide Web. You can access our page via:

http://weewave.mer.utexas.edu/DPN_files/courses/FabLab/Fab_Lab_Manual/MSDS.html

The University of Texas Environmental Health and Safety Office's main web page can be found at http://www.utexas.edu/business/oehs/ .

This information is provided to help you evaluate the relative hazards involved in handling and working with many of the common chemicals used in the semiconductor fabrication process. As you leave the university and enter the work place you will find the most common way in which such infromation is disseminated is via the Materials Safety Data Sheet, also known as a MSDS. You should be most concerned with Section II: Hazard Data; Section VI: Health Hazard Information; and Section VIII: Special Protection Information.

i) At UT, you can get access to MSDSs via the web at http://msds.lib.utexas.edu/.
ii) A good web site on MSDSs is provide by Interactive Learning Paradigms, Incorporated: http://www.ilpi.com/msds/index.chtml#What .
7) A good FAQ on MSDSs can be found at http://www.ilpi.com/msds/msdsfaq.chtml .
iii) A wide collection of safety-related links can be found at http://www.utexas.edu/business/oehs/main/links.html .

As an example, look at the MSDS for automotive gasoline shown on the next two pages (pp. VI-2 and VI-3 or via the WWW at http://msds.lib.utexas.edu/n2c?urn:utlol:msds.mdl.OHS33841 .

Note in Section II the column labeled "Hazard Data": here you will find the statement

"8-hr TWA 300 ppm or 900 mg/m^3"

The abbreviations used refer to the **TLV**:

> Threshold Limit Value, the term used by the American Conference of Governmental Industrial Hygienists Inc. (ACGIH), to express airborne concentration of a material to which nearly all persons can be exposed day after day without adverse effects.

In conjunction with the TLV, several sub-definitions are used:

TWA: time-weighted average concentration for a normal 8-hour workday or 40-hour week.

STEL: short-term exposure limit, the maximum concentration for continuous short exposure.

TLV-C: Ceiling exposure limit, the concentration that should never be exceeded even instantaneously.

Thus the MSDS for gasoline tells us that over the course of an 8-hour work day exposure to gasoline should not exceed more than 300 parts per million (ppm). Also note this same information, with details on specific health hazards, is given on p. VI-3 in Section VI: Health Hazard Information.

Further abreviations can be found at http://www.utexas.edu/business/oehs/resources/msdsgloss1.html .

When followed properly, the laboratory procedures described in this manual, along with established laboratory practices outlined in class, should keep exposure to the chemicals we use to levels less than the TLV's given in the MSD Sheets.

V. Data Sheets

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Buffer - HF IV-2
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PR Stripper IV-9
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Miscellaneous equipment sheets

VI. Physical Constants

Resistivity vs. Doping V-1
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