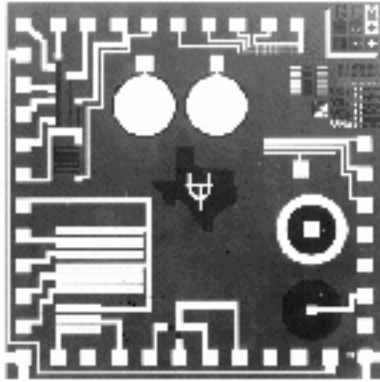


IC Fab Lab Manual

Copyright 1999 by Dean P. Neikirk

The University of Texas at Austin

Microelectronics Fabrication Teaching Laboratory
Laboratory Manual



Spring, 1985

Rev 1: Fall, 1985; Rev 2: Spring, 1986; Rev 3: Fall, 1986;
Rev. 4: Spring, 1987; Rev 5 Fall, 1987; Rev 6 Fall, 1988;
Rev. 7 Fall 1989; Rev. 8 Spring 1990; Rev. 10 Fall 1990;
Rev. 11 Fall 1991; Rev. 12 Fall 1993; rev. 13 Fall 1996;
Rev. 14 Fall 1997; Rev. 15 Fall 1998; Rev. 16 Fall 1999

by

Dean P. Neikirk

Department of Electrical and Computer Engineering
University of Texas at Austin
Austin, TX 78712-1084 USA
tel (512)471-4669 or 471-8549
web: <http://weewave.mer.utexas.edu>

Preface

The Microelectronics Fabrication Laboratory has now been in operation here at UT for almost fifteen years; even so, it is still a lab course which requires constant updating. This course has a number of objectives, chief among them your exposure to basic silicon device processing. You will be required to make use of information from many areas: solid state physics, chemistry, electrical engineering, and computer science. Regardless of your future intentions, we feel the material covered in lecture, and your experiences in the lab, will be very valuable. The use of integrated circuits is pervasive, and knowledge of how they are made is an important compliment to your knowledge of how they can be used.

This laboratory is a synthesis of the work of a number of people. Similar laboratories at Caltech (under the supervision of Prof. Jim McCaldin and Prof. David Rutledge) and at the University of Illinois (originally developed by Prof. Ben Streetman) have provided both inspiration and guidance. Industrial support has been provided by Bell Laboratories, Advanced Micro Devices, Motorola, and Texas Instruments. Both TI and Monsanto have provided silicon wafers for our use. The Semiconductor Research Corporation has also provided generous support for the development of our new mask set. The technical staff (under the supervision of Mr. Harold Traxler and Marty Ringuette) has provided invaluable assistance in setting up and maintaining the lab equipment. The help of Philip Cheung, Doug Miller, Jeff Meitz, Stu Wentworth, Carl Kyono, Doug Holberg, and Garrett Neaves in designing the experiments is also gratefully acknowledged.

This lab is quite different from any other of the labs in your ECE curriculum. The processing we do is very complicated, and there will be frequent, and often very subtle, problems associated with it. You must be very patient and **methodical** at all times. Since we have essentially only one set of equipment, you must also be very careful. Please feel free to make suggestions that you think will help improve the lab.

Updates to this manual are made as necessary; make sure to check the World Wide Web version of the lab manual at:

http://weewave.mer.utexas.edu/DPN_files/courses/FabLab/Fab_Lab_Manual/TOC.html

Dean Neikirk
Fall, 1999

Table of Contents

IC FAB LAB MANUAL	1
MICROELECTRONICS FABRICATION TEACHING LABORATORY LABORATORY MANUAL.....	II
PREFACE.....	III
TABLE OF CONTENTS.....	IV
I. INTRODUCTION: LAB RULES.....	7
FILENAME: INTRO.....	7
A. LABORATORY NOTEBOOKS AND REPORTS.....	7
B. GRADING	9
C. SAFETY	10
II. EXPERIMENTS: SINGLE DIFFUSED DEVICE FABRICATION.....	12
FILENAME: FABINT	12
INTRODUCTION	12
PROCESS FLOW SUMMARY	16
LAB SCHEDULE.....	18
PROCESSING DESCRIPTION	19
LABORATORY REPORT GUIDELINES	32
HOLBERG MASK SET	41
TROUBLE SHOOTING DURING DEVICE TESTING	56
DEVICE TESTING	63
III. OPERATING PROCEDURES	74
PAGE	74
OP-A: OPERATION OF HIGH TEMPERATURE FURNACES.....	75
OP-B WET OXIDATION	79
OP-C: DRY OXIDATION AND CHLORINE OXIDATION OF SILICON.....	83
OP-D: BORON PREDEPOSITION	86
OP-E: PHOSPHORUS PRE-DEPOSITION.....	91
OP-F: DRIVE IN FURNACE AND DIFFUSION PROCESSING.....	93
OP- G: VACUUM SYSTEMS AND VACUUM EVAPORATION.....	102
OP-H: MEASUREMENT OF SEMICONDUCTOR RESISTIVITY USING A FOUR POINT PROBE.....	109
OP-J: WAFER CLEANING.....	115
OP-K: PLASMA ASHING	117
OP-L: PHOTOLITHOGRAPHY.....	121
OP-M: INTRODUCTION TO CAPACITANCE MEASUREMENTS	127
OP-N: JUNCTION DEPTH MEASUREMENTS	132
OP-O: MASK ALIGNMENT AND THE MICROTECH MASK ALIGNERS	134
OP-P: HYDROFLUORIC ACID ETCHING.....	140
OP-Q: TEKTRONIX CURVE TRACER	143
OP-R: OPTICAL THIN FILM MEASUREMENT.....	157
OP - S: MICROSCOPE OPERATION AND LINE WIDTH MEASUREMENTS	190
IV. MATERIAL SAFETY DATA SHEETS.....	192
INTRODUCTION: MATERIAL SAFETY DATA SHEETS	193
V. DATA SHEETS	195
VI. PHYSICAL CONSTANTS.....	195

Figures

FIGURE 1: COMPOSITE DRAWING OF HOLBERG MASK SET.	44
FIGURE 2: HOLBERG MASK LEVEL 1, DIFFUSION.....	45
FIGURE 3: HOLBERG MASK LEVEL 2, GATE.	46
FIGURE 4: HOLBERG MASK LEVEL 3, CONTACTS.	47
FIGURE 5: HOLBERG MASK LEVEL 4, METAL.	48
FIGURE 6: SCANNED IMAGES OF THE HOLBERG MASKS	49
FIGURE 7: COMPOSITE VIEW OF ALIGNMENT AND REGISTRATION PATTERNS OF HOLBERG MASK SET; ALL FOUR LEVELS ARE SHOWN SUPERIMPOSED. THE SCALE BAR IS 50 μm LONG.	50
FIGURE 8: ILLUSTRATION OF Y-AXIS MISREGISTRATION VERNIERS. THREE CASES ARE SHOWN: ZERO, +1, AND -1 μm MISREGISTRATION.	51
FIGURE 9: ILLUSTRATION OF X-AXIS MISREGISTRATION VERNIERS. THREE CASES ARE SHOWN: ZERO, +1, AND -1 μm MISREGISTRATION.	52
FIGURE 10: RESOLUTION BARS. SEE TABLE 7 FOR DIMENSIONS.	53
FIGURE 11: COMPOSITE VIEW OF RESISTOR PATTERNS OF HOLBERG MASK SET; FOUR LEVELS ARE SHOWN SUPERIMPOSED: DIFFUSION: LEVEL 1; DIFFUSION: LEVEL 2; CONTACT: LEVEL 3; AND METAL: LEVEL 4.	54
FIGURE 12: COMPOSITE VIEW OF MOSFET PATTERNS OF HOLBERG MASK SET; ALL FOUR LEVELS ARE SHOWN SUPERIMPOSED.	55
FIGURE 13: MOSFET SUB-COMPONENTS.....	58
FIGURE 14: I-V PARAMETERS FOR DIFFUSED DIODE	65
FIGURE 15: CROSS-SECTION OF A ROTAMER TYPE FLOW METER.....	75
FIGURE 16: 3-ZONE RESISTANCE HEATED FURNACE.	76
FIGURE 17: BORON CONCENTRATION AFTER PRE-DEP.	86
FIGURE 18: SHEET RESISTANCE VS. BORON PRE-DEP TIME.	88
FIGURE 19: SHEET RESISTANCE VS. PHOSPHORUS PRE-DEP TIME.	91
FIGURE 20: COMPARISON OF CONSTANT AND LIMITED SOURCE DIFFUSION PROFILES.....	95
FIGURE 22: NORMALIZED ERFC AND GAUSSIAN CURVES.	95
FIGURE 23: IRVIN CURVE FOR N-TYPE IMPURITY, ERFC PROFILE.....	96
FIGURE 24: IRVIN CURVE FOR N-TYPE IMPURITY, GAUSSIAN PROFILE.	97
FIGURE 25: IRVIN CURVE FOR P-TYPE IMPURITY, ERFC PROFILE.	98
FIGURE 26: IRVIN CURVE FOR P-TYPE IMPURITY, GAUSSIAN PROFILE.	99
FIGURE 27: ROTATING-VANE TWO-STAGE ROUGH PUMP (FROM J. O'HANLON, <i>A USER'S GUIDED TO VACUUM TECHNOLOGY</i> . NEW YORK: JOHN WILEY & SONS, 1980, p. 161).....	102
FIGURE 29: OIL DIFFUSION PUMP	103
FIGURE 28: THERMOCOUPLE GAUGE.	104
FIGURE 30: BAYARD-ALPERT IONIZATION GAUGE . ADAPTED FROM J. O'HANLON, <i>A USER'S GUIDED TO VACUUM TECHNOLOGY</i> . NEW YORK: JOHN WILEY & SONS, 1980, p. 63.	104
FIGURE 33: VARIAN VACUUM EVAPORATION SYSTEM USED IN OUR LAB.....	105
FIGURE 32: RESISTANCE HEATED EVAPORATION SOURCES.....	105
FIGURE 33: FOUR POINT PROBE; SAMPLE DIMENSIONS AND ORIENTATION OF PROBE REFER TO TABLE 13.	109
FIGURE 34: PLASMOD CONTROLS AND INDICATORS.....	118
FIGURE 35: BASIC LITHOGRAPHIC PROCESS (ADAPTED FROM INTRODUCTION TO MICROLITHOGRAPHY, THOMPSON ET AL)	122
FIGURE 36: P-N JUNCTION CAPACITANCE	127
FIGURE 37	129
FIGURE 38: JUNCTION SECTIONING GEOMETRY.	132
FIGURE 39: SCHEMATIC DIAGRAM OF THE MICROTECH MASK ALIGNER	136
FIGURE 40: TOP VIEW OF BHF ETCH STATION.	140
FIGURE 41: PLUMBING DIAGRAM FOR BHF ETCH STATION.	141
FIGURE 42: FRONT PANEL OF TEKTRONIX 577 CURVE TRACER	148
FIGURE 43: SINGLE INTERFACE REFLECTION.	158
FIGURE 44: MULTI-INTERFACE REFLECTIONS.....	159
FIGURE 45: SAMPLE REFLECTANCE TRACE.....	160
FIGURE 46: FILMETRICS SYSTEM.....	161

FIGURE 47: MAIN FILMETRICS DATA ANALYSIS WINDOW	162
FIGURE 48: FILMEASURE MAIN WINDOW:.....	163
FIGURE 49: EDIT STRUCTURE WINDOW	164
FIGURE 50: EXAMPLE EDIT STRUCTURE:LAYERS WINDOW FOR MEASURING THE THICKNESS, n , AND k OF FILMS ON AN OPAQUE SUBSTRATE.....	165
FIGURE 51: EXAMPLE EDIT STRUCTURE:OPTIONS WINDOW FOR MEASURING THE THICKNESS, n , AND k OF FILMS ON AN OPAQUE SUBSTRATE.....	166
FIGURE 52: MEASURED AND CALCULATED REFLECTANCE SPECTRA WHEN MEASURING THE THICKNESS, n , k , AND ROUGHNESS OF SiO_2 ON SILICON.....	167
FIGURE 53: CALCULATED n AND k SPECTRA WHEN MEASURING THE THICKNESS, n , k , AND ROUGHNESS OF SiO_2 ON SILICON.	168
FIGURE 54: MAIN COMPONENTS OF AN ELLIPSOMETER.	170
FIGURE 55: GAERTNER L117 ELLIPSOMETER	171
FIGURE 56: THICKNESS PERIODS FOR SILICON.....	175

Tables

TABLE 1: n -TYPE MPT CHIPS OXIDE THICKNESS MEASUREMENTS.....	37
TABLE 2: p -TYPE MPT CHIPS OXIDE THICKNESS MEASUREMENTS.....	37
TABLE 3: SHEET RESISTANCE MEASUREMENTS SUMMARIES	38
TABLE 4: UNDOPED WAFER CHARACTERIZATION.....	38
TABLE 5: LITHOGRAPHY AND ETCH RESULTS	39
TABLE 6: MOS DEVICE CHARACTERIZATION	40
TABLE 7: RESOLUTION BARS	43
TABLE 8: TROUBLE SHOOTING CHECKLIST	60
TABLE 9: DIODE CHECKLIST.....	60
TABLE 10: FURNACE GAS FLOW RATES	77
TABLE 11: FURNACE CONTROLLER SETTINGS.....	78
TABLE 12: COLOR CHART FOR THERMALLY GROWN SiO_2 FILMS OBSERVED PERPENDICULARLY UNDER DAYLIGHT FLUORESCENT LIGHTING (ADAPTED FROM GHANDHI)	82
TABLE 13: DIAMETER CORRECTION FACTOR CF_D (AFTER REF. 2).....	113
TABLE 15: THICKNESS CORRECTION FACTOR (AFTER REF. 1).....	113
TABLE 16: 4 POINT PROBE CURRENT SETTINGS (AFTER REF. 3).....	114
TABLE 17: FUNCTIONS OF CONTROLS AND CONNECTORS FOR TEKTRONIX MODEL 577 CURVE TRACER	149
TABLE 18: TEKTRONIX CURVE TRACER GATE BIAS POLARITY TABLE.....	155
TABLE 19: ELLIPSOMETRIC PARAMETERS Ψ/Δ VERSUS THICKNESS & INDEX.....	176