

# I. Introduction: Lab Rules

filename: INTRO

## A. Laboratory Notebooks and Reports

One important objective of this laboratory is learning how to keep a good lab notebook. You have undoubtedly been told in your other lab courses the importance of keeping an accurate (and comprehensive) account of your work, but I cannot possibly overstate this point. Anyone who works in research and development must keep a complete notebook: many of the companies you may someday work for will in fact require this, and will keep possession of the notebook. Many patent decisions have been based on the worker's lab notebook (or lack of it). Your notebook should be like a diary, recording what you do, and why you did it. Especially in I.C. processing, you should feel free to speculate as to the causes of process failures, of which there will be many. You will frequently learn more from these failures, and your attempts to correct them, than from a process that works perfectly the first time. *It is crucial, however, that your notebook accurately records everything you did.* A good test of your work is the following question: could someone else, versed only in the general processing arts, use your notebook to repeat your work, and obtain the same results? For that matter, could you come back six months later, read your notes, and make sense of them? If you can answer yes to these two questions, you are keeping a good notebook.

To make things easier, you **must** buy a specific lab notebook for this class. This is a duplicate notebook with carbon paper; at the end of each lab you will be required to tear out the duplicate pages and turn them in to the TA for grading. The Co-Op has these notebooks. Your notebook should be neat, but informal. There is no need to copy information from this lab manual into your notebook, except as it reflects what you do. Put in notes on procedures, why you do things, what you observe, and speculations and conclusions. The following rules apply to your notebook:

1. Everything must be written in INK.
2. **Date** every page as you record your work.
3. All data and notes must go **DIRECTLY INTO THE NOTEBOOK**. The duplicate pages will be collected at the end of each lab period. **LOOSE LEAF SHEETS OR SCRAP PAPER SHOULD NEVER BE USED, AND WILL NOT BE ACCEPTED.**
4. Label all graphs and tables.
5. Write only on one side of each page. All writing should be **LEGIBLE**. Leave room for comments by the TA.
6. Each student must keep her/his own lab notebook.
7. If a particular experiment has pre-lab questions, you **must complete them before the lab period begins**. Record your answers in the lab notebook.

The TA's will deduct 5 points from your score if these rules are not strictly adhered to.

## Laboratory Reports

## SEE UPDATES IN REPORT SECTION

In addition to your lab notebook, after completion of certain stages in the device processing sequence (this will often take several lab periods) you must submit a **Lab Report**. The Lab Report should be typed; it is similar to your Senior Lab technical memos, but not as formal. The Lab Report should contain the following:

- 1) Experiment title, dates performed, and your lab partner's name.
- 2) Summary of experimental objectives.
- 3) Experimental processing procedure: **DO NOT SIMPLY RECOPY THE CONTENTS OF THIS LAB MANUAL.** A very short summary of important points is sufficient, with emphasis on any changes to the process given in the Lab Manual. You should attempt to explain the reasons any process changes were made, as well as any unusual results in the actual processing. **Normally this section should not exceed about two pages, and may be shorter in later lab reports.**
- 4) Data: present a summary of the measurements made during the process (originally recorded in your lab notebook) in a **concise, tabular** form. Make sure you do not give numbers to any more than the **proper number of significant digits**. Reference the page numbers in your notebook from which you obtained the raw data. Include sample calculations where necessary. Make clear the estimated accuracy of your measurements.
- 5) Answers to any specific questions and problems given in the lab manual. Specify any graphs or tables from the lab manual or text book used. Write out any equations used in calculations (but not algebraic details).
- 6) Brief comments on experimental results. Point out any unusual problems or experimental observations, and explain them if you can.

Further information will be discussed in class.

SEE LAB REPORT GUIDELINES following the Processing Description, p. Reports - 1.

## B. Grading

A significant portion of your course grade is your lab grade. Each lab is worth ten points; each Lab Report is worth another fifty points. Grades will be based on the following:

- 1) **Be present at each lab ON TIME.** This is VERY important. Tardiness will be penalized. Lab work, even more than lectures or homework, cannot be made up in a last-minute rush. Results in the fabrication lab come slowly, and you will need every minute available to you. Arrangements may be made to make up missed lab periods if you have an EXCELLENT excuse.
- 2) **Be prepared before you come to lab.** There will be assigned readings from the lab manual for each experiment. You MUST COMPLETE these BEFORE coming to lab, since they explain the operating procedures for the equipment you will be using. We may occasionally give lab quizzes over this material, and it will be fair game for the course exams.
- 3) Keep a complete lab notebook, and answer any pre-lab questions there may be in the experimental description.
- 4) Lab Reports are due one lab period after you complete the experiment. Unless you have an excellent excuse, late reports will be derated by ten points per week they are late. See the Lab Schedule for due dates.

The lab TA's will take any equipment problems into account when grading your lab work.

ONE FINAL WARNING: I take this lab very seriously, and will STRICTLY enforce all the rules stated in this manual. Whatever you do, don't tell me you didn't know simply because you failed to **read this manual carefully**. Woe will indeed be unto you in those circumstances.

### Policy on CHEATING:

It is expected that you will discuss your experimental procedures and results with each other; you are, however, responsible for doing your own written work. All lab notes and Lab Reports should be your own ORIGINAL WORK. If you transpose data collected by your lab partner you should acknowledge this fact in writing, as if this was a reference.

ANY EVIDENCE OF PLAGIARISM OR CHEATING WILL BE TREATED AS GROUNDS FOR FAILURE OF THE COURSE.

## C. Safety

We have done everything we can to make this laboratory as safe as possible; we cannot, however, completely protect you without your cooperation. There are very hot furnaces, powerful acids, and strong solvents which are all used, so you must be careful. If you do not show sufficient regard for safety, you will be told to leave the lab, and your grade will suffer accordingly. This section of the lab manual is intended to give some general guidelines, but the most important item is your COMMON SENSE.

THE UNIVERSITY OF TEXAS AT AUSTIN'S LAB SAFETY MANUAL  
YOU SHOULD ALSO REFER TO THE MANUAL FOUND ON LINE AT:  
<http://www.utexas.edu/business/oehs/resources/labman/>

OTHER UPDATES TO THIS SECTION CAN BE FOUND ON-LINE AT:

[http://weewave.mer.utexas.edu/DPN\\_files/courses/FabLab/Fab\\_Lab\\_Manual/SAFETY.html](http://weewave.mer.utexas.edu/DPN_files/courses/FabLab/Fab_Lab_Manual/SAFETY.html)

--Wear glasses whenever you are in the laboratory.

If you do not ordinarily wear glasses, get a pair of safety glasses from the apparel cabinet when you put on your lab coat.

--**Never** wear shorts or open shoes to this lab. You must always wear long pants and regular shoes when you work in this lab to help insure your safety.

--Keep all the chemicals, whether in beakers or bottles, under the hoods at all times.

Before beginning any work, make sure the water is running in the sink and leave it running at all times. Whenever working under the hoods you should wear the green acid/solvent resistant gloves over your normal gloves. When you finish, rinse the gloves in running water, then remove them, and finally rinse your normal gloves. If you think any liquid has penetrated the gloves, remove them and thoroughly wash your hands. The large sink in the lithography room is more convenient for rinsing your arms than the fume hood sink.

--**Never mix an organic solvent with an acid:** the combination may explode.

Always rinse chips with high purity water between etching steps and solvent cleaning steps. Acids should be diluted with water in a large beaker, and then poured down the drain very slowly, with the sink water running. Solvents such as ethanol may be poured down the drain with water dilution. **Acetone should NOT be poured into the city drains.**

### **HYDROFLUORIC ACID**

We use a 10% hydrofluoric (HF) acid mixture for etching SiO<sub>2</sub>. HF is **EXTREMELY DANGEROUS**, and we use it **ONLY IN THE HF ETCHING HOOD. AT NO TIME**

**IS ANY OTHER PROCESSING TO BE DONE IN THIS HOOD.** One major problem with HF is the fact that it does not hurt immediately after exposure. When it does begin to hurt a few hours after exposure, it is too late. It will slowly eat through tissue over the course of several days, until it reaches bone, where it is neutralized by calcium. It is excruciatingly painful.

Although an HF burn is very serious, it is also very easy to prevent. Only when the acid is left in contact with the skin for an extended period is it dangerous. Our procedure is very simple: always wear the green gloves when working at the HF etch station, and rinse them with water frequently. When you finish, rinse thoroughly, and finally rinse your hands and arms. The etch station itself is designed to minimize the chance of exposure, but always be VERY CAREFUL. I have never seen a serious HF accident, but this is only because all the labs I have worked in treat it with healthy paranoia. Please do not break my record.

If an accident does occur, there is both a safety shower and eyewash next to the main door. For any chemical splash onto a person's face, they should immediately go to the eyewash and activate it. You should put your face into the water stream and rinse for at least several minutes. For whole body splashes, pull down on the safety shower handle, and leave the water on. A non-injured person should use the phone next to the spill kit to call for emergency help if necessary:

**DIAL 9911 FOR EMERGENCY HELP.**

**TELL THE OPERATOR YOU ARE LOCATED AT THE UNIVERSITY OF TEXAS IN ENGINEERING SCIENCES BUILDING ROOM 214**

**NOTIFY ME AT ONCE IN CASE OF ANY ACCIDENT.**

**Please see the Materials Safety Data Sheets (MSDS) in Section IV (p. 192) of this Lab Manual for more information.**

## II. Experiments: Single Diffused Device Fabrication

**filename: FABINT**

### Introduction

In order that you may understand the flexibility which planar technology affords the circuit designer, we have designed a set of test masks (the Holberg Masks, see p. Masks-1) for use in this lab. This mask set contains device test structures, resolution bars, and alignment verniers. The devices fabricated include several MOS transistors, as well as diodes and MOS capacitors. We will also check diffused resistors, metal step coverage, and metal and contact resistance. In addition to the device chips, we will process, in parallel, unpatterned test chips. These samples will allow us to make several measurements we could not make on our device arrays. You will start with four chips, two identical n-type samples and two identical p-type samples. You will pattern one each of the n-type and p-type chips, as described below, to make your device arrays. The remaining two chips will serve as materials properties test (MPT) samples allowing you to determine such properties as oxide thickness, doping concentration, sheet resistance, and junction depth. Several of these measurements would be destructive or not possible on the patterned device array chips. This is why we process the MPT samples in parallel with the device samples.

### Processing Description: Device Array Chips

Starting with an oxidized wafer, a pattern will be etched through the oxide using Mask Level 1 (p. Masks-5) and the Photo-Resist (PR) process outline in OP-L for use with the Positive Resist. The wafer will then be subjected to a boron or phosphorus ambient at high temperature so that the dopant will diffuse into the silicon through the holes in the oxide, forming doped regions on the wafer in those areas delineated by Mask 1. This diffusion is known as the predeposition or "predep" diffusion (see OP-D and OP-E). The rear surface of the wafer will be protected with oxide in this diffusion. We will use both n-type and p-type substrates to facilitate comparisons of device characteristics during the testing phase of the experiment.

After the wafer has been suitably cleaned, it will then be subjected to another diffusion, called the redistribution or "drive" diffusion, this time without the dopant source. The idea here is to redistribute the dopant such that its concentration is more uniform. This diffusion will be initiated in an oxygen atmosphere so that another layer of oxide is grown simultaneously on the wafer to protect the doped regions. See OP-F.

The next step in our wafer fabrication will use a second photoresist (PR) process using Mask Level 2 (labeled **G** for "gate" in the upper right corner of the mask), p. Masks-6, to delineate areas for growth of a high quality gate oxide. After resist processing, a buffered HF (BHF) etch will completely remove previously grown oxides, leaving a clean silicon

surface over the gate region of our MOSFET and over our MOS capacitors. The resist will then be cleaned off, and the Dry Oxide Furnace used to grow a thin, high quality oxide. We will perform these gate oxide growths with chlorine injection to improve the quality of the gate oxide.

After gate oxide growth, a third PR process using Mask Level 3 (labeled **C** for "contact" in the upper right corner of the mask), p. Masks-7, will be used to cut holes down to the doped regions in the silicon, through which contacts can be made. Aluminum will then be vacuum evaporated over the entire wafer, and a 4th PR process utilized to etch the contact pattern using Mask 4 (labeled **M** for "metal" in the upper right corner of the mask), p. Masks-8.

Once the front metalization pattern is etched, aluminum will be evaporated onto the backside of the chip to help form the substrate contact. Before metalization we damage the back with sandpaper to help insure an ohmic contact will be formed (strictly speaking, the damage will insure that any Schottky diode formed between the aluminum and the silicon will be very leaky).]

Finally, you will form the ohmic Al-Si contacts by annealing. This is a process in which the components of a system are heated to a temperature below the system's eutectic point. (The melting point of a given alloy of one substance in another depends upon the percentages of the materials present. That point on a phase diagram of temperature vs. percent of each parent material present where a temperature minimum occurs in the liquidus line is known as the eutectic point.) The eutectic point for the Al-Si system is 576°C. You will use a temperature of 450° which permits the aluminum atoms to move around and spread more uniformly over the silicon surface. In addition, during annealing, the aluminum can diffuse into the silicon itself. This will ensure low resistance contacts to the silicon devices.

This concludes the device processing.

## Processing Description: Materials Properties Test Chips

Starting with the oxidized wafers, the ellipsometer is used (see OP-R) to measure the initial field oxide thickness. After measurement, a simple pattern is etched through the oxide. This pattern will simply uncover one-half of the MPT samples. A predep (at the same time as your device chips) is then performed. We can now measure the sheet resistance of the predep layer using the four-point probe (see OP-H). Note this allows you to infer the sheet resistance of the doped regions on your device chips.

After cleaning, we will subject the MPT samples to a drive-in diffusion (again, at the same time as the device samples). After the drive, the oxide thickness grown during the drive is measured, then completely etched away in buffered HF. You will now be able to measure the sheet resistance of the doped layer (note it will not be the same as it was after the predep), as well as the resistivity of the wafer substrate (by measuring on the half of

the substrate that was covered with oxide during the predep). Again, this will give you information about certain areas on your device chips at this point in the process.

The last high temperature process step performed on your samples is the gate oxide growth step. The oxide-free MPT samples will be included with your device chips during the TCE dry oxidation (see OP-C). After completion, you will measure the oxide thickness grown on the MPT chips; this will give you the gate oxide thickness on your device samples. We will also use a technique called junction grooving (see OP-N and Gandhi, pp 196-197 (1st edition)) to find the depth of the p-n junctions below the wafer surface. Note this step is destructive, requiring the grinding of a groove in the surface of your MPT samples. If possible, after determining the junction depth, you will etch all oxide off the MPT chips so that the sheet resistance of the doped layers can be measured again. This is necessary since the dopants will have diffused during the high temperature gate oxidation. Note that based on the measurements made on your MPT samples, you will now have all the materials properties necessary to analyze the devices on your patterned device chips.

## General Comments

In order to complete all the processing required, you must keep up with the schedule on pp. F\_int-5-7. In particular, there are three steps that will be batch processed, with everyone's chips together: process step 5, lab 4, the predep process; process step 7, lab 5, the drive-in process; and process step 11, lab 7, the gate oxidation process. **You MUST have all necessary processing and measurements done before each of these steps so that you samples are ready for the batch process.** Catch-up lab periods (outside of normal lab times) will be held before each of these critical steps to allow you extra processing time, if necessary.

**Before coming to each lab read the appropriate Processing Description, and any operating procedures used in that section.** Answer any pre-lab questions assigned. Use the checklist in the Processing Description at all times to ensure that each step is completed. Do not use the checklist as a substitute for reading and understanding all procedures and instructions **BEFORE** lab begins.

Because of limited equipment and space, different groups will do different portions of a process at different times. In particular, some groups will be making measurements on the MPT samples while others are processing their device chips. For example, during lab period 5 two groups will be using the ellipsometer and 4-point probes on their MPT samples, while the other two groups will be performing the 2nd photoresist process (process step 8) on their device chips. In lab 6 these groups will reverse roles.

**Always consult your lab TA at the beginning of the lab period for updated processing instructions.** Check with the TA if any mistakes are made in processing or if



you do not complete the procedure outlined for that period. Please be considerate of the other groups in the lab, and do not monopolize the processing equipment.

## Process Flow Summary

Process Step	Device Chip	Materials Properties Test Chip
<u>Lab 2 &amp; 3</u>	on one p-type, one n-type pre-oxidized chip	on one p-type, one n-type pre-oxidized chip
1		ellipsometric oxide thickness measurement
2	Photoresist 1: diffusion, Holberg Mask Level 1	Photoresist 1: half mask
3	Etch 1st diffusion windows	Etch oxide from half of chip
4	Strip all resist	Strip all resist
<u>Lab 4</u>		
5	p-type sample: phosphorus predep, 20 min n-type sample: boron predep, 30 min	p-type sample: phosphorus predep, 20 min n-type sample: boron predep, 30 min
6	Strip boro/phospho-silicate glass in BHF	Same as device chips; 4-point probe for sheet R
<u>Lab 5 &amp; 6</u>		
7	Both p- & n-type: drive-in, 1100°C, 30 min.	Same as device chips; after drive: oxide thickness
8	PR 2: gate ox pattern, Holberg Mask Level 2	NA
9	BHF oxide etch	Same as device chips; 4-point probe for sheet R
10	Strip PR	NA

(Process Flow Summary cont.)

Process Step	Device Chip	Materials Properties Test Chip
<u>Lab 7 &amp; 8</u>		
11	Gate oxidation: 1100°C, with TCE	Same as device chip; after ox: oxide thickness
12	PR 3: contact windows, Holberg Mask Level 3	NA
13	BHF oxide etch	same as device chip; 4-pt probe for final $R_s$ ; junction groove for $x_j$
<u>Lab 9-11</u>		
14	Backside damage	
15	Strip PR	
16	Front side Al evaporation	
17	PR 4: Metal contacts, Holberg Mask Level 4	
18	Aluminum contact etch	
19	Strip PR	
20	Backside metallization	
21	Form contacts	

## Lab Schedule

filename: fall\_lab\_schd

<u>Week of</u>	<u>Lab</u>	<u>Topic</u>
Aug. 30	1	Intro to Safety and Facilities
<b>Sept. 8</b>		<b>Lab Report O DUE IN LECTURE!!</b>
Sept. 6	2	Group A: oxide thickness;
Sept. 13	3	1st PR; etching
		Group B: 1st PR: diffusion; etching oxide thickness
Sept. 16-17		Catch-up lab; must be ready for lab 4
Sept. 17-20		<b>Batch process: Pre-dep; Process Step 5</b>
Sept. 20	4	etch; 4-pt probe
Sept. 23-24		Catch up lab; must be ready for lab 5
Sept. 24-27		<b>Batch process: Drive-in; Process Step 7a</b>
Sept. 27	5	Group A: oxide thickness; etch; 4-pt probe
Oct. 4	6	2nd PR: gate mask; etching
Oct. 7-8		Catch up lab: must be ready for lab 7
Oct. 8-11		<b>Batch process: Gate-ox; Process Step 11c</b>
Oct. 18		<b>LAB REPORT I DUE Monday Oct. 18 IN LECTURE!</b>
Oct. 11	7	Group A: oxide thickness; junction depth
Oct. 18	8	3rd PR: contact windows
Oct. 25	9	etch windows; front side evap.; 4th PR
Nov. 1	10	front side Al evap., 4th PR cont.; Al etch; backside Al evaporation
Nov. 8	11	4th PR, Al etch cont., backside evap cont.; Al anneals
Nov. 11-12		Catch up lab: must have device fab complete
Nov. 15		<b>LAB REPORT II DUE MONDAY Nov. 15 IN LECTURE!!</b>
Nov. 15	12	Electrical Testing
Nov. 22	13	Electrical Testing
Nov. 29	14	Electrical Testing
Dec. 3		<b>FINAL LAB REPORT III DUE FRIDAY</b>
CLASSES END Fri. Dec. 3		
REPORTS DUE:		
		Oct. 18: Lab Report I, Process and results to date
		Nov. 15: Lab Report II, Complete process summary
		Dec. 3: Lab Report III, Final test results

## Processing Description

filename: PROCESS

Device and Materials Properties Test (MPT) Chips  
Processing Description

MOSFET/CAPACITOR/DIODE/DIFFUSED RESISTOR FABRICATION

### Lab 2 and 3: First Photoresist, Diffusion Mask

Required reading: pp. 7 - 43, , OP-L, OP-O, OP-R

1. Obtain (two each) clean, oxidized n- and p-type silicon chips from your T.A. Record the number scribed on the back of each chip. Store the chips in a clean petri-dish until you are ready to use them.

Note: Wafers are cleaned using OP-J and wet oxidized for an oxide to serve as a diffusion mask. See the Wet Ox Log Book for oxidation time used on your sample.

On the oxidized samples provided, measure the oxide thickness on one n-type and one p-type sample using the Filmetrics system and OP-R. Make sure to record the sample numbers on these chips in your notebook, and keep track of them as the materials properties test chips (here after referred to as the MPT chips). **Also make sure to mark these chips so you can tell which half will be oxide-etched and doped.** You will use the other two chips for your device arrays.

DEVICE CHIP NUMBERS:

n-type device chip # \_\_\_\_\_

p-type device chip # \_\_\_\_\_

MPT CHIP NUMBERS AND INITIAL FIELD OXIDE THICKNESS:

n-type MPT sample # \_\_\_\_\_ : t = \_\_\_\_\_ Å

p-type MPT sample # \_\_\_\_\_ : t = \_\_\_\_\_ Å

2. PHOTO-RESIST I (PRI): Windows for 1st diffusion.

- \_\_\_ a. Bake-out the sample for 5 mins. in post-bake oven. (This step may be skipped if sample did not go through any wet processing prior to PRI).
- \_\_\_ b. Spin-on the Adhesion Promoter (HMDS) at 4000 rpm for 30 sec.
- \_\_\_ c. Spin-on positive-resist (1350J) at 4000 rpm for 30 sec.
- \_\_\_ d. Pre-bake sample for 10 mins in the Pre-bake oven, 95° C.
- \_\_\_ e. On your device samples, use OP-0 to align the sample with the 1st diffusion mask, MASK I, so that its edges are approximately parallel to the edges of your chip.
- \_\_\_ f. Using the same OP, do a 15 sec exposure to UV. CHECK LOG BOOK FOR UPDATED EXPOSURE TIMES.
- \_\_\_ g. Dip the sample in developer for 60 sec followed by two rinses in the high purity H<sub>2</sub>O beakers. Blow dry the sample. Inspect pattern under microscope.

minimum resolution line: \_\_\_\_\_ μm  
minimum resolution space: \_\_\_\_\_ μm

\_\_\_ e'. On your materials properties test chips align the samples to the 50% opaque/50% clear mask so that 1/2 your chip is covered. **NOTE WHICH SIDE OF THE CHIP IS EXPOSED FOR LATER REFERENCE!!!!!!!!!!**

\_\_\_ f'. Expose as above.

\_\_\_ g'. Develop as above.

\_\_\_\_\_ h. Flood expose the chips under the U.V. lamp. Use a 5 sec exposure /pause 5 sec/ 5sec exposure sequence. CHECK FOR UPDATES ON THE TIMING OF THE FLOOD EXPOSURE!

NOTE IF BACK SIDE RESIST COATING PROCEDURE IS USED, IT MUST BE DONE BEFORE POST-BAKE! IF USING RESIST FOR BACK SIDE PROTECTION, FOLLOW THE NEXT TWO STEPS (steps i1 and j1; IF USING THE WAX PROCEDURE, SKIP TO steps i2 and j2. **Check with TAs for updates on these steps.**

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\_\_\_\_\_ i1. To protect the oxide on the back side of the chip during etching we need to coat it. Resist coating procedure: Working in the small hood, place a VERY SMALL drop of resist on a clean microscope slide. Now CAREFULLY place your chip BACKSIDE DOWN onto the resist. Using forceps, gently press down on the corners of the chip, and rotate the chip to evenly distribute the resist over the back. **CAREFULLY** slide your chip off the the microscope slide (DO NOT TRY TO PULL IT VERTICALLY OFF) and inspect for good resist coverage. Place the chip vertically in the teflon carrier with the other chips; now procede to post bake.

\_\_\_\_\_ j1. Post-bake samples for 15 min in the Post Bake Oven, 125° C.

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\_\_\_\_\_ i2. Post-bake samples for 15 min in the Post Bake Oven, 125° C.

\_\_\_\_\_ j2. To protect the oxide on the back side of the chip during etching we need to coat it. Wax coating procedure: In the small hood turn the hot plate on, set for LOW, and allow it to warm up. Place a clean microscope slide on the hot plate, and place a SMALL amount of clear wax on the slide by rubbing the wax stick on the slide. Now CAREFULLY place your chip BACKSIDE DOWN onto the molten wax. Using q-tips, gently press down on the corners of the chip, and rotate the chip to evenly distribute the wax over the back. **Quickly** slide your chip off the the microscope slide (DO NOT TRY TO PULL IT VERTICALLY OFF) and inspect for good wax coverage. The chip will cool quickly, then place it back in your petri dish.

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**Check your pattern by examining your chips with the Nikon Microscope; make sure you know what is photoresist and what is bare substrate.**

3. Etch windows for 1st diffusion (all chips).

\_\_\_\_\_ a. Etch oxide in buffered HF (BHF) for approximately 4 min. Etch rate is about 1000 Å/min. When etching is complete the etched areas should dewet. Rinse and blow dry. **Check with TAs for updated etch times.**

\_\_\_\_\_ b. Clean the photoresist off the chips after etching: rinse in acetone/ethanol/HP H<sub>2</sub>O.

minimum resolution line etched: \_\_\_\_\_ µm  
minimum resolution space unetched: \_\_\_\_\_ µm

4. Strip remaining photoresist (all chips).

\_\_\_\_\_ a. Place chips in the boat inside the Plasmod (see OP-K) and oxygen ash at full power for 5 min.  
**THIS STEP MAY BE OMITTED: CHECK WITH THE TA's!**



**Lab 4:** Boron, Phosphorus Predeposition

Required reading: OP-A, OP-D, OP-E, OP-F, OP-H

**PRELAB QUESTION:** ANSWER IN LAB NOTEBOOK BEFORE LAB PERIOD BEGINS!

1. The operating procedures for the pre-dep furnaces specify that you use several different flow meter settings. Using the settings given find about how long it takes to completely displace the volume of gas contained in the furnace tube for each flow rate given. Why might each of these rates have been chosen?

2. For the sheet resistance measurements on the MPT chips, what are the dimensions you should use in order to find the correction factors  $CF_d$  and  $CF_t$  in order to convert I and V measurements into true sheet R's? Remember you have doped only one half of the sample, and think about where the current will be confined to flow.

5. Pre-deposition

- \_\_\_ a. Immediately prior to predep, perform a 5 sec BHF etch to remove any native oxides.
- \_\_\_ b. On the n-type substrates, perform a 30 min. boron pre-dep (see OP-A, OP-D).
- \_\_\_ c. On the p-type substrates, perform a 20 min. phosphorus pre-dep (see OP-A, OP-E).

6. Predep sheet resistances and Oxide thickness measurement.

- \_\_\_ a. Strip boro-silicate/phospho-silicate glass from all chips with BHF etch:  
n-type chips (boron-doped): 30 sec.  
p-type chips (phosphorus-doped): 15 sec.  
Rinse and spin dry.
- \_\_\_ b. Measure the sheet resistance of the doped layers on the materials test chips using the 4 point probes and OP-H. Make three (3) measurements at slightly different locations on each chip to check the accuracy of the measurement.

n-type substrate, boron-doped:  $R_S =$  \_\_\_\_\_

p-type substrate, phosphorus-doped:  $R_S =$  \_\_\_\_\_

**Record these results in the appropriate Furnace Log Books.**

\_\_\_\_\_ c. Using the Filmetrics system and OP-R, measure the oxide thickness on both the doped and undoped sides of your MPT chips.

ox thickness, n-type : doped\_\_\_\_\_ undoped\_\_\_\_\_  
ox thickness, p-type : doped\_\_\_\_\_ undoped\_\_\_\_\_

**Labs 5 and 6:** Drive-in, 2nd Photoresist pattern.

Required reading: OP-F, OP-L, OP-O, OP-H, OP-R

**PRELAB QUESTION:** ANSWER IN LAB NOTEBOOK BEFORE LAB PERIOD BEGINS!

1. How long does it take to completely displace the volume of gas contained in the furnace tube for each flow rate given? Why might each of these rates have been chosen? During the drive, roughly how much time is spent in an oxidizing ambient, and how much in a non-oxidizing one?

7. Drive-in

\_\_\_\_\_ a. On all your samples, perform a 30 min. drive-in at 1100° C:

i) initiate drive-in in O<sub>2</sub>, 1 liter/min., for 5 min.

ii) conclude with N<sub>2</sub>, 1 liter/min., for 25 min. (see OP-A, OP-F)

\_\_\_\_\_ b. After drive, on your material properties samples measure the oxide thickness using OP- R. Make sure to measure the thickness on both the doped and undoped sides of the samples.

ox thickness, n-type : doped\_\_\_\_\_ undoped\_\_\_\_\_  
ox thickness, p-type : doped\_\_\_\_\_ undoped\_\_\_\_\_

8. PR II: Gate oxide pattern, Mask 2, on device chips ONLY.

\_\_\_\_\_ a. Dehydration bake, 5 min. at 125° C (use the Post Bake oven).

\_\_\_\_\_ b. Spin on adhesion promoter, 4000 rpm, 30 sec.

\_\_\_\_\_ c. Spin on photoresist (1350J), 4000 rpm, 30 sec.

- \_\_\_ d. Pre-bake: 10 min, 95° C.
- \_\_\_ e. Using OP-O, align the sample pattern to the pattern on Mask 2. Be very careful; do the rotational alignment first, then the x-y alignment. Use the split-field technique.
- \_\_\_ f. Expose for 15 sec.; **check for current exposure time.**
- \_\_\_ g. Develop (60 sec), rinse, blow dry. **Inspect pattern with Nikon microscope! Is it OK??**

x registration error: \_\_\_\_\_  $\mu\text{m}$   
 y registration error: \_\_\_\_\_  $\mu\text{m}$

- \_\_\_ h. Flood expose: use a 5 sec. exposure, pause 5 sec., then 5 sec. exposure.
- \_\_\_ i. Post-bake: 15 min, 125° C.

9. Etch all oxide from gate/capacitor areas and all oxide from materials chips.

- \_\_\_ a. Using buffered HF, perform a 4 min. oxide etch. When complete the back side of the chip should de-wet. Remember to include your materials properties test chips. **Check with TAs for updated etch times.**
- \_\_\_ b. Inspect pattern with microscope.
- \_\_\_ c. On the material properties test chips (which should now be completely free from all oxides) measure the sheet resistance of both the doped and undoped sides of the chips using OP-H. Again take three different measurements.

n-type : B doped  $R_S =$  \_\_\_\_\_ undoped  $R_S =$  \_\_\_\_\_  
 p-type : P doped  $R_S =$  \_\_\_\_\_ undoped  $R_S =$  \_\_\_\_\_

**Record these results in the appropriate Furnace Log Books.**

10. Strip Photoresist from device chips: NA Fall 1988

- \_\_\_ a. Rinse sample: acetone/ethanol/HPH<sub>2</sub>O.
- \_\_\_ b. Strip sample in Plasmod (OP-K), full power, 5 min. **STEP MAY BE OMITTED: CHECK WITH TA's!**

\_\_\_\_\_ c. Inspect pattern with microscope.

**Lab Report I (see p. 34) is due on SOON: see course schedule for exact date!**

**Labs 7 and 8:** Gate Oxidation, 3rd Photoresist Pattern, Contact Windows

Required reading: OP-J, OP-N, OP-C

11. Gate oxide growth on ALL chips.

\_\_\_\_\_ a. Immediately prior to oxide growth, perform a 5 sec. BHF etch, rinse, dry.

\_\_\_\_\_ b. Immediately after the BHF dip perform the RCA cleaning step for inorganic contamination using a 5:1:1 solution of HP H<sub>2</sub>O: 30% H<sub>2</sub>O<sub>2</sub>: 37% HCl for 5 min. (see OP-J). Rinse thoroughly in HP H<sub>2</sub>O.

**Note: TA's should check temperature of Dry Ox Furnace prior to this step.**

\_\_\_\_\_ c. Grow oxide in Dry Ox Furnace, as per OP-C, but before pushing samples into furnace center zone, allow them to heat in the furnace neck for 5 min. Make sure to oxidize all four of your samples. Perform the oxidation WITH CHLORINE INJECTION, for the time indicated by your lab TA.

time in O<sub>2</sub>: \_\_\_\_\_;

time in O<sub>2</sub> + TCE: \_\_\_\_\_;

time in N<sub>2</sub>: \_\_\_\_\_.

**Record in Furnace Log Book!!!!**

\_\_\_\_\_ d. On your material properties test samples, measure the thickness of the oxide just grown using OP-R. Measure the oxide thickness over both doped and undoped regions.

n-type, thickness : doped \_\_\_\_\_ undoped \_\_\_\_\_

p-type, thickness : doped \_\_\_\_\_ undoped \_\_\_\_\_

**Record in Furnace Log Book!!!!**

12. PR III: Contact window pattern, Mask 3, on device chips only.

\_\_\_\_\_ a. Dehydration bake, 5 min. at 125° C.

- \_\_\_ b. Spin on adhesion promoter, 4000 rpm, 30 sec.
- \_\_\_ c. Spin on photoresist (1350J), 4000 rpm, 30 sec.
- \_\_\_ d. Pre-bake: 10 min., 95° C.
- \_\_\_ e. Using OP-O, align the sample pattern to the pattern on Mask 3. Be very careful; do the rotational alignment first, then the x-y alignment.
- \_\_\_ f. Expose for 15 sec. Check for current exposure time.
- \_\_\_ g. Develop (60 sec) in AZ developer, rinse, blow dry. **Inspect for proper results with Nikon microscope.**

minimum resolution line: \_\_\_\_\_  $\mu\text{m}$   
 minimum resolution space: \_\_\_\_\_  $\mu\text{m}$   
 x registration error: \_\_\_\_\_  $\mu\text{m}$   
 y registration error: \_\_\_\_\_  $\mu\text{m}$

- \_\_\_ h. Flood expose (5 sec. exposure, 5 sec. pause, 5 sec. exposure).

Note: Do NOT cover back side of chip with wax or photoresist.

- \_\_\_ i. Post-bake: 15 min., 125° C.

13. Etch oxide from contact windows and oxide from materials properties test samples.

- \_\_\_ a. Using the BHF etch station, perform a 4 min. oxide etch. When complete the back side of the chip should de-wet.
- \_\_\_ b. Inspect pattern with microscope.
- \_\_\_ c. Using OP-H, measure the sheet resistance of the doped layers on your materials properties test samples.

n-type substrate, B-doped :  $R_S =$  \_\_\_\_\_  
 p-type substrate, p-doped :  $R_S =$  \_\_\_\_\_

- \_\_\_ d. Using OP-N, measure the junction depth on the doped side of your material properties test chips.

n-type substrate, B-doped  $R_j =$  \_\_\_\_\_  
p-type substrate, P-doped  $R_j =$  \_\_\_\_\_

**Lab 9, 10, and 11:** Complete Device Fabrication

Required Reading: OP-G, Vacuum Evaporation

14. Back side damage chip (device samples only for rest of processing).

\_\_\_ a. Place chip face down on a piece of filter paper. While holding one corner down with your forceps, CAREFULLY damage the back side of your chip with the fine sandpaper provided. It is not necessary to damage a large area of the chip.

15. Strip photoresist.

\_\_\_ a. Rinse sample: acetone/ethanol/HPH<sub>2</sub>O.

\_\_\_ b. Strip sample Plasmod (OP-K), **1/2 power**, 5 min.  
STEP MAY BE OMITTED: CHECK WITH TA's!

\_\_\_ c. Inspect pattern with microscope.

minimum resolution line etched: \_\_\_\_\_  $\mu\text{m}$

minimum resolution space unetched: \_\_\_\_\_  $\mu\text{m}$

16. Aluminum evaporation

\_\_\_ a. CAREFULLY follow OP-G to vent and raise the vacuum system bell jar.

\_\_\_ b. Load the aluminum evaporation filament with 4 inches of aluminum wire. The wire should be very carefully wrapped around the center of the filament. **See TAs for help.**

\_\_\_ c. Clamp your sample front-side down using the clips on the chimney cover plate. Remember to put at least one clear glass slide on the cover plate to double check metallization thickness.

\_\_\_ d. Follow OP-G to pump down the vacuum system. Allow 15 min. for vacuum to improve.

\_\_\_ e. Evaporate aluminum: see lab TA for up-date on evap system operation.

\_\_\_ f. After concluding evaporation, allow 5 min. for the filament to cool, then vent and remove your sample as per OP-G.

17. PR IV: Aluminum contact pattern, Mask 4.

\_\_\_ a. Spin on adhesion promoter, 4000 rpm, 30 sec.

\_\_\_ b. Spin on photoresist (1350J), 4000 rpm, 30 sec.

- \_\_\_ c. Pre-bake: 10 min., 95° C.
- \_\_\_ d. Using OP-L, align the sample pattern to the pattern on Mask 4.
- \_\_\_ e. Expose for 25 sec. **Note the increased exposure time used when exposing resist over metal. Check for current exposure time.**
- \_\_\_ f. Develop (60 sec), rinse, dry. **Inspect for proper pattern with Nikon microscope.**

minimum resolution line: \_\_\_\_\_ μm  
 minimum resolution space: \_\_\_\_\_ μm  
 x registration error: \_\_\_\_\_ μm  
 y registration error: \_\_\_\_\_ μm

- \_\_\_ g. Flood expose (5 sec. exposure, 5 sec. pause, 5 sec. exposure).
- \_\_\_ h. Post-bake: 15 min., 125° C.

18. Aluminum etch.

- \_\_\_ a. Etch aluminum in Transene Type A Aluminum Etchant. Etch time should be approximately two minutes; continue etch until pattern is clearly visible.
- \_\_\_ b. Rinse thoroughly in HPH<sub>2</sub>O.

19. Strip photoresist.

- \_\_\_ a. Rinse sample: acetone/ethanol/HPH<sub>2</sub>O.
- \_\_\_ b. Strip sample Plasmod (OP-K), **1/2 power**, 5 min.  
STEP MAY BE OMITTED: CHECK WITH TA'S.
- \_\_\_ c. Inspect pattern with microscope.

minimum resolution line etched: \_\_\_\_\_ μm  
 minimum resolution space unetched: \_\_\_\_\_ μm

20. Metallize chip back side.

- \_\_\_ a. Follow OP-G to vent and raise the vacuum system bell jar.
- \_\_\_ b. Load the aluminum filament with metal (4" wire length).



- \_\_\_\_\_ c. Load sample back side down. Remember to put in a blank slide to monitor the evaporation.
- \_\_\_\_\_ d. Follow OP-G to pump down the vacuum system. Allow 15 min. for pump down.
- \_\_\_\_\_ e. Evaporate aluminum at 40 amps for 2 min.
- \_\_\_\_\_ f. After completing evaporation, allow 5 min. for cooling, then vent and remove sample as per OP-G.

21. Form ohmic contacts and anneal gate oxide.

- \_\_\_\_\_ a. Set N<sub>2</sub> flow in small annealing furnace #1 to 100 with steel ball (160 cc/min). Flush furnace for 5 min. before loading samples.
- \_\_\_\_\_ b. Load samples into quartz boat, push into center of furnace. Anneal for 15 min. at 450° C.

Note: This furnace controller gives temperature in Fahrenheit, so be careful. Sample fabrication is now complete. You should now proceed to the Lab Report section in the Lab Manual. **Make sure to refer to any updates on what testing is actually required given in class!!!**

**Lab Report II (see p. 35) is due SOON, see course schedule for date!**

## Laboratory Report Guidelines

filename: REPORTS update

This is an update containing further details on your lab reports. You should still read Section A, p. Intro-1, that contains the old information on lab report format; most comments made there are still valid.

### GENERAL COMMENTS:

As usual, where ever possible check your results based on "reasonableness" arguments. You should always find several other ways to check each measurement you have made, for instance by checking the expected process results against Gandhi or the Lab Manual, by checking the process log books in lab, and by performing any calculations that are reasonable. REFERENCE ALL OUTSIDE SOURCES OF INFORMATION, AS WELL AS THE LOCATION OF YOUR RAW DATA IN YOUR LAB NOTEBOOK. As a general rule, the statement "as expected," when used in reference to the results of some measurement, is NOT acceptable, unless you state *explicitly* why it is expected.

MAKE COPIES OF THE TABLES INCLUDED HERE (pp. Up-6 through Up-8) FOR USE IN EACH LAB REPORT. **I STRONGLY ADVISE YOU KEEP A COPY OF ALL YOUR COMPLETED TABLES AND DRAWINGS, IN ADDITION TO WHAT YOU TURN IN.**

### **TWO COPIES OF REPORT 1 AND 2 MUST BE SUBMITTED!**

### CRITIQUES

You are not only be responsible for writing lab reports, but also for **critiquing** other group's reports. The quality of your understanding of what you do and observe is influenced by how hard you work on the Lab Reports, and can be greatly enhanced by exposure to alternative views. This is not just a scheme to get you to grade the reports for me; I will read and grade the reports, as well as reading and grading your critiques. **Except for Lab Report 0 you and your lab partner(s) will prepare the reports as a team, submitting one report per group.** You will, however, do your critiques individually.

### General comments about critiques:

You will receive a copy of another group's lab report. Read the report carefully; editorial comments should be made in the margins of the report. Try to flag things you do not understand, weak and/or unsupported arguments, or incorrect conclusions. Also flag good points, or conclusions you agree with but did not notice when you wrote your own report.

## **Fall 1999 Updates on Reports:**

### **LAB REPORT "ZERO": DUE IN CLASS, Weds. Sept. 8:**

#### **Every individual must do this assignment**

**Construct a flow chart which illustrates the major steps in our fabrication procedure.**

Separate flow charts for the MPT and Device chips should be used, but they should be drawn in parallel to illustrate the common (and dissimilar) processes used for the two sets of chips. You should read the **entire** Processing Description Section of the Lab Manual, and make sure you understand the sequence of steps necessary to fabricate our devices. This assignment is critical to the successful completion of your devices.

### **Critique of Lab Report 0, due in class, Monday, Sept. 20.**

The remaining reports should be done in formal collaboration with your lab partner(s):

### **LAB REPORT I (one report per lab group; two copies required), due Monday, Oct. 18:**

Give a **very brief** overview of the processing; outline form is adequate. In the tables, **do not** fill out the "Calculated" sheet resistance boxes. **Concentrate on reporting the experimentally measured values, along with their uncertainty estimates.**

### **Critique of Lab Report I, due Monday, Nov. 1:**

Look carefully at significant figures and justification for the precision and accuracy of the measurements.

### **LAB REPORT II (one report per lab group; two copies required), due Monday, Nov. 15:**

**Concentrate on presenting your calculations for sheet resistance and junction depth.** Use "purely" theoretical means to find the diffusion profiles. Do **NOT** use empirical formulas for pre-dep results. Discuss the impact of possible concentration-dependent diffusion on your measurements, and the agreement or disagreement between theory and actual measurements.

### **Critique of Lab Report II, due Friday., Dec. 3.**

### **LAB REPORT III and TESTING (one report per lab group; one copy required) due Friday Dec. 3:**

Perform only the basic qualification procedure for your MOSFETs as outlined in the DEVICE TROUBLE SHOOTING section of the Lab Manual. Discuss this procedure and your results in Lab Report III. You may skip the rest of the Device Testing Section, but read it, as well as the complete guidelines for Lab Report III in the Lab Manual.

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## Questions for Lab Report 1

Discuss the following points in your lab reports. Please phrase your answers to questions 2 and 3 below in such a way as to re-state the question being answered. A **short** discussion is appropriate.

1. Give a brief overview of the process to date; an **outline format** would probably be most appropriate. You should clearly identify the location of each device in the Holberg Mask Set (pp. 38-47), along with the function of Masks 1, 2, 3 and 4 in terms of how they form the devices. You should include **accurate, clearly labeled cross-sectional drawings** of the MOSFET, diffused diode, and MOS capacitor with guard ring, at the following points in the processing: after step 4 (immediately before pre-dep); after step 6 (immediately before drive); and after step 10 (immediately before gate ox). Based on data gathered from your MPT chips you should be able to give some of the actual thicknesses of various layers in the devices.

2. Discuss the geometry correction factors necessary to interpret the four point probe measurements. Be careful to distinguish between the doped and undoped sides, and how this affects the dimensions you use for calculations of sheet resistance. Which measurements can be used to calculate a resistivity, and which can only be used to determine sheet R? Based on the measurements made so far, for what areas of the chip can you give an actual doping concentration, either background or diffused? Use this data to fill out the appropriate blocks in Tables II and III. Make sure you do not quote numerical results of precision greater than what you actually think is significant. You should give in the Tables an approximate value for the uncertainty. A short discussion of how you calculated each value (both the quantity of interest and its associated uncertainty) should be given.

3. Discuss the ellipsometric results. Again, make sure to consider in which cases your results are reasonable. The index of refraction calculated from your measurements is a good place to start. Reference from a book any materials properties you need to interpret the results. Fill out all the blocks in Table I that you have sufficient information to determine. Again you must determine how many significant figures you have actually measured to. You should give in the Tables an approximate value for the uncertainty. A

short discussion of how you calculated each value (both the quantity of interest and its associated uncertainty) should be given.

4. Use the information gathered in the lab using the registration verniers and resolution bars on the masks to fill out Table IV. "Statistics" are important here, so indicate in footnotes how many measurements your numbers are based on.

## Questions for Lab Report 2

1. Provide ACCURATE, CLEARLY labeled cross-sectional drawings of all the completed devices. You should have enough information to label your device cross sections with actual dimensions in **both the vertical and horizontal directions**. Based on the data you have obtained from the MPT chips, you should be able to fill out several more blocks in Tables I and II; as before, a short discussion of how you calculated each value (both the quantity of interest and its associated uncertainty) should be given.

2. Using information in Ghandhi, calculate the junction depths in your n- and p-type chips. Be very careful, and cross check any approximations you might use concerning diffusion constants, etc. Once you have calculated a diffusion profile you can use the Irwin curves to find the final sheet resistance of the diffused layers; compare this calculated value to your measured values, and discuss any differences. Show your junction grooving results, and compare them to your calculations.

3. Use the information gathered in the lab using the registration verniers and resolution bars on the masks to complete Table IV. "Statistics" are important here, so indicate in footnotes how many measurements your numbers are based on.

## Questions for Lab Report 3: READ THESE BEFORE YOU BEGIN TESTING

1. Draw diagrams for each device showing the relationship between the the device layout and the electrical connections to the device. Where necessary make sure that you consider connections through the backside of the chip. Indicate how the electrical test connections are made between the probe stations and the device-under-test (the DUT).

2. Device parameter extraction equations should be properly referenced, and great care used in determining what approximations have been used. The Lab Manual and OP's contain some of the necessary equations, but you will probably need to use some 339 equivalent text to get everything right.

**Perform only the basic qualification procedure for your MOSFETs as outlined in the DEVICE TROUBLE SHOOTING section of the Lab Manual. Discuss this procedure and your results in Lab Report III. You may skip the rest of the Device Testing Section, but read it, as well as the complete guidelines for Lab Report III in the Lab Manual.**

PLEASE NOTE THE SIGN UP PROCEDURE FOR TESTING EQUIPMENT:

For each test station (CV Station; IV Station; Resistance Station) there will be a SIGN UP SHEET posted outside the lab. Please do NOT sign up for more than two time slots at a time.

**Table 1: n-type MPT chips Oxide Thickness Measurements**

Process Step	boron-doped areas		undoped areas	
	thickness (Å)	index	thickness (Å)	index
field oxide				
after pre-dep				
after drive-in				
after gate ox				
Test capacitors: with guard				
without guard				

**Table 2: p-type MPT chips Oxide Thickness Measurements**

Process Step	phosphorus-doped areas		undoped areas	
	thickness (Å)	index	thickness (Å)	index
field oxide				
after pre-dep				
after drive-in				
after gate ox				
Test capacitors: with guard				
without guard				

**Table 3: Sheet Resistance Measurements summaries**

Process Step	n-type MPT chip (boron diffused areas) Sheet Resistance $R_s$ ( $\bullet$ per square)		p-type MPT chips (phosphorus-diffused) Sheet Resistance $R_s$ ( $\bullet$ per square)	
	measured	calculated	measured	calculated
after pre-dep				
after drive-in				
after gate ox				
from resistors				
$R_{\text{contact}}$ ( $\bullet$ )				
bend size (squares)				

**Table 4: Undoped Wafer Characterization**

	Sheet R (4-pt probe) ( $\bullet$ /sq)	$\rho$ (calc) ( $\bullet$ -cm)	Background Concentration		
			(4-pt probe) ( $\text{cm}^{-3}$ )	(diode C-V) ( $\text{cm}^{-3}$ )	(cap C-V) ( $\text{cm}^{-3}$ )
p-type chip					
n-type chip					



**Table 5: Lithography and Etch Results**

	Level 1 Diffusion	Level 2 Gate	Level 3 Contact	Level 4 Metal
PR min line				
PR min space				
Etch min line				
Etch min space				
x reg				
y reg				

**Table 6: MOS Device Characterization**

	$V_{fb}$		Threshold Voltage	
	(cap C-V)	(cap C-V)	(long MOSFET #1 I-V)	(short MOSFET #2 I-V)
p-type chip				
n-type chip				

	Transconductance			
	(long MOSFET #1)	(calc)	(short MOSFET #2)	(calc)
p-type chip				
n-type chip				

	"Excess" Surface Charge			
	$Q_{ss}$ (col/cm <sup>2</sup> )		$Q_{ox}$ (#/cm <sup>2</sup> )	
	w/o guard	w guard ring	w/o guard	w guard ring
p-type chip				
n-type chip				

## Holberg Mask Set

filename: MASKS

This section describes in detail the functions of the Holberg Mask Set, shown with all four layers overlaid in Figure 1, and level-by-level in Figure 2, Figure 3, Figure 4, and Figure 5. Each functional block on the chip is discussed separately. These blocks are:

- i) Alignment, resolution, and registration patterns
- ii) Metal step coverage and leakage patterns
- iii) Diffused resistor and contact resistance test structures
- iv) Diffused diodes
- v) MOS capacitors
- vi) Thick and thin oxide MOSFETs

### Alignment, resolution, and registration patterns

The purpose of this part of the chip is to allow accurate alignment of each mask level to preceding levels already patterned, as well as to evaluate the accuracy of the alignment and the resolution of both lithographic and etching processes. The area in the upper right corner of the chip (Figure 1) is used for these purpose. Figure 7 shows a four level composite view of this region of the chip.

Figure 8 and Figure 9 shows diagrams to illustrate how the registration verniers are used to determine mis-alignment. In Mask Level 1 (Diffusion, Figure 2) windows are opened to provide the center part of the verniers; each subsequent level patterns bars on either side of the Level 1 pattern. Misalignment is determined by finding the outer and inner boxes which line up, and counting how many boxes from the end this occurs at. Each box from the end corresponds to 1  $\mu\text{m}$  misregistration.

Figure 10 shows a close up of the resolution bars. By inspecting these patterns using a microscope it is possible to evaluate the performance of our lithographic and etch processes. For evaluating the lithographic process, looking at the smallest bars that are made up of equal widths of exposed and unexposed resist tells us whether we have over-exposed (open, exposed regions wider than photoresist between the open regions) or under-exposed the resist (open, exposed regions narrower than photoresist between the open regions). Similar inspection after etch can be used to help determine the extent of undercutting during overetch.

### Diffused resistor and contact resistance test structures

The purpose of this part of the chip is to allow us to measure the sheet resistance due to our diffusions, as well as to find contact and bend resistance corrections. The area in the upper left corner of the chip (Figure 1) is used for these purposes. Figure 11 shows a three level composite (diffusion: Level 1; contact: Level 3; and metal: Level 4) view of this region of the chip.

There are four basic structures in this region. Two straight resistors, one short ( $R_1$ ) and one long ( $R_2$ ), are used to find sheet and contact resistances. Another serpentine resistor ( $R_3$ ) is used

to find the equivalent size and resistance of bends. The last structure allows four point measurement of sheet resistance, to help remove contact resistance problems from the measurements. See the TEST section for more details.

### Diffused diodes

The purpose of this part of the chip is to allow us to evaluate a diffused p-n junction diode. The region in the lower right corner of the chip (Figure 1) is used for this purpose. There are two diodes of identical size, the top device also having a field relief plate over the oxide covering the surface p-n junction.

### MOS capacitors

The purpose of this part of the chip is to allow us to evaluate the quality of our gate oxides. The region in the upper center of the chip (Figure 1) is used to make two MOS capacitors at the same time we grow the gate oxide for our MOSFETs. There are two capacitors of equal metal plate and thin oxide areas. The right device, however, also has a diffused guard ring around the perimeter of the capacitor that will reduce somewhat the effective area of the capacitor (and hence its capacitance) compared to the MOS cap without guard ring.

### Thick and thin oxide MOSFETs

The purpose of this part of the chip is fabricate two MOSFETs with different gate lengths, as well as a thick oxide MOSFET to help evaluate the quality of our field oxide. The area in the bottom left corner of the chip (Figure 1) is used for these purposes. Figure 12 shows a four level composite view of this region of the chip. The upper MOSFET (Device 1) has a longer channel than the device below it (Device 2). All three MOSFETs share a common source connection through the upper-most pad shown in Figure 12.

**Critical Mask Dimensions:**

MOSFET channels:

Device 1      800 $\mu$ m x 30 $\mu$ m  
Device 2      800 $\mu$ m x 20 $\mu$ m

MOS cap w guard ring:      600 $\mu$ m diam.  
MOS cap w/o guard ring:      550 $\mu$ m diam.

Diode diffusion diam.:      550 $\mu$ m

Diffused resistors (straight):  
Device 1      250 $\mu$ m (l) x 25 $\mu$ m (w)  
Device 2      500 $\mu$ m (l) x 25 $\mu$ m (w)

Registration verniers:      1 $\mu$ m increments

**Table 7: Resolution bars**

line number	line	following space	line number	line	following space
1	2 $\mu$ m	2 $\mu$ m			
2	2 $\mu$ m	3 $\mu$ m	8	10 $\mu$ m	10 $\mu$ m
3	3 $\mu$ m	3 $\mu$ m	9	15 $\mu$ m	15 $\mu$ m
4	3 $\mu$ m	5 $\mu$ m	10	15 $\mu$ m	15 $\mu$ m
5	5 $\mu$ m	5 $\mu$ m	11	20 $\mu$ m	20 $\mu$ m
6	5 $\mu$ m	5 $\mu$ m	12	20 $\mu$ m	20 $\mu$ m
7	10 $\mu$ m	10 $\mu$ m	13	25 $\mu$ m	25 $\mu$ m
			14	25 $\mu$ m	

Contact Windows:

Diffusion area:      50 $\mu$ m x 50 $\mu$ m

Oxide window size (metal/semiconductor contact area):  
25 $\mu$ m x 25 $\mu$ m

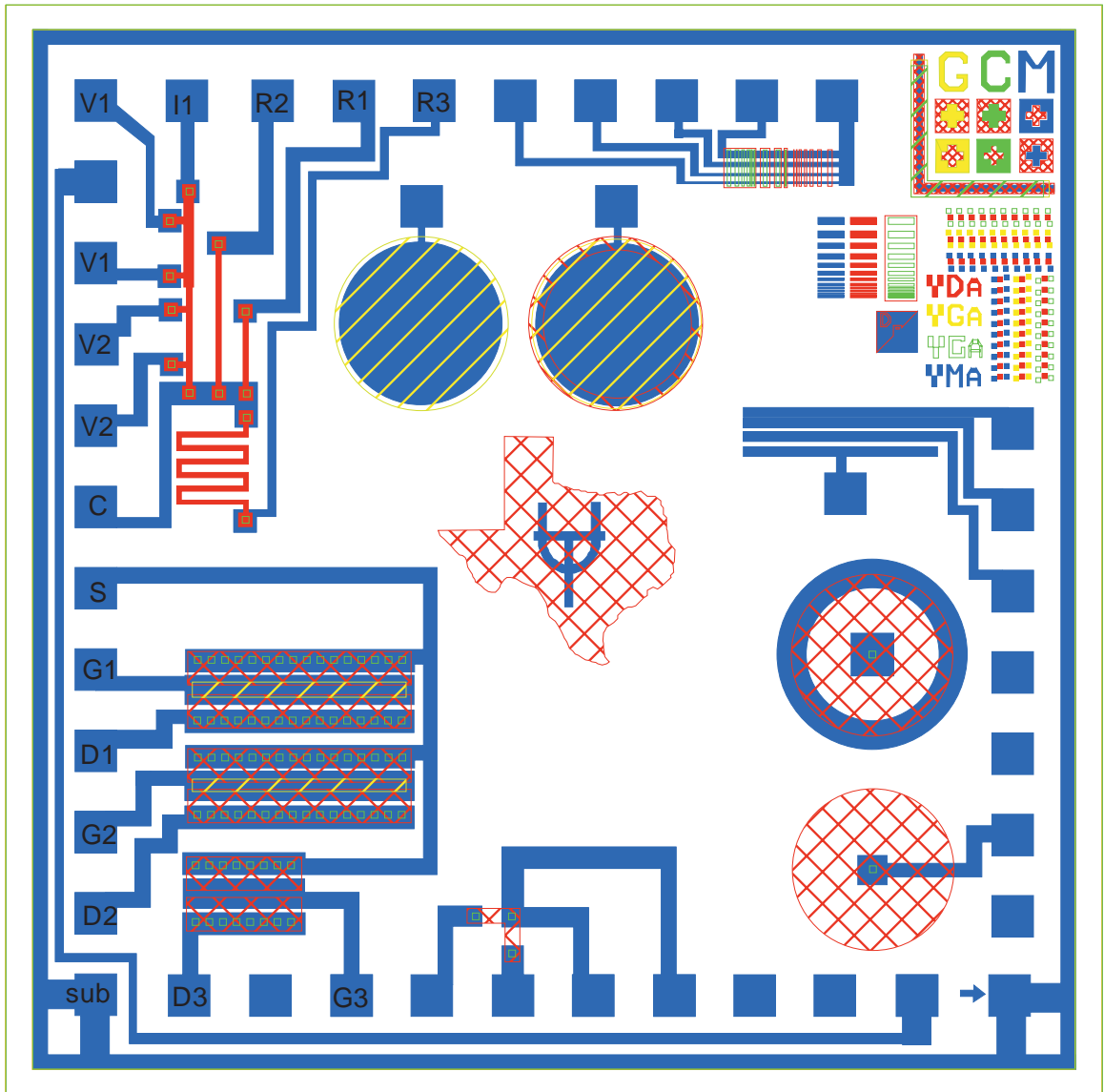
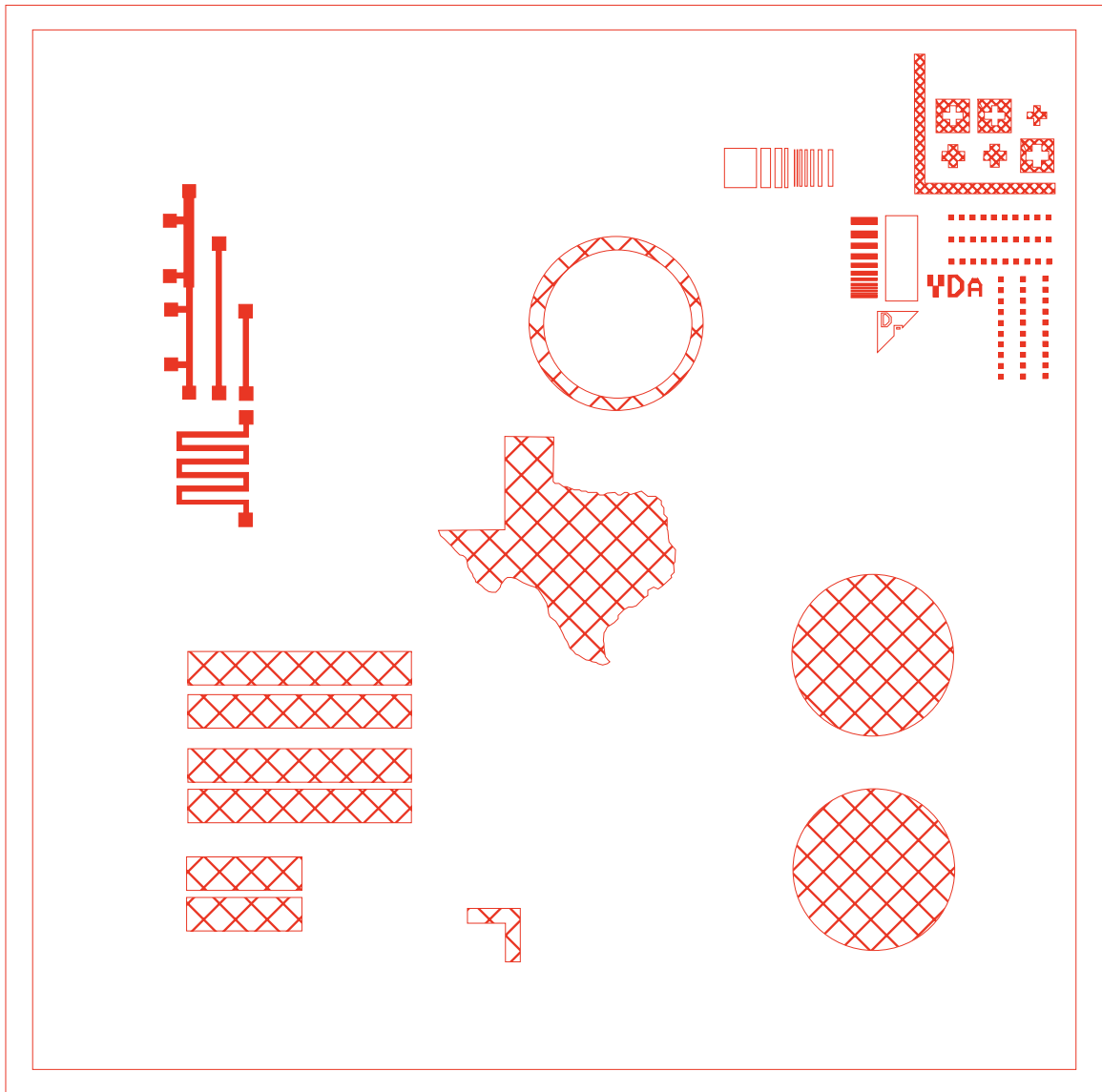


Figure 1: Composite Drawing of Holberg Mask Set.



**Figure 2: Holberg Mask Level 1, Diffusion**

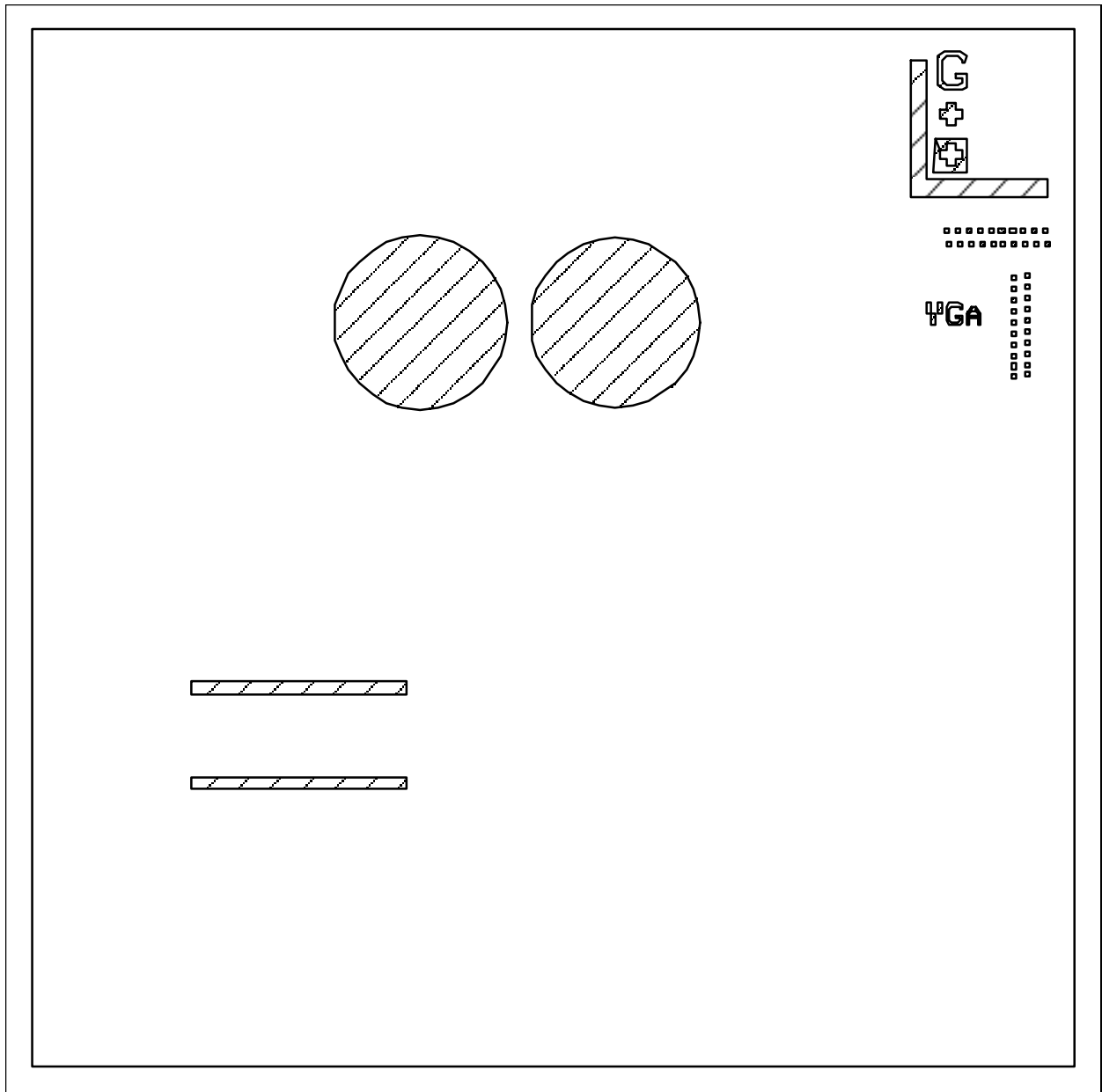


Figure 3: Holberg Mask Level 2, Gate.



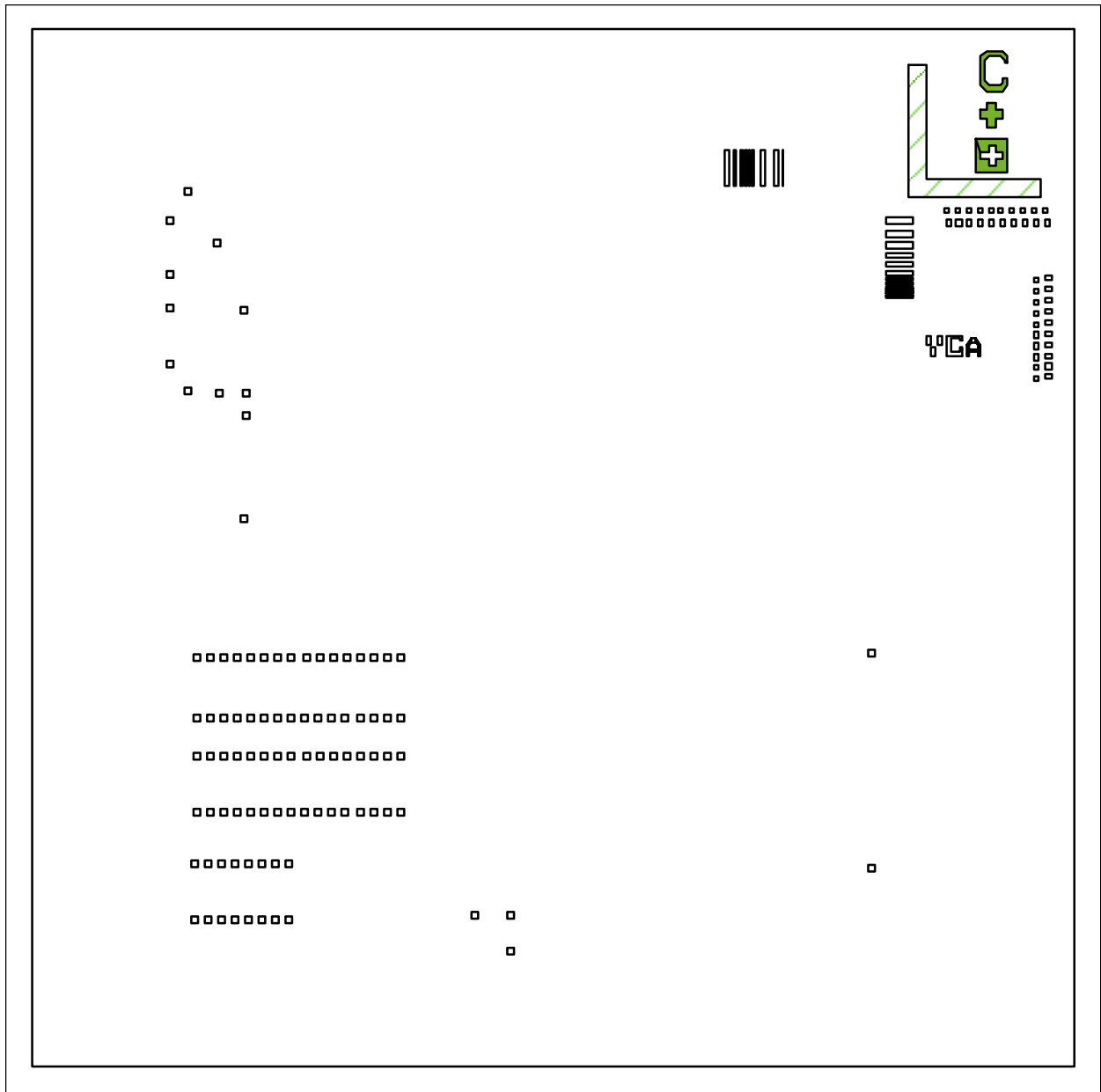


Figure 4: Holberg Mask Level 3, Contacts.

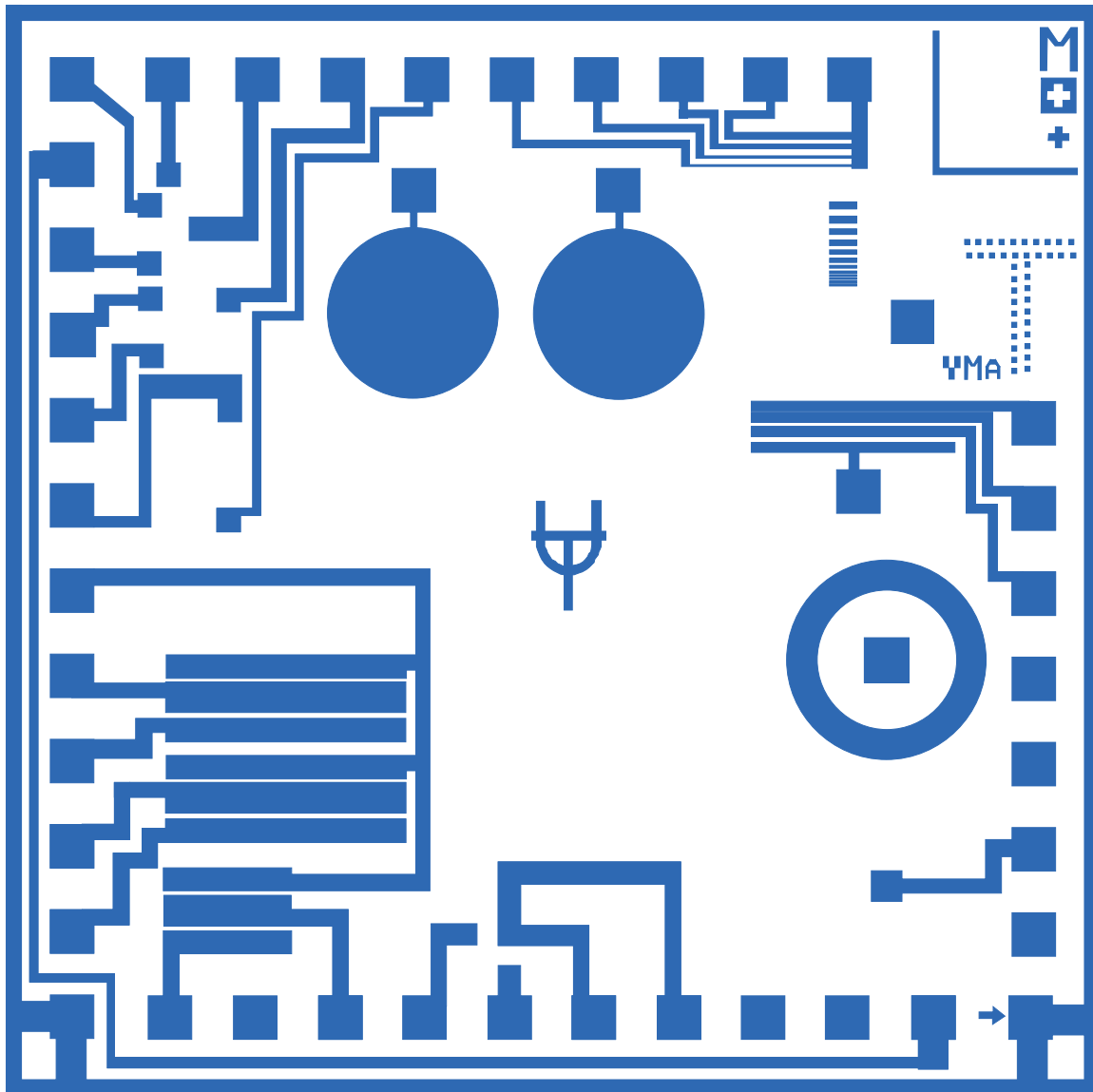
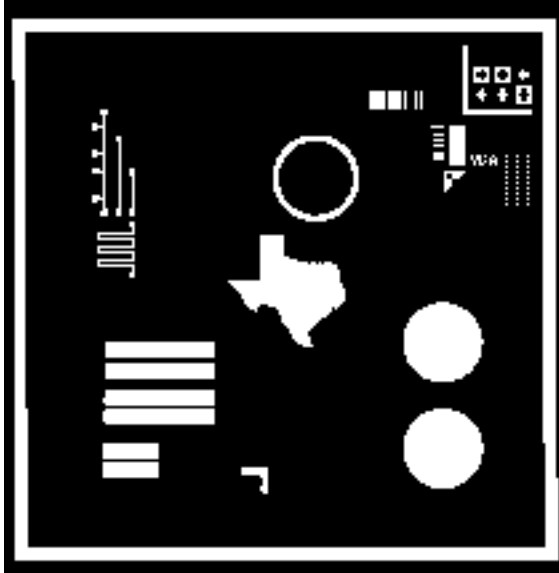
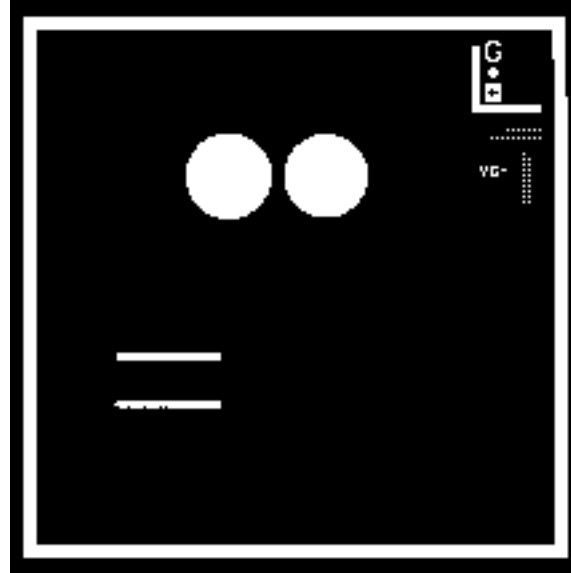


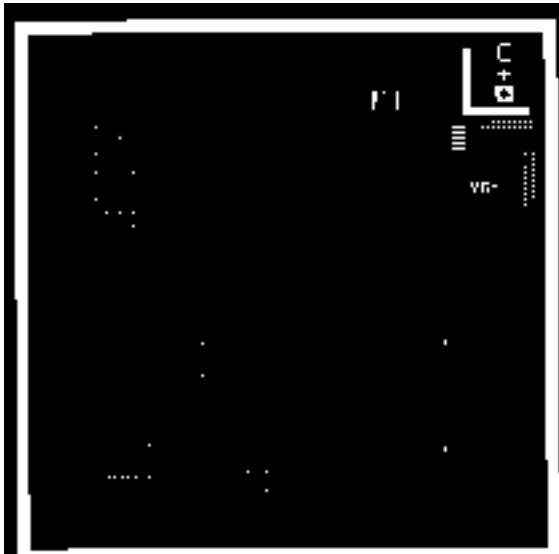
Figure 5: Holberg Mask Level 4, Metal.



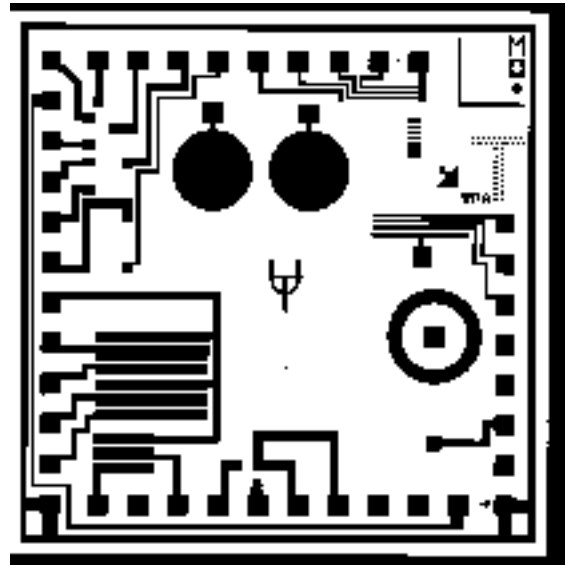
Holberg Mask 1, Diffusion



Holberg Mask 2, Gate



Holberg Mask 3, Contacts



Holberg Mask 4, Metal

**Figure 6: Scanned images of the Holberg Masks**

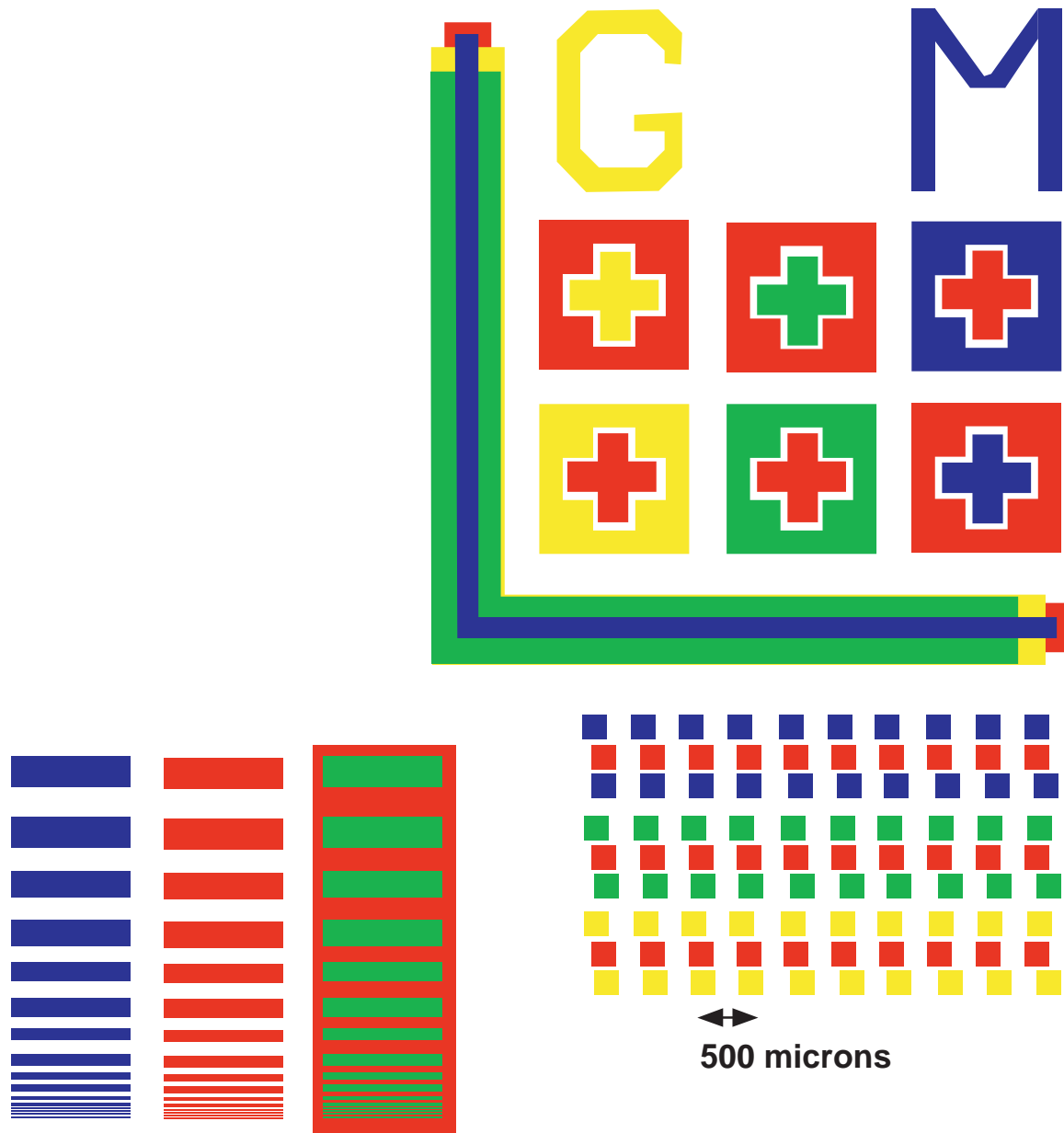
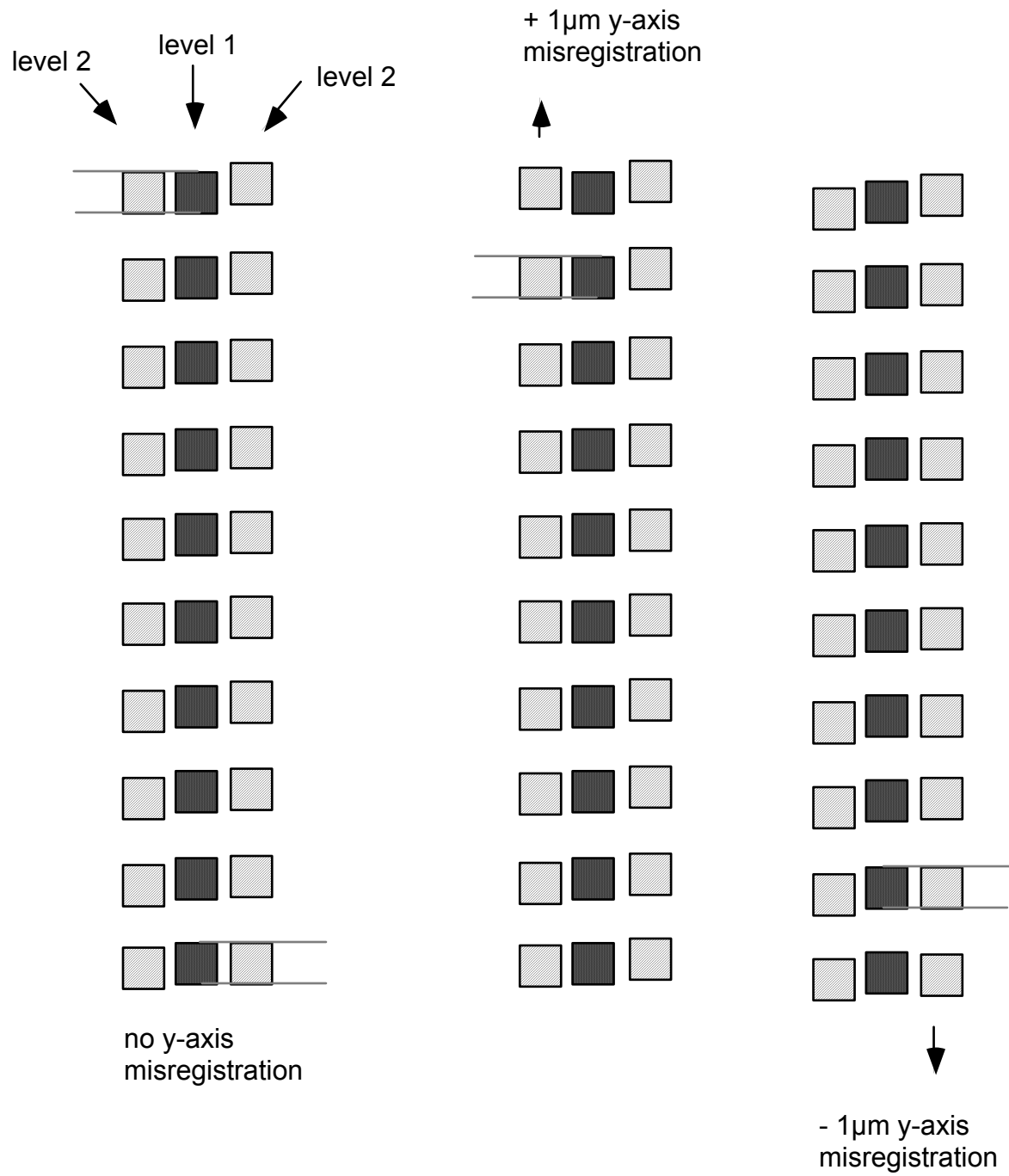
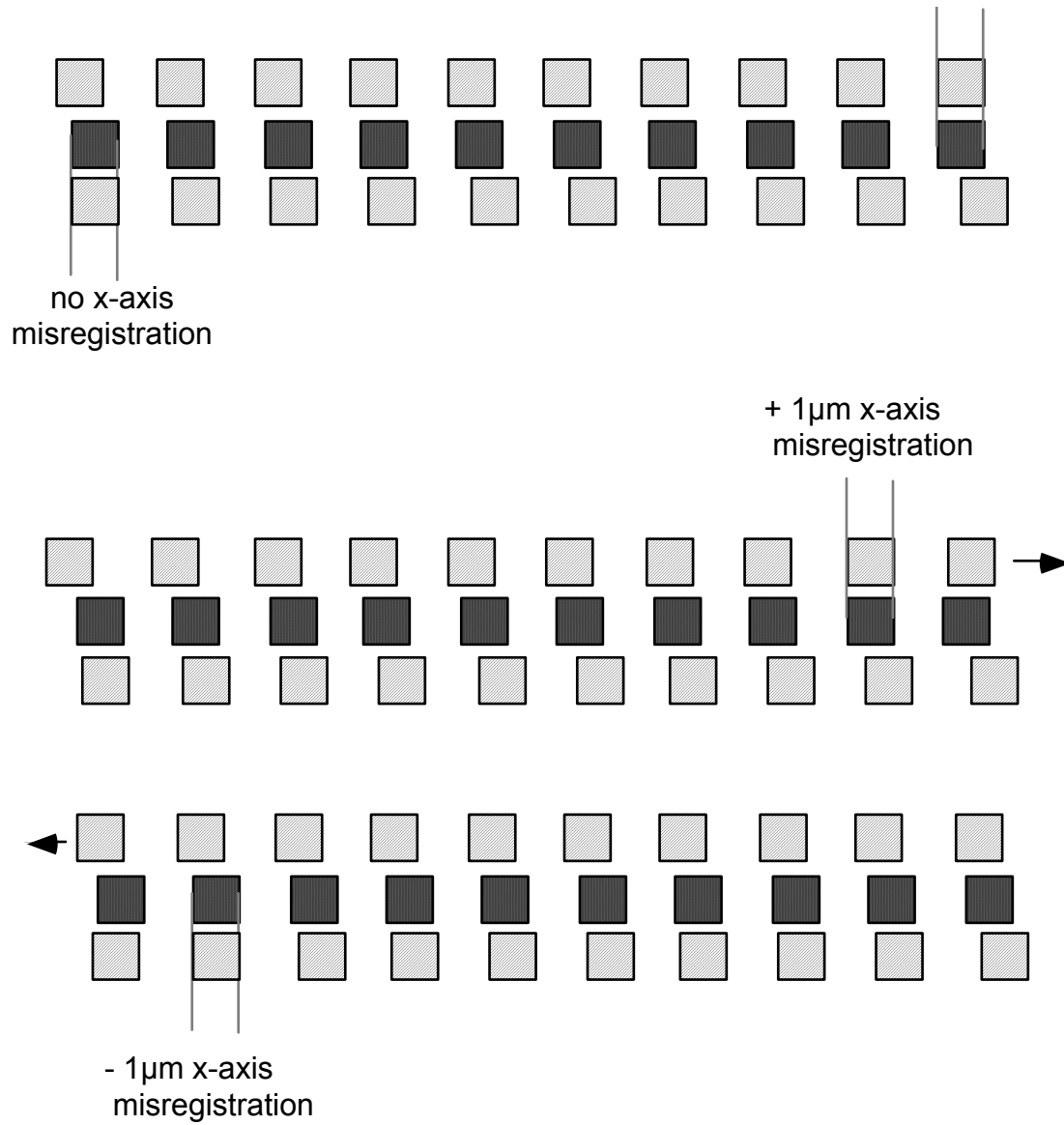


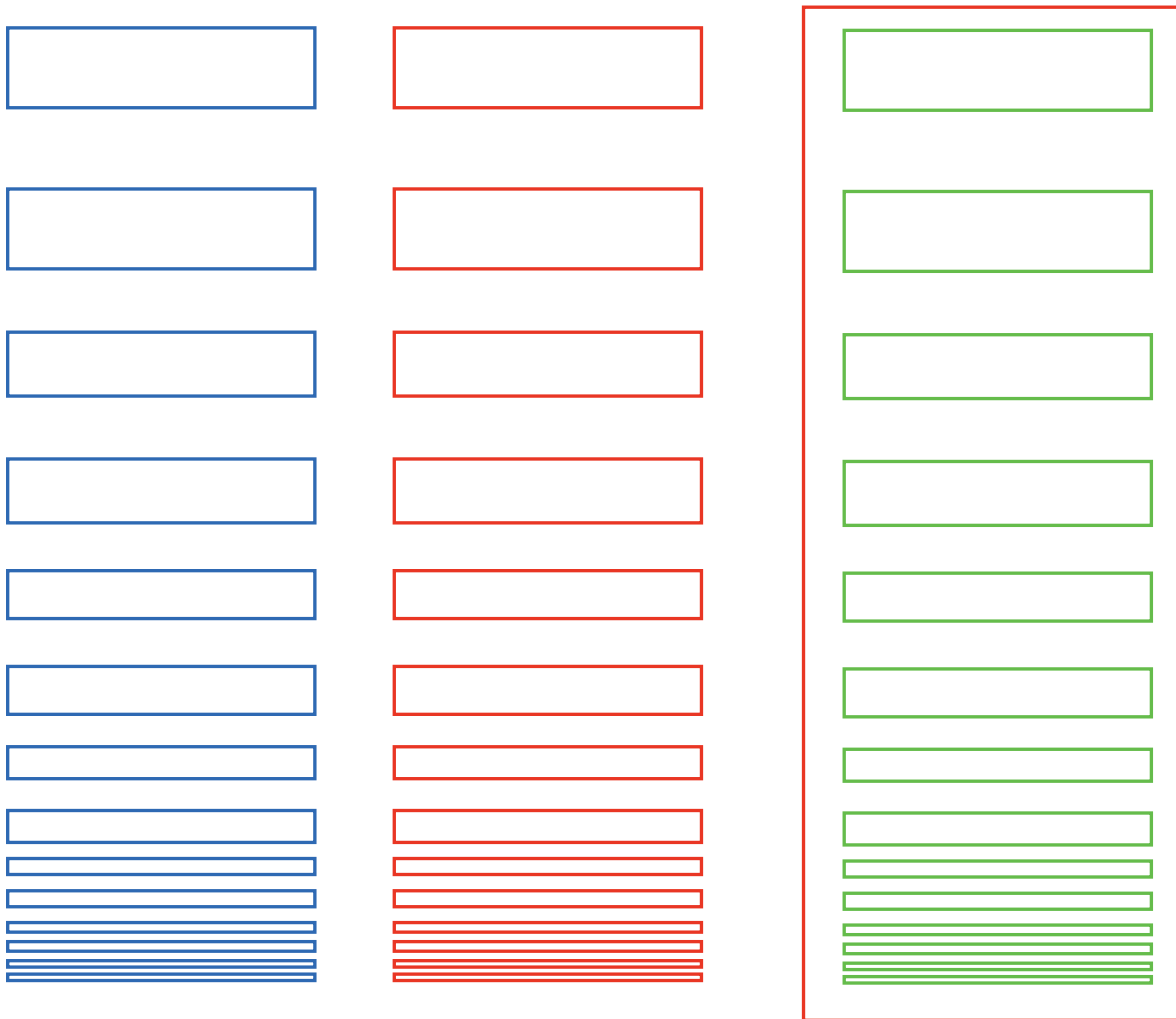
Figure 7: Composite view of alignment and registration patterns of Holberg Mask Set; all four levels are shown superimposed. The scale bar is 50  $\mu\text{m}$  long.



**Figure 8: Illustration of y-axis misregistration verniers. Three cases are shown: zero, +1, and -1 μm misregistration.**



**Figure 9: Illustration of x-axis misregistration verniers. Three cases are shown: zero, +1, and -1 μm misregistration.**



**Figure 10: Resolution bars. See Table 7 for dimensions.**

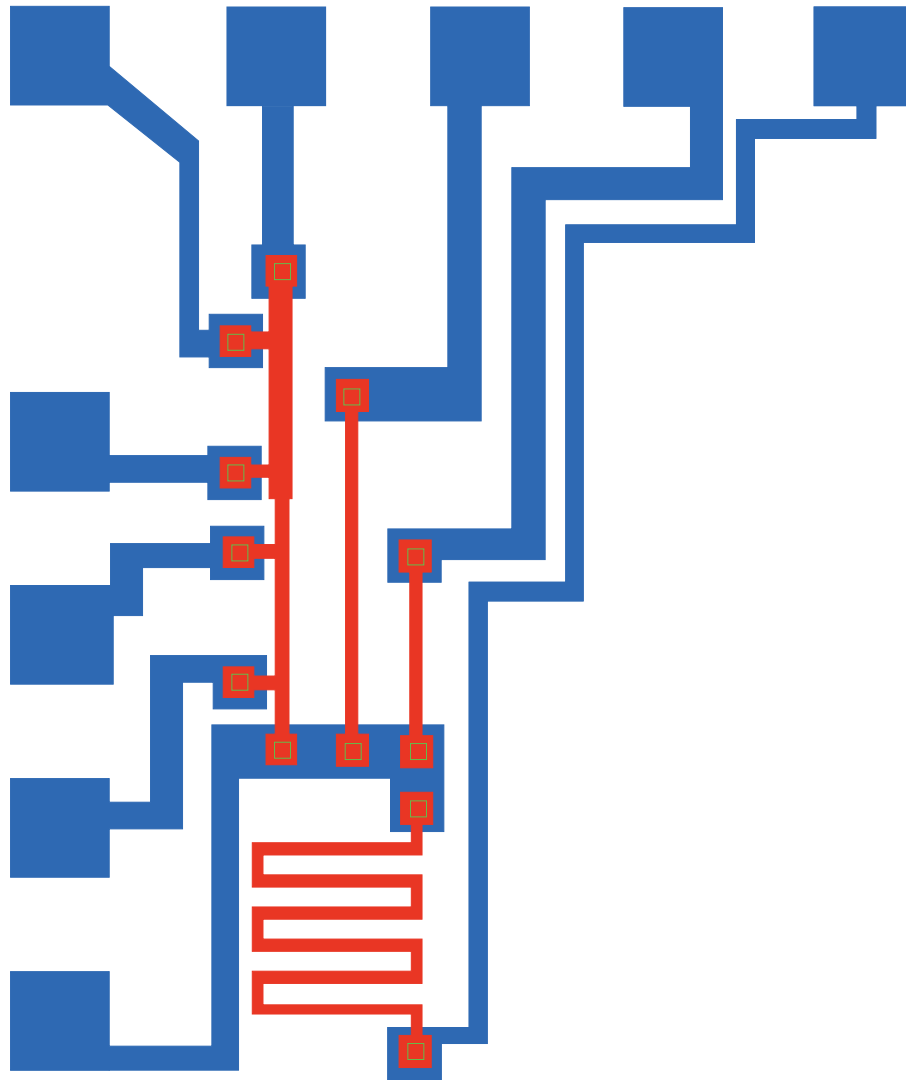
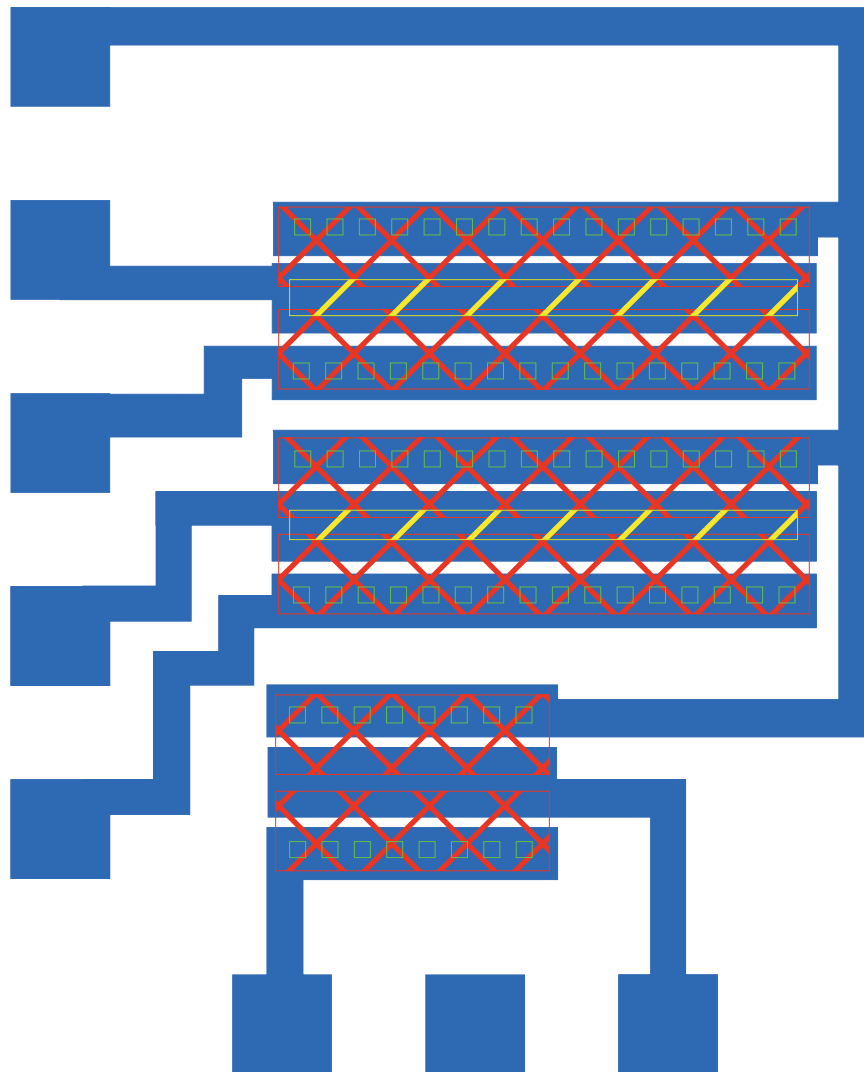


Figure 11: Composite view of resistor patterns of Holberg Mask Set; four levels are shown superimposed: diffusion: Level 1; diffusion: Level 2; contact: Level 3; and metal: Level 4.





**Figure 12: Composite view of MOSFET patterns of Holberg Mask Set; all four levels are shown superimposed.**

## Trouble Shooting During Device Testing

filename: TROUBLE

The device testing done in our lab is one of the most difficult parts of the class. This is because many of you are not accustomed to making measurements of truly unknown quantities. As discussed in the lab report section, we never really know what to expect from our fabrication process. Because the range of electrical characteristics that can result from nonideal fabrication is bewildering, you may feel overwhelmed by the data you collect during the test phase.

STEP ONE: DON'T PANIC!!!!

STEP TWO: **NEVER TAKE DATA BEFORE YOU UNDERSTAND EXACTLY WHAT YOU ARE MEASURING!!**

There are a number of very simple things you need to verify before making a measurement:

Do you have the wires connected correctly between probes and test instrument? to the **substrate chuck**? to the device itself?

These questions are not as simple as they may seem, and require that you really understand how to hook up a device. For an I-V measurement, one way to test the connections between probes and the test instrument is to try to form a "short circuit" at the probe tips (touch them together!). Since you know what the I-V curve of a short looks like (I hope), you can check your connections. Now try an open circuit. These are simple tests, but **very important**.

Once you have verified that you really have the right connections, what do you do if the device doesn't work? Obviously, I would ask: "**How** doesn't it work?" Is it a short? An open? A resistor when you expected a diode? A diode when you expected a resistor? This could go on forever, but you should be asking yourself these kind of questions. You really have to think about how devices work, but don't get too lost in elaborate semiconductor physics.

Another important thing to realize is **the order of your testing is important!** For instance, C-V measurements rarely make sense for devices that pass a large amount of dc current.

- For MOS capacitors this means an I-V measurement should be done to insure the caps are not leaky before any C-V measurements are attempted.
- For diodes, this means an I-V measurement must be performed to insure C-V is done only over a voltage range where the reverse bias leakage current is small.

Note you cannot even make I-V measurements unless you know you have good ohmic contacts to the silicon. A good way to check this would be an I-V measurement between the backside and front-side "substrate" contacts to the chip. What does it mean if this gives a diode-like curve? A resistor-like curve? What **should** it be?

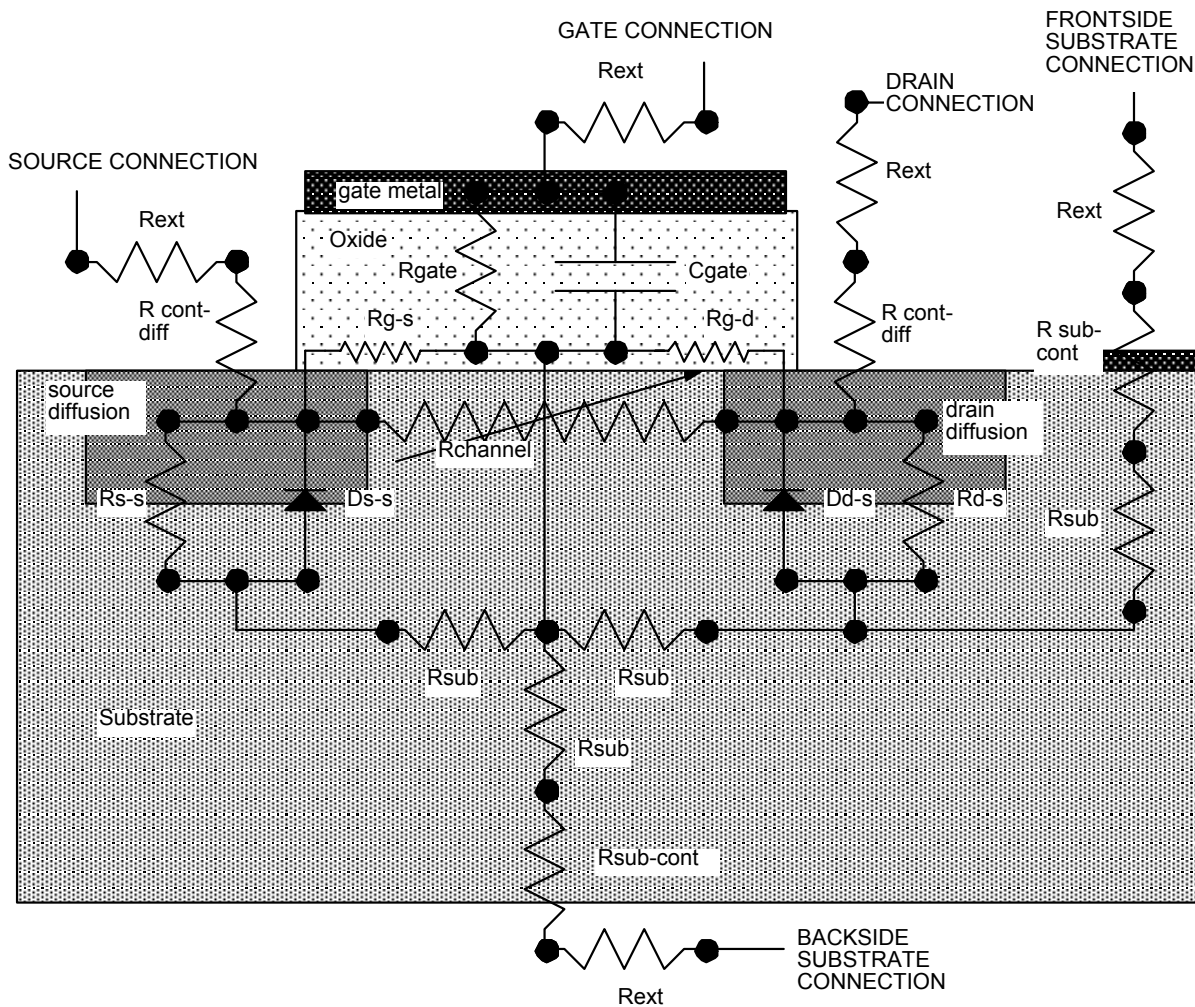
If a device doesn't work the way you "expected," you need a strategy to determine why it didn't work. For a MOSFET, the most useful approach is to look at the various components that make up a MOSFET. For instance, the source-substrate and drain-substrate form p-n junction diodes. A good check would be to measure the I-V curve of these diode "sub-components." What would happen to the MOSFET I-V curves if these junctions are leaky? What would happen to the curves if your source/drain contacts to the silicon exhibit very high resistance? Even if everything is fine with the device, you may still have hooked it up wrong; for instance, what would the I-V curve look like if you select the "wrong" polarity (with respect to the substrate) for the drain bias?

I recommend the following procedures:

- **Before doing any C-V measurements, do I-V testing on the devices to ensure that leakage currents are small.**
- **Don't collect large amounts of "strange" looking data, expecting you will be able to figure it out later.** Think about it while you are measuring, and try different tests to check for obvious errors (mis-connections, leaky diodes, bad contacts, etc.).
- **Do C-V on MOS capacitors before doing I-V on your MOSFETs.** This will allow you to determine what gate biases are needed to operate the MOSFETs.
- Think about the relationships between data seen in one type of device to other devices. How does diode I-V data help you understand MOSFETs? How does MOS cap C-V data help you understand the MOSFETs? What does resistor behavior tell you about diodes, and vice versa?
- **THINK!!!**

### How to find a "GOOD" MOSFET:

The following procedure could be used to ensure that you find a "good" MOSFET (or alternatively, find out what part of your MOSFET does **not** work). This sequence is designed to identify the sub-components of a MOSFET, as shown below. To measure a working MOSFET **all** the sub-components must work properly.



**Figure 13: MOSFET sub-components**

The sub-components are defined as follows:

8.  $R_{\text{ext}}$ : external parasitic resistances due to probe cables and connectors
9.  $R_{\text{sub-cont}}$  (frontside and backside): contact resistance between Al metallization and the undiffused (substrate) areas of chip
10.  $R_{\text{gate}}$ : resistance of gate oxide "insulator" to substrate under gate
11.  $C_{\text{gate}}$ : capacitance of gate oxide
12.  $R_{\text{g-s}}$  and  $R_{\text{g-d}}$ : resistance of gate oxide "insulator" to source and drain diffused regions (respectively) under gate
13.  $R_{\text{channel}}$ : gate voltage-controlled effective resistance of the channel region
14.  $R_{\text{cont-diff}}$ : contact resistance between Al metallization and the diffused areas of chip
15.  $D_{\text{s-s}}$  and  $D_{\text{d-s}}$ : diodes formed by source-substrate and drain-substrate p-n junctions
16.  $R_{\text{s-s}}$  and  $R_{\text{d-s}}$ : reverse-bias leakage "resistance" of source-substrate and drain-substrate p-n junctions
17.  $R_{\text{sub}}$ : substrate resistance

Most of us would recognize the essential feature of a MOSFET as the channel, whose equivalent resistance  $R_{\text{channel}}$  (i.e., the relation between the source-drain current and the source-drain voltage) is controlled by the voltage applied between the gate and the substrate. These characteristics are represented by the conventional family of  $I_{\text{ds}}-V_{\text{ds}}$  vs  $V_{\text{g}}$  curves for the device. However, for our "home-made" MOSFETs, the characteristics of all the other sub-components must also be verified. The various structures fabricated with the Holberg mask set should allow you to check each part of the device in turn.

If you understand how a MOSFET works, then you should know what an approximately "proper" value is for each. Here is a check list; indicate with a check mark what value you should get for each sub-component:

**Table 8: Trouble shooting checklist**

Sub Components	Resistance Value			
	Open	high	low	short
$R_{ext}$				
$R_{sub-cont}$				
$R_{gate}$				
$R_{g-s}$				
$R_{g-d}$				
$R_{cont-diff}$				
$R_{s-s}$				
$R_{d-s}$				
$R_{sub}$				

For the diode sub-components (assuming the substrate is the grounded reference), we should also determine which polarity is forward bias, and which is reverse. In the following table, indicate whether a positive (+) or negative (-) voltage should be applied to the diffusion contact to achieve the indicated bias condition. Also indicate whether the junction should exhibit a high or low resistance under the given bias condition.

**Table 9: Diode checklist**

sample	forward bias		reverse bias	
	polarity	resistance	polarity	resistance
p-type substrate, n-type diffusion				
n-type substrate, p-type diffusion				

Now that you have filled in the tables, you know what to look for as you take data. As I said earlier, it is extremely important to examine your data as you take it to see if it is reasonable. The rest of our procedure will be designed to measure each sub-component, ideally one at a time. Some components are almost always connected together, so we may need to be creative in trying to isolate their individual contributions to the measurements.

It is also critical to determine whether a measurement made on one device can be assumed to hold for another, i.e. we need to check for uniformity. For instance, if you find that one p-n diffused diode is "OK," can you assume all the MOSFET source-substrate and drain-substrate p-n junctions are also OK? You need a quick strategy to check for "qualitative uniformity." For this example, one way is to check several p-n diodes; they must ALL have I-V curves which are qualitatively similar. If even one is "bad," since your sample was probably small, the chance of another p-n junction being bad is HIGH! In such a case you will have to individually qualify a single MOSFET, and make **all your measurements on that SAME device.**

## MOSFET QUALIFICATION PROCEDURE:

STEP 1: Check  $R_{ext}$ : Obviously, you have to make sure the hook-up between measurement instrument and device. You should do this both visually and electrically (for instance, by either shorting or opening appropriate connections).

STEP 2: Check  $R_{sub-cont}$ : We must have an **ohmic** contact to the substrate to make any further measurements. One way is to try to measure an I-V curve between the frontside and backside substrate contacts. It should be linear through the origin, NOT a Schottky-like curve.

STEP 3: Check  $R_{cont-diff}$ : This is actually very hard to do quantitatively. We have one device on the chip (in the lower center area of the die shown on p. 44) called a Kelvin structure which is specifically designed for contact resistance measurement. At present we are not using this device, but instead use the diffused resistors to estimate  $R_{cont-diff}$ . The I-V measurements discussed on p. 64, along with the analysis on p. 69 should be used estimate  $R_{cont-diff}$ . You should also do a quick check now to see if the diffusion sheet resistance extracted from the resistors compares well with your four-point probe measurements made on the MPTs.

STEP 4: Evaluate p-n junctions: This should help establish the characteristics of  $D_{s-s}$  and  $D_{d-s}$  (and thereby  $R_{s-s}$  and  $R_{d-s}$ ). Start with I-V measurements on the diffused diodes, p. 64. In addition, set up to measure I-V between the source of your target MOSFET and the substrate; it should look similar to your diode curves. Same thing for the drain-to-substrate I-V. **These measurements can be made with the curve tracer.**

STEP 5: Check  $R_{gate}$ ,  $R_{g-s}$ , and  $R_{g-d}$ : Here we want to determine if gate oxide leakage is a problem. Start with I-V measurements of your MOS Caps, p. 65, done using PicoPete. Also check your target MOSFET, measuring I-V between the gate and substrate, gate and source, and gate and drain.

Assuming all the measurements made above are sensible, we are now ready to progress to C-V measurements

STEP 6: Check  $C_{gate}$ : Start by measuring the C-V characteristics of a MOS Cap which I-V has shown to have low leakage. See p. 67. Make sure you look at more than one, and determine the gate voltage range over which the MOS Cap goes from accumulation to depletion. This should establish the polarity of the threshold voltage  $V_t$ , and the range over which  $V_g$  should be swept when you go back to I-V measurements of the MOSFET.

STEP 7: You are now ready (finally) to measure the family of  $I_{ds}$ - $V_{ds}$  versus  $V_g$  curves which characterizes your MOSFET. See p. 65. Please make sure to save at least one set of curves for your lab reports. Also make sure to make the transconductance measurement.



**Device Testing: FOR REFERENCE ONLY!!!!!!!!!!!!!! DO NOT DO ALL THE TESTING DESCRIBED BELOW!!!!!!!!!!!!!!!!!!!!!!**

Required Pre Lab Reading: Trouble Shooting, p. 56; OP-Q, Tektronix Curve Tracer; OP-M, Capacitance-Voltage Measurements

Because of limited test equipment each group must schedule their testing time independently. There are a large number of measurements to make, and a great deal of data to analyze. You must work efficiently to get everything done. In addition, make sure you **read the post-lab questions now and begin to think about them.** Where you feel it is necessary you may use any text books or reference works, but you MUST REFERENCE ALL FORMULAS OR EXPLANATIONS YOU FIND IN THESE WORKS.

**PLEASE read the section on trouble shooting (p. 56).** You can take an enormous amount of data which is utterly meaningless if you are not careful! **Never take data you don't understand, assuming you'll come back someday and think about it.** I guarantee you'll never get around to it, you'll just end up with a very thick pile of garbage. Don't attach this to Lab Report III, expecting I'm going to figure it out for you. Understand your measurements as you do them: spend your time **thinking**, not simply generating numbers! **You MUST complete the procedure for trouble shooting, BEFORE continuing with the complete device testing procedures.**

**CAUTION: THE MICROMANIPULATOR PROBE TIPS ARE VERY SHARP, AND VERY FRAGILE.** You MUST be extremely careful not to strike the needles against one another or the substrate chuck. It is very easy to bend the tips, making them useless for your measurements. The devices you are probing are fairly small, and only sharp tips will be able to contact them. When you lower the tips to contact your chips be very gentle; you should use the minimum amount of tip pressure necessary to ensure contact. **Due to optical injection effects you must make all your measurements in as nearly dark as possible. Make sure you turn the microscope illuminator OFF before making any measurements.**

**Please use the sign-up sheets posted on the Lab doors to reserve the curve-tracer and C-V system.** Sign up in your own lab period slots if possible; do not sign up for more than one period at a time on each system.

**Note: We have / are changing software, so the references to the program PCASP below may be obsolete!!**

**CHECK FOR UPDATES ON REQUIRED MEASUREMENTS BEFORE  
PROCEEDING!**

## Part I Current-Voltage Measurements

### A) Diffused Resistors

On your n-type and p-type substrates measure:

1. For one "good" R2 resistor measure the I-V curve of the resistor at low voltages using PicoPete. Check at small voltages for linearity as V crosses zero. Make a qualitative sketch of your results. The substrate should be floating for these measurements.
  2. For the R1, R2, and R3 resistors measure the total resistance of:
    - i) Two resistors near the center of the chip.
    - ii) Two resistors near each edge of the chip. Make sure to note the location on the chips of each resistor, along with its resistance.
- \* Use the probe station connected to the DMM for these measurements.\* This will only work if your ohmic contacts are OK; see step 1 above for linearity near zero bias.**

This data will be used to determine sheet, contact, and bend resistances, as well as doping uniformity.

3. Connect a current source between the I1 and C terminals, then measure the voltage drop between the V1 terminals, and between the V2 terminals. Check for several currents. This data can be used to check the resistance per square using a four-point type measurement, largely free from contact resistance effects

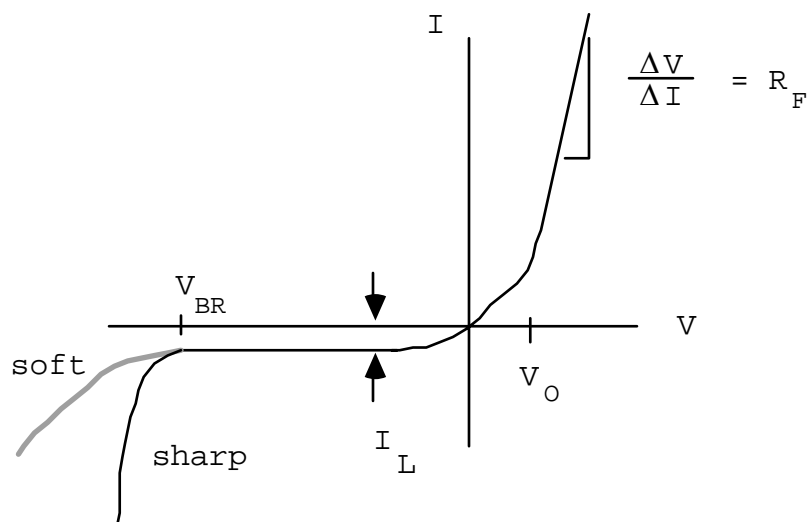
### B) Diffused Diode

[Note: You should remember which diode you probed, and if possible use this same diode for C-V measurements.]

On your n-type and p-type substrates measure:

1. A complete I-V curve for one good diode. You should be able to extract the following parameters: forward resistance,  $R_F$ , breakdown voltage,  $V_{BR}$ , reverse leakage current,  $I_L$ , and turn on voltage,  $V_O$ . The breakdown voltage is the voltage required for a leakage current of  $10 \mu A$ .  $I_L$  is measured at  $V_{BR}/2$ . See diagram on next

page. Use **PicoPete** for these measurements. I suggest outputting your data in table format for future calculations.



**Figure 14: I-V PARAMETERS FOR DIFFUSED DIODE**

### C) MOS Capacitors

On each of your samples check for leakage currents with a sweep of about  $\pm 20V$  applied to the metal electrode. Check several capacitors without guard rings on each chip. Make sure you know which ones are either shorted or leaky, if any. Use **PicoPete** for this. **Do this quickly; your main objective is to qualitatively determine if your caps are unusually leaky. We do NOT need to see these curves in your lab reports, but we do want a number for leakage current at 10 V bias.**

### D) MOSFET (Use PicoPete for this)

See OP-Q for measurement details. The MOSFET layouts are shown on p. 55.

Normal connections to PicoPete are: short source and substrate together, connect to ground; connect drain to  $V_A$  (this is the bias line which PicoPete sweeps and simultaneously measures current in); and connect gate to  $V_B$  (this is the "BIAS VOLTAGE" line which Pete can step through).

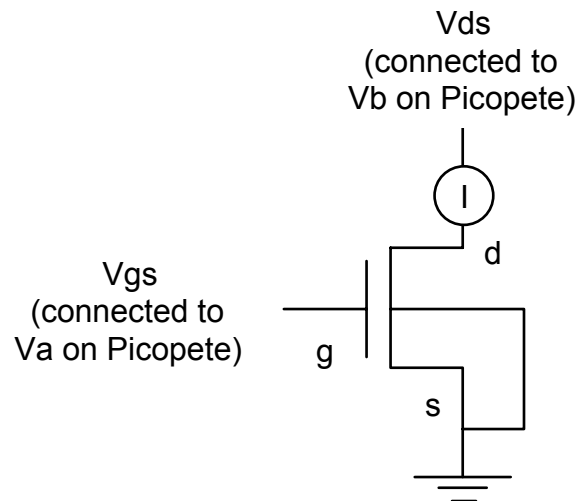
For each substrate:

1. Find the maximum transconductance and threshold voltage at max  $g_m$  of at least three MOSFET's on each chip.

First obtain the family of curves describing the MOSFET operation. Connect PicoPete to your devices as discussed above. Start with a gate voltage range (i.e. "BIAS VOLTAGE" in PCASP General I-V Menu) of about -3 V to 0 V, in 5 steps. **See TAs for updates on parameters to use with PCASP.** We do NOT need to see all of these curves in your Lab Reports; this is to determine qualitatively whether you are probing a good MOSFET. We do want you to save one "representative" set of curves.

Now measure  $g_m$  and  $I_{ds}$  vs  $V_{gs}$ :

Change the connections to the MOSFET as indicated below.



You can do this by simply swapping the BNC connections to  $V_A$  and  $V_B$  on PicoPete. You can now use the PCASP general I-V measurement to measure the  $I_{ds}$  vs  $V_{gs}$  curves of your MOSFETs. Selection of the differential output conductance option will directly measure  $g_m$ , while the I-V option will give us  $V_t$ . See pp. 34 below for parameter extraction techniques.

Suggested starting values:

- a) Set Source Voltage range to -5 to +5 V; set number of intervals to ; set Bias Voltage to 0.1 V.
- b) Select IV curve Table, output to printer; IV Graph, output to Screen.
- c) Select Differential Output Conductance Table, output to printer; Differential Output Conductance Graph, output to screen. Now perform measurement.

For ONE good MOSFET on each chip, output the IV and Differential Output Conductance curves to the plotter for your lab reports. They should look approximately as those posted in the lab.

Note: You can do all this very rapidly by measuring one device, then raising all the probes using the z- axis adjustment ONLY, translating the substrate to bring another device under the probes, and finally lowering the probes into contact with the new device. Summarize the data in a table.

Note: Your p-type substrates may yield MOSFET's that are conducting at  $V_{gate} = 0$ , and may require the application of a negative gate bias to turn them off. See the TAs for recommendations.

## Part II Capacitance - Voltage Measurements

### A) Diffused Diode

On your n-type and p-type substrates:

1. Find a good diode by quickly measuring the capacitance- voltage curves for several devices. A good diode should have its maximum capacitance at about  $V=0$ , and it should decrease with increasing REVERSE BIAS (see the introductory section to OP-M). If you have already done your I- V measurements, use the diode you used there. Don't save this; this is just to locate a good diode.

Measure the C-V curve from 0V to 10V (reverse bias - you may have to reverse the LO and HI connections to the capacitance meter). Use PCASP to set up this measurement. Use the diode data acquisition and analysis screen, and output only the doping profile.

### B. MOS Capacitors

On your n-type and p-type substrates:

1. Look at two capacitors near the edges, and two near the middle of each chip. For each cap perform the following:

Quickly measure the C-V curve from about -10V to +10V (where our convention is to measuring the polarity of the Al electrode with respect to the substrate) for your capacitors. Use the PCASP MIS Capacitor Analysis menu, and select Output Raw CV Data, graph to screen. Once you have a "good" cap, **output the C-V curve to the plotter**. Use PCASP to perform doping profile and flat band analysis on each capacitor. To get good doping profile results, select a source voltage range to take about 10 data points across the transition region from accumulation to depletion. For

the flatband analysis select  $C_{\max}$  and  $C_{\min}$  voltages to be  $\pm 10\text{V}$  (polarity appropriate to p or n type chip). Make sure to note the location on the chips of each capacitor. These results will be used to check the substrate background doping and oxide thickness uniformity of your chips.

2. Repeat for capacitors with guard rings. Be careful about the difference in areas for the caps with guard rings.

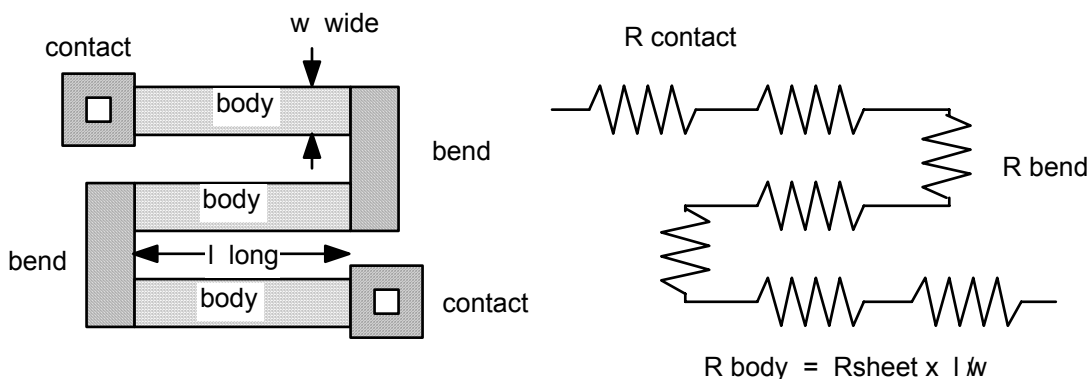
THIS CONCLUDES THE DEVICE MEASUREMENT SECTION

Questions related to device testing:

**Remember to be careful about significant figures and error estimates when filling out the Tables!!**

### A) Diffused Resistor

A simplified schematic of a diffused resistor is shown below. The total resistance is made up of three contributions: the body resistance  $R_B$  found from the number of squares and the sheet resistance of the main sections of the resistor; the bend resistance  $R_{BND}$  due to current crowding around corners in serpentine resistors; and the contact resistance  $R_C$ , due to current injection at the ends of the resistor.



Using the measurements made earlier we can determine the different contributions to the resistance of our devices. For a straight resistor (i.e.  $R_1$  and  $R_2$  on our chips) simple algebra gives both the sheet resistance  $R_S$  and the contact resistance  $R_C$ :

$$R_S = \frac{R_2 - R_1}{N_2 - N_1}$$

$$R_C = \frac{R_2 - N_2 R_S}{2} \quad \text{or} \quad R_C = \frac{R_1 - N_1 R_S}{2}$$

where

- $R_1$  = measured resistance of resistor 1
- $R_2$  = measured resistance of resistor 2
- $R_S$  = sheet resistance due to diffusion
- $R_C$  = contact resistance
- $N_1$  = number of squares in body of resistor 1
- $N_2$  = number of squares in body of resistor 2

Compare the  $R_S$  from the resistors to the  $R_S$  from your MPT chip measurements. Comment on the differences. Also compare your measurement of  $R_C$  to the formulas given in Gandhi (pp. 628-629).

We can find the effective resistance of bends (one complete fold-over) using the data found for contact and sheet resistances:

$$R_{BND} = \frac{R_3 - 2R_C - N_3R_S}{N_B}$$

where

$R_3$  = measured resistance of resistor 3

$R_S$  = sheet resistance due to diffusion

$R_C$  = contact resistance

$N_3$  = number of squares in body of resistor 3

$N_B$  = number of fold-overs in resistor 3

$R_{BND}$  = effective resistance of bend

We can then find the "effective size" of a bend  $L_{BND}$  (measured in squares) using

$$L_{BND} = \frac{R_{BND}}{R_S}$$

Compare your measurements to the formulas given in Gandhi (pp. 628-629). Use this information to complete Table II.

2. Based on your resistor measurements, can you tell if the doping is uniform across the face of the chip? Comments?



## B) Diffused Diodes

1. C-V data analysis: [NOTE: we have/are changing programs for the CV section, so PCASP may not be available]

Recall that

$$C = A\epsilon_{OX}/x_d$$

where A = area of diode (get this from the Holberg Masks) and  $x_d$  = depletion layer width.

PCASP uses your C-V data to calculate  $x_d$  vs. V. Assuming

$$x_d = BV^n$$

PCASP can find B and n. For an abrupt, one-sided junction we expect the value of n above to be 1/2. Under these conditions the doping at  $x_d$  is given by

$$N(x_d) = \frac{-2}{q \epsilon_S \left[ \frac{d(1/C^2)}{dV} \right] A^2}$$

PCASP can use this model to calculate the substrate doping,  $N_B$ , as a function of depth into the sample. How does this value of  $N_B$  compare to the substrate doping measured from your MPT chips? Why can't we obtain (much) information about the diffusion doping profile with these measurements? Use this data to complete Table III.

2. I-V data analysis

A standard way to analyze diode characteristics is to try to fit the I-V curve to the ideal diode equation

$$I = I_o \left[ \exp\left(\frac{qV}{nkT}\right) - 1 \right]$$

where n is the ideality factor. Plot your I-V data on a semi-log scale, i.e.  $\ln(I)$  vs V. **Under what conditions (i.e. what voltage bias range) is the slope of a real I-V curve related to the ideality factor?** What ideality factor does your diode give? What is  $I_o$ ?

## C) MOS Capacitors

1. Use the PCASP C-V doping profile results to determine the background doping concentration in your chips. For each cap measured, find the average doping concentration over the measured depletion width. Use this information to complete Table III.

2. From the PCASP C-V flat band analysis measurements, find  $t_{OX}$ , and determine how uniform the oxide thickness is across your chips. Compare the calculated oxide thickness here to your MPT oxide measurements. Use this data to complete Table I (note that the index of refraction given by the ellipsometer is  $\sqrt{\epsilon_r}$ , measured at the He-Ne laser wavelength, while  $\epsilon_r$  given by C-V is measured at 1 MHz). Also use this information to complete Table ???. Please give the excess surface charge  $Q_{OX}$  in units of number density, i.e.  $\#/cm^2$ , NOT IN COULOMBS/cm<sup>2</sup>. Comment on possible sources of this excess charge.

## D) MOSFET

1. Use the PCASP Differential Output Conductance Tables to find the maximum transconductance  $g_m^{max}$  of your MOSFETs. Use this data to complete appropriate entries in Table V. Include one representative plot in your lab report.

A very simple estimate of the transconductance expected from your MOSFETs is given by

$$g_m = \mu C_{ox} \frac{W}{L_{eff}} V_{ds}$$

where for an

$$\text{n-channel device } \mu = \mu_n \cdot 1400 \text{ cm}^2/\text{Vsec}$$

$$\text{p-channel device } \mu = \mu_p \cdot 500 \text{ cm}^2/\text{Vsec}$$

and

$$C_{ox} = \epsilon_r^{oxide} \epsilon_0 / t_{ox}$$

$W$  = width of the MOSFET gate

$L_{eff}$  = effective channel length

$V_{ds}$  = drain-source bias used in your measurement.

Using the Holberg masks and the other information (such as the gate oxide thickness  $t_{ox}$ ) you have, calculate the  $g_m$  of your MOSFETs; use this information to fill out Table V. Comments on differences?

2. One way to define the threshold voltage of your MOSFETs is to use the  $I_{ds}$  vs  $V_{gs}$  measurements described on p. ??. We will use the convention that

$$V_t = 2 V_{g1} - V_{g2} - \frac{1}{2} V_{ds}$$

where  $V_{g1}$  is the gate voltage necessary to achieve  $I_{ds}$  of  $100\mu A$ , and  $V_{g2}$  is that necessary to achieve  $200\mu A$ . You set  $V_{ds}$  when you made your measurements (I suggested  $0.1V$ ; if you changed it use the new value). Using the tables of  $I_{ds}$  vs  $V_{gs}$  you measured, find  $V_t$  for each MOSFET measured. Use this information to fill out the appropriate parts of Table V.