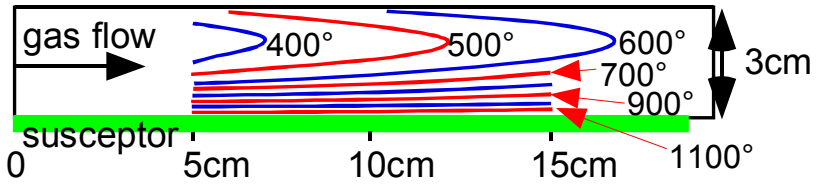
Epitaxy

- growth of thin crystalline layers upon a crystalline substrate
  - heteroepitaxy
    - dissimilar film and substrate
  - autoepitaxy
    - same film and substrate composition
- techniques
  - Vapor-Phase Epitaxy (VPE)
    - CVD: Metal-organic VPE (MOCVD, OMVPE, ...)
    - PVD: Molecular Beam Epitaxy (MBE)
  - Liquid-Phase Epitaxy (LPE)
    - mainly for compound semiconductors
  - Solid-Phase Epitaxy
    - recystallization of amorphized or polycrystalline layers
- applications
  - bipolar, BiCMOS IC's
    - 2-5 μm in high speed digital
    - 10-20 μm in linear circuits
  - special devices
    - SOI, SOS
    - HEMT, MODFET, HBT

Vapor Phase Epitaxy

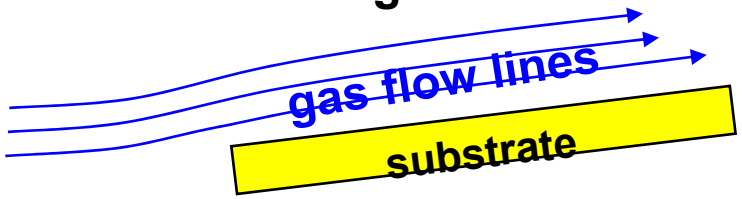
- **transport of reactants to the substrate from gas stream primarily laminar(uniform velocity) away from the substrate, parallel to substrate face**
  - **friction at surfaces forces gas flow velocity to be zero at substrate face**
    - **stagnant boundary layer at interface through which reactants must diffuse**
    - **causes concentration, temperature gradients between gas & substrate**

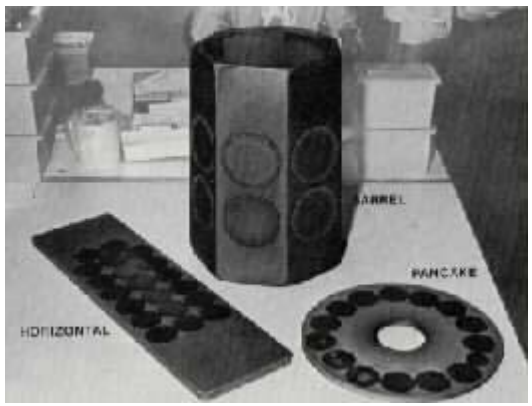


adapted from Sze, 2nd ed., p. 60.

T_{sub} = 1200°C, v_{gas} = 50 cm/sec

- **tilt substrate to get uniform growth rates**





from Sze, 2nd ed., p. 68.

VPE System Design

- general requirements:
  - cleanliness essential
    - particle
    - gas purity (H_2 typically 99.9999%)
  - precise control of gas flows necessary
  - provision for in situ etch
  - substrate mounting and slice carrier designed to minimize turbulence
    - chamfer wafer edges
    - recess wafer slots
  - boundary layer control via tilted carrier to increase gas velocity as x increases
  - heating of susceptor via (cold wall)
    - induction
    - radiant lamps
- use of LPCVD:
  - increases boundary layer thickness for given gas velocity
  - produces good uniformity

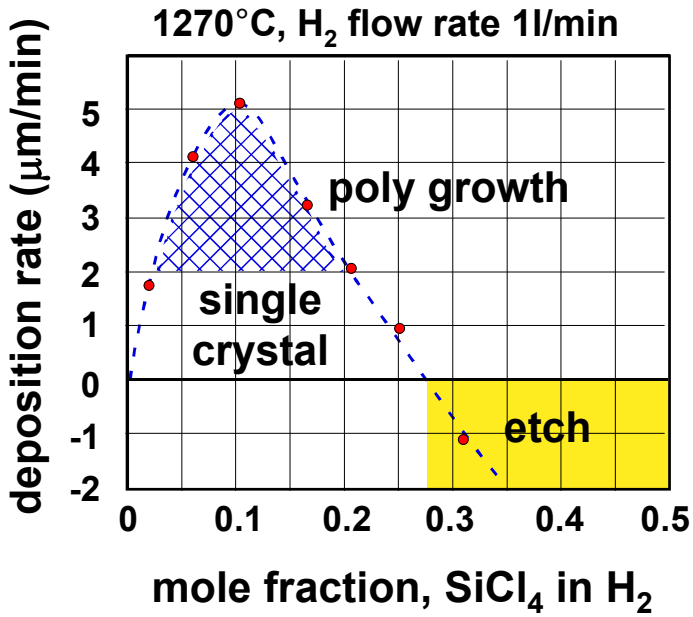
Silicon VPE chemistry

- hydrogen reduction of chlorosilanes:
  - silicon tetrachloride, $SiCl_4$
  - dichlorosilane, SiH_2Cl_2
  - trichlorosilane, $SiHCl_3$
- reaction paths: $T \geq 800^{\circ}C$
  - predominant species formed are HCl and $SiCl_2$; at temperatures between 1150-1250˚C

adapted from Ghandhi, 2nd ed., p. 298.

$$\underbrace{SiCl_2}_{adsorb} + \underbrace{SiCl_2}_{adsorb} \Leftrightarrow \underbrace{Si}_{solid} + \underbrace{SiCl_4}_{desorbs}$$

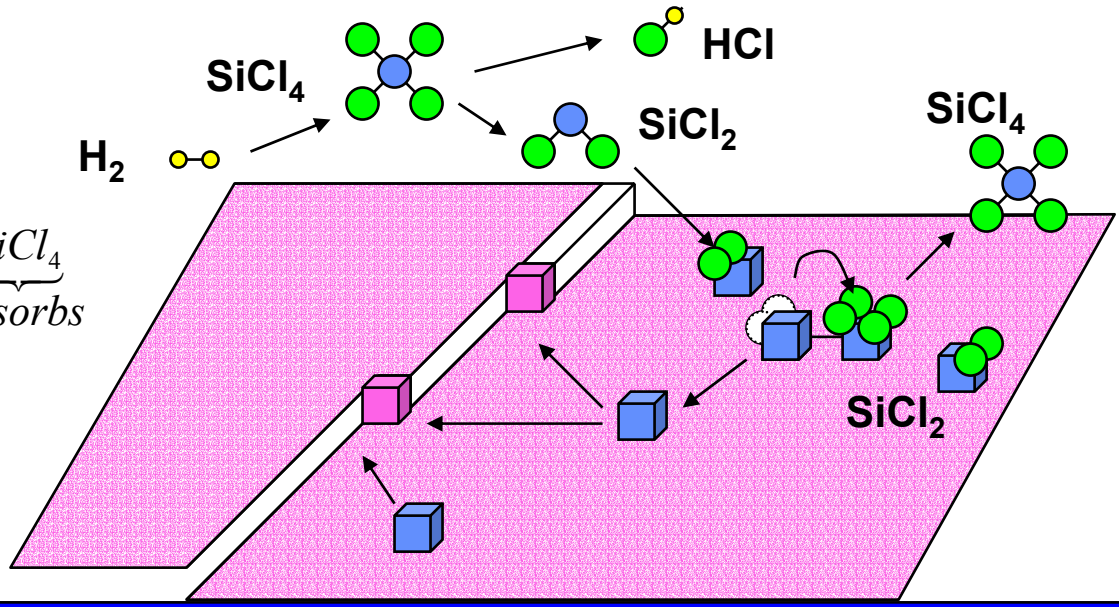
    - $SiCl_4$ reacts again in gas phase to produce HCl, $SiCl_2$
  - overall reaction:
    $SiCl_4 + 2H_2 \leftrightarrows Si + 4HCl$
- all these are reversible reactions
  - etching occurs if have $SiCl_4$ rich gas stream



Silicon VPE growth

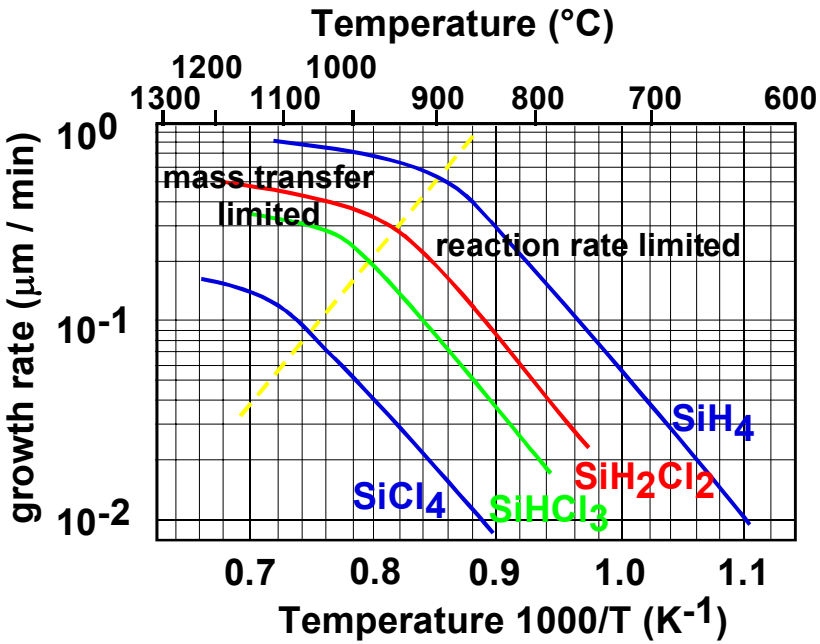
- **homogeneous nucleation**
  - **reactants combine to form isolated nuclei in gas phase, then attach to substrate surface**
  - **can cause poor crystal quality growth**
- **heterogeneous nucleation**
  - **reactants coalesce only on the surface where deposition occurs**
  - **note growth is lateral, not really vertical:**
    - **adsorbed species move rapidly by surface diffusion until they find a "kink," frequently a screw-type dislocation**

$$\underbrace{SiCl_2}_{adsorb} + \underbrace{SiCl_2}_{adsorb} \Leftrightarrow \underbrace{Si}_{solid} + \underbrace{SiCl_4}_{desorbs}$$



Deposition rate limiters

- reaction rate limited
  - growth rate limited by chemical kinetics
  - conventional exp(-E/kT) behavior
  - also depends on reactant partial pressures
- mass transfer limited
  - reaction rate very “fast” compared to diffusion across stagnant boundary layer
  - growth rate weakly dependent on temperature
- operate in the mass-transfer regime to prevent extreme sensitivity to temperature variations across and between wafers



adapted from Sze, 2nd ed., p. 62.

Comparison of silicon VPE sources

- silicon tetrachloride:
  - highest temperature required to produce $SiCl_2$
  - most stable chlorosilane
  - least deposited silicon per gas input
- trichlorosilane:
  - approx. 50˚C lower growth temperature
- dichlorosilane:
  - lowest temperature of chlorosilane processes
  - most efficient deposition per gas input
- silane:
  - have to be careful to avoid poly growth

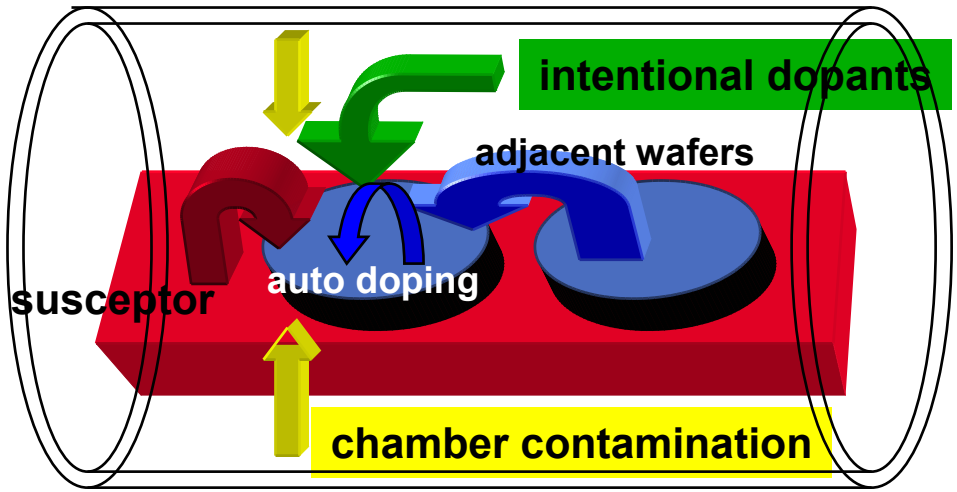
reactant	growth rate (μm / min)	temp. (°C)	allowed oxidizer (ppm)
$SiCl_4$	~0.4 – 1.5	1150 – 1250	5 - 10
$SiHCl_3$	~0.4 – 2	1100 – 1200	5 - 10
SiH_2Cl_2	~0.4 – 3	1050 – 1150	< 5
SiH_4	~0.2 – 0.3	950 – 1050	< 2

Typical process

- hydrogen backfill and flush
- reactor heating,
  - temperature equilibration
  - H_2 atmosphere, elevated temperature causes reduction (removal) of surface oxides
- in situ etch
  - HCl etch @ 1150-1200˚C for 5 min. to remove thin surface layer of silicon
- H_2 flush of HCl, set temperature for growth
- establish source gas, dopant gas flows

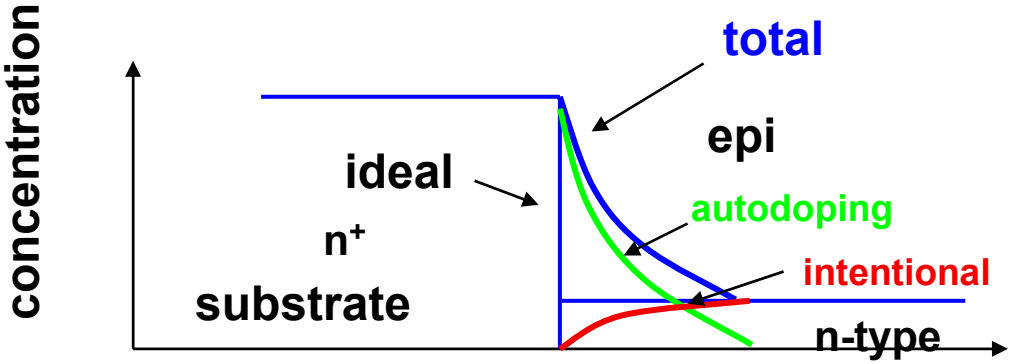
Doping and autodoping

- intentional dopants added to gas stream:
  - boron, B_2H_6
  - phosphorus, PH_3
  - arsenic, AsH_3
- in addition to intentional impurities have impurity introduction and redistribution:
  - sources
    - conventional diffusion in crystal
    - gas stream doping of epi due to evaporation of Si, dopants, reactor materials
- minimum background impurity concentration due to reactor, etc. contaminants $\approx 10^{14}/cm^3$

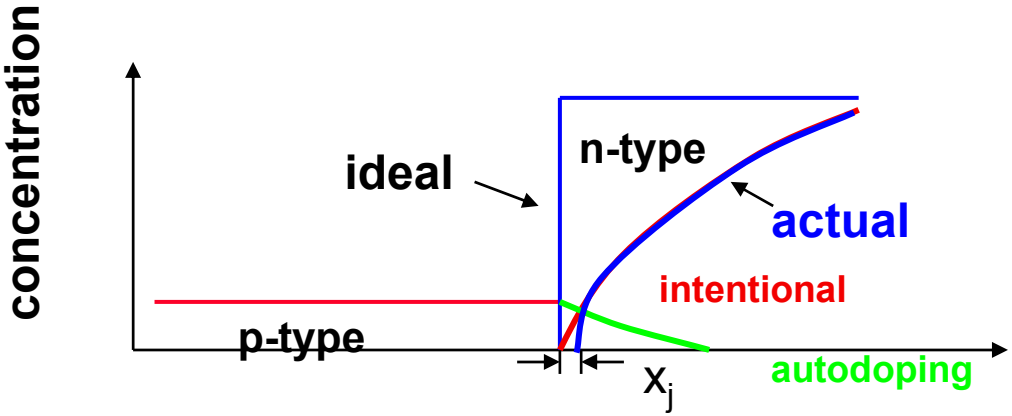


Autodoping

- in addition to reactor contaminants also have evaporation and diffusion of dopants from the wafers themselves.
- combined diffusion and evaporation-induced doping dominate the first ~2μm of epi growth
  - heavily doped substrate, lightly doped epi

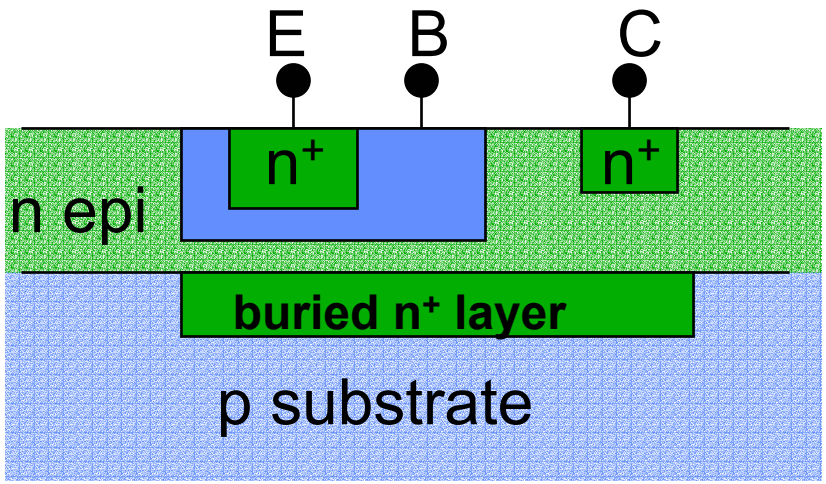


  - lightly doped substrate, opposite epi



Problems in bipolar design with epi

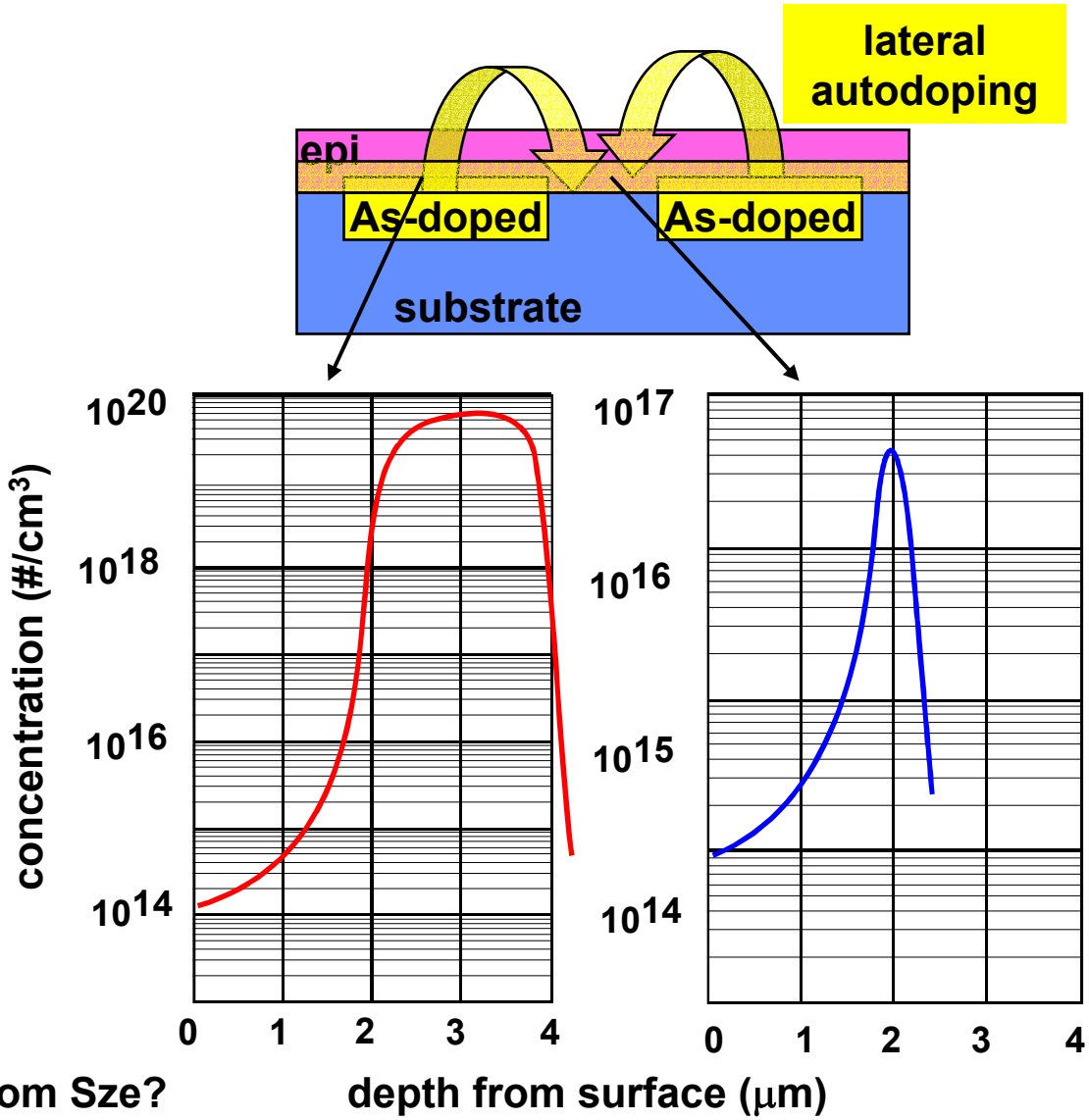
- typical, idealized configuration for n-p-n transistor:



- problems:
  - lateral autodoping
    - dopant from n+ regions evaporates into stagnant layer, diffuses laterally, dopes adjacent areas
  - pattern shift
    - growth process shifts position of steps on substrate

Lateral Autodoping

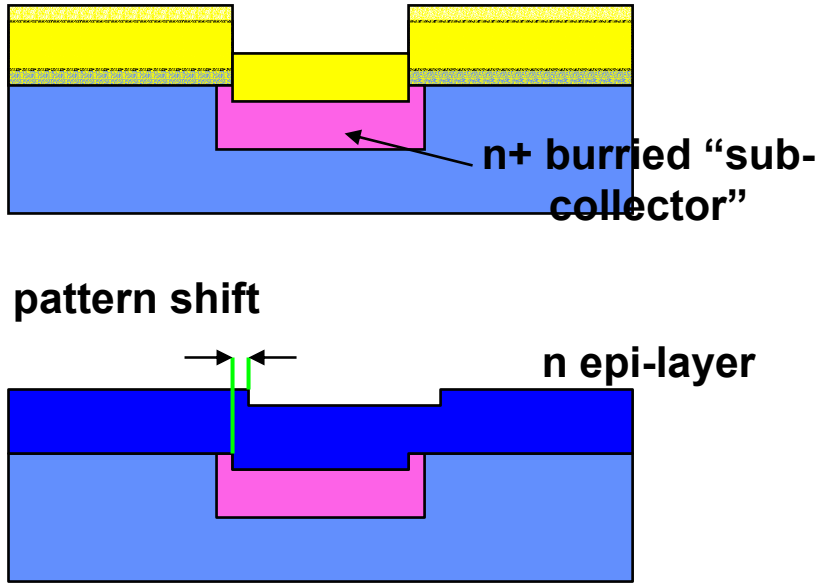
- worse for higher temperatures, lower growth rates
- decreases with decreasing pressure
  - increases vertical diffusion rates
  - lateral autodoping less important in LPCVD



adapted from from Sze?

Pattern Shift in Epi Growth

- in bipolar process:
  - 50-100 nm steps in silicon surface from initial oxide mask and from oxidation during drive of n^+ buried layer
  - must maintain steps for subsequent alignment
- during epi growth:
  - growth is lateral on microscopic scale
  - growth rate depends on crystal surface orientation
  - causes shift and distortion of buried layer pattern



- pattern shift:
  - increases with increasing growth rate and decreasing growth temperature
  - is minimized for:
    - <111> Si by misorienting surface by 2-5˚
  - worst case design rule:
    - shift = layer thickness

Heteroepitaxy

- growth of dissimilar film/substrate combination
- what do you need?
  - chemical compatibility
  - thermal compatibility
  - “crystal” compatibility
    - similar lattice structure
    - similar lattice constants
- examples
  - silicon-on-sapphire
    - violates lattice match
  - $Al_xGa_{1-x}As$ system

Silicon on Sapphire

- heteroepitaxial process, usually pyrolisis of silane at 1000˚-1050˚C, ≈ 1 μm thick
- sapphire chosen for high temperature, chemical stability
  - lattice mismatched at interface
  - aluminum silicate formed at interface
  - aluminum autodoping from substrate
  - thermal expansion coefficient mismatch
- high defect density:
  - stacking faults, misfit dislocations
  - density ≈ inverse with distance to interface
  - Very short minority-carrier lifetimes
    - cannot be used for bipolar IC's
- used only in MOS devices for
  - radiation hardness
  - latch-up immunity

Molecular Beam Epitaxy

- non-CVD vapor phase epitaxy via evaporation of material in ultra-high vacuum environment. By utilizing very low growth rates (≈ 1μm/hour) can tailor doping profiles and composition on a monolayer scale.
  - growth temperatures 400° - 800°C
  - background vacuum pressures ≈ 10^{-11} Torr
  - monolayer formation time > 2 days
  - silicon, SiGe, GaAs, AlGaAs, II-VI materials all grown
- machine design:
  - source materials evaporated from effusion cells
    - (Si MBE uses e-beam evaporators for Si source)
  - temperature control critical, up to 1600°C
  - beams interrupted with mechanical shutters to control composition and doping
  - all growth chamber surfaces cooled to LN2 temp to prevent impurity incorporation in films

Silicon Molecular Beam Epitaxy

- process requires:
  - ultra high vacuum system for deposition
  - very clean initial wafer surface
- flash decompose protective thin oxide in UHV @ 750-850˚C
- growth temperature 450-850˚C
- epitaxial materials grown:
  - silicon with very abrupt doping profiles
  - metal silicides: $NiSi_2$, Co_2Si, etc.
  - Ge_xSi_{1-x}/Si
- applications:
  - buried silicides to replace buried layers in bipolar
  - metal base transistor, permeable base transistor
  - HEMTs, HBTs, superlattice devices

Summary Slide

- Epitaxy
- Silicon VPE growth
- Doping and autodoping
- Pattern Shift in Epi Growth
- Heteroepitaxy
- Epitaxial Growth of GaAs
- next topic: metallization