Performance characteristics and the SIA Roadmap (1997)

- **transistor count**

Year of first product shipment	1997	1999	2001	2003	2006	2009	2012
Memory							
bits @ samples/intro	256M	1G	*	4G	16G	64G	256G
bits @ production	64M	256M	1G	1G	4G	16G	64G
Bits/cm^2 @ sample/intro	96M	270M	380M	770M	2.2B	6.1B	17B
DRAM chip size, mm^2	100 mm^2	140 mm^2	160 mm^2	200 mm^2	280 mm^2	390 mm^2	550 mm^2
Logic (high volume, cost sensitive)							
Logic transistors/cm^2 (packed, including on-chip SRAM)	3.7M	6.2M	10M	18M	39M	84M	180M
Microprocessor transistors/chip	11M	21M	40M	76M	200M	520M	1.4B
MPU chip size, mm^2	110 mm^2	125 mm^2	140 mm^2	150 mm^2	180 mm^2	220 mm^2	260 mm^2
Logic (low volume; ASICs)							
Usable transistors/cm^2	8M	14M	16M	24M	40M	64M	100M

Performance characteristics and the SIA Roadmap (1997)

- **performance**

Year of first product shipment	1997	1999	2001	2003	2006	2009	2012
Chip frequency							
on chip. local, high perf.	750 MHz	1.25 GHz	1.5 GHz	2.1 GHz	3.5 GHz	6 GHz	10 GHz
on chip, global, high perf.	750 MHz	1.2 GHz	1.4 GHz	1.6 GHz	2 GHz	2.5 GHz	3 GHz
on chip, cost sensitive	400 MHz	600	700	800	1.1 GHz	1.4	1.8
chip to board, high perf.	750 MHz	1.2 GHz	1.4 GHz	1.6	2	2.5	3
Max number of wiring levels	6	~7	7	7	~8	8-9	9

Performance characteristics and the SIA Roadmap (1997)

- **wafer, package dimensions**

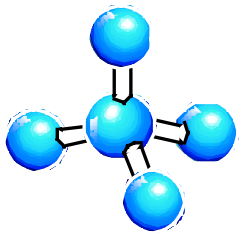
Year of first product shipment	1997	1999	2001	2003	2006	2009	2012
Lithography field size (mm x mm; mm^2)	22x22 484 mm^2	25x32 800 mm^2	25x34 850 mm^2	25x36 900 mm^2	25x40 1000 mm^2	25x44 1100 mm^2	25x52 1300 mm^2
Wafer diameter (mm)	200 mm (8")	300 mm (12")	300 mm	300 mm	300 mm	450 mm (18")	450 mm
Number of chip I/O's							
chip-to-package high performance	1490	2000	2400	3000	4000	5400	7300
"low cost"	800	975	1195	1460	1970	2655	3585
Number of package I/Os							
ASIC (high perf.)	1100	1500	1800	2200	3000	4100	5500
MPU, cost sensitive	600	810	900	1100	1500	2000	2700

Silicon Semiconductor Integrated Circuits

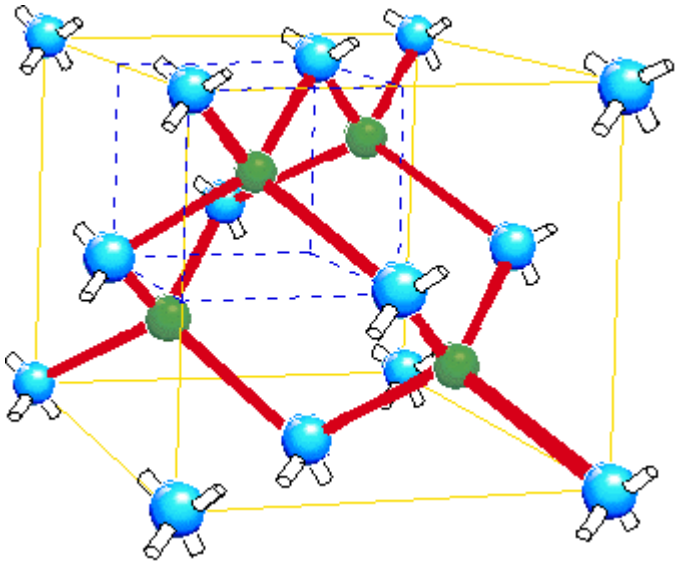
- Silicon makes up over 26% of the earth's crust, mainly in the form of silicon dioxide, SiO_2, more commonly known as sand or quartz
- For semiconductor use, the silicon must be purified so that there are no more than about ten impurity atoms to every billion silicon atoms
- Large diameter (> 8 inch), single crystal silicon boules weighing more than 100 lbs are routinely grown from a melt at over 2500˚F

What does silicon look like?

- **fundamentally, it looks like diamond!**
  - **each atom bonds to four neighbors in a tetragonal configuration**



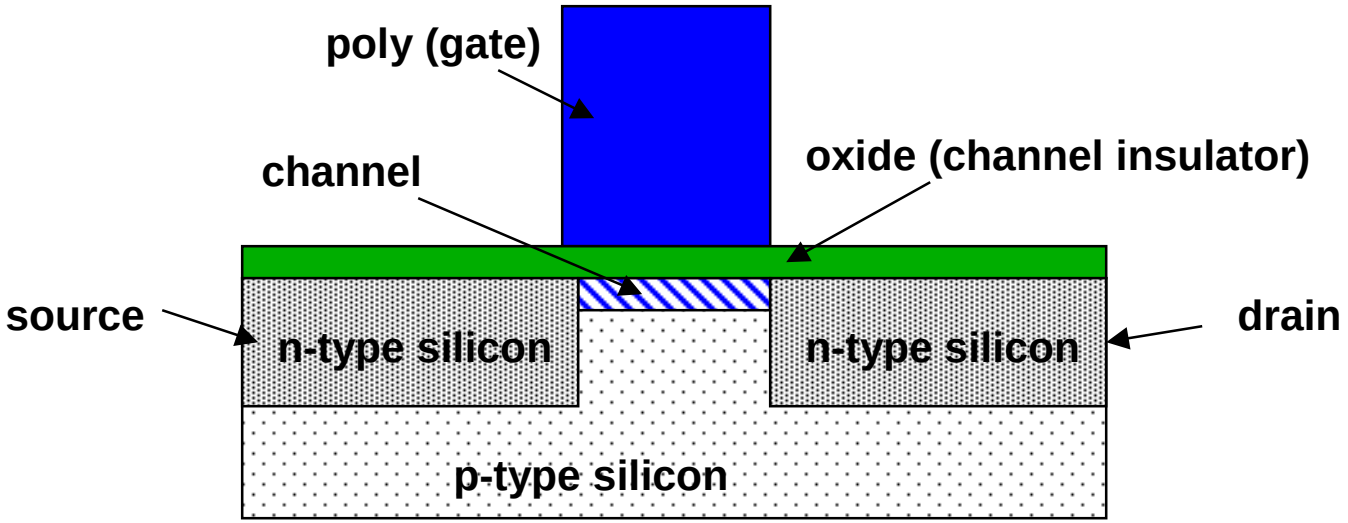
  - **the atoms are arranged into a face-centered cubic crystal structure**



picts

How to make a MOSFET

- What do you need?
  - a good semiconductor (SILICON)
  - a p-n junction (boron-doped Si - phosphorus-doped Si)
  - a good insulator (SILICON DIOXIDE)
  - a good conductor (poly-silicon and aluminum, copper)

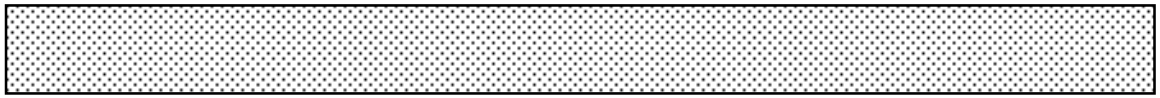


Silicon Device Processing

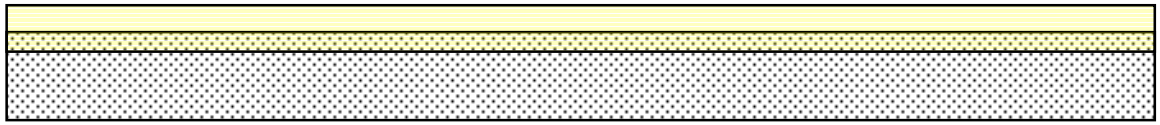
- **The construction of a silicon integrated circuit uses three basic processes:**
  - **Oxidation:**
    - **by heating silicon to about 2000^0 F in oxygen the surface of the silicon becomes silicon dioxide (glass), a very good insulator.**
  - **Photolithography:**
    - **is a way of producing a pattern of bare areas and covered areas on a substrate. This serves as a mask for etching of the silicon dioxide.**
  - **Diffusion:**
    - **is a process for the introduction of controlled amounts of impurities into the bare areas on the silicon (as little as one impurity atom per million silicon atoms). This allows the formation of p-n diodes in the substrate.**
- **When all these steps are combined, along with metal wires for connections between devices, an integrated circuit can be made.**

How to make a MOSFET

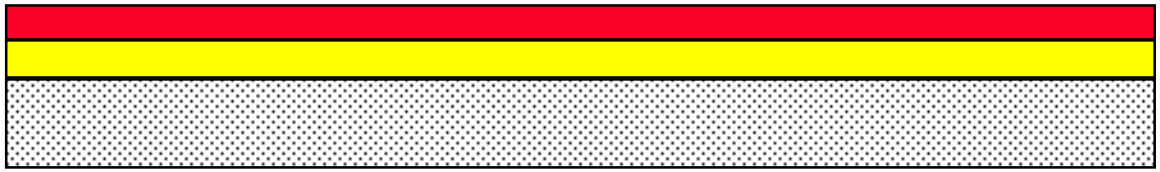
start: bare silicon wafer



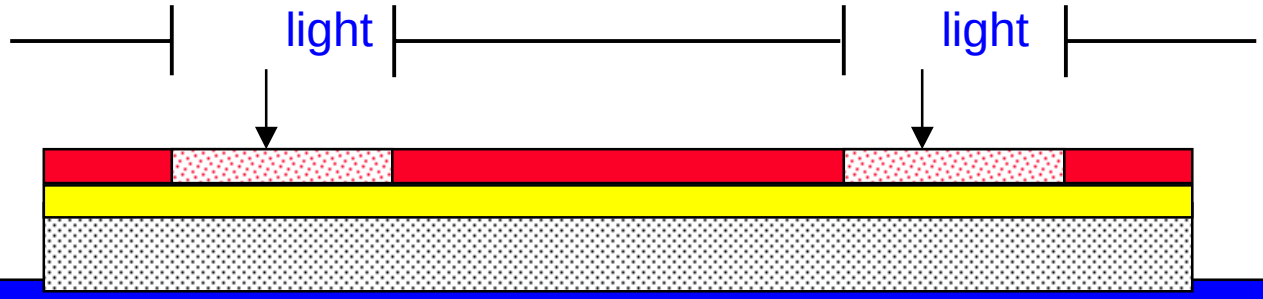
oxidize



apply *photoresist* (pr)

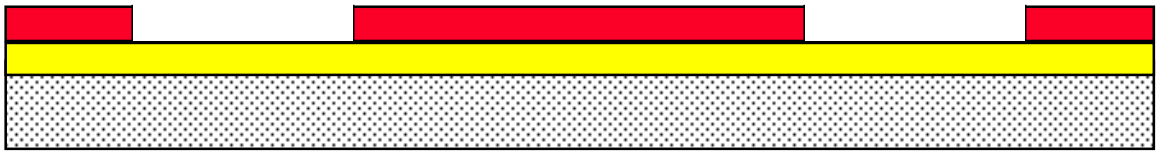


expose mask 1

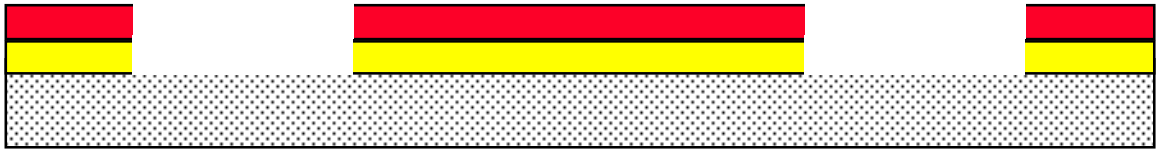


How to make a MOSFET

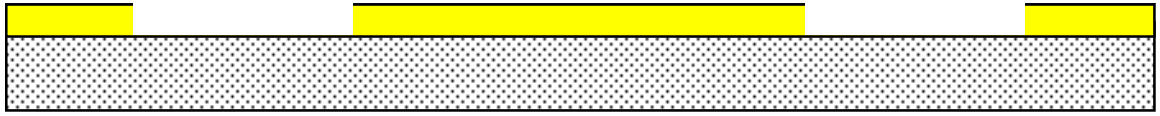
develop pr



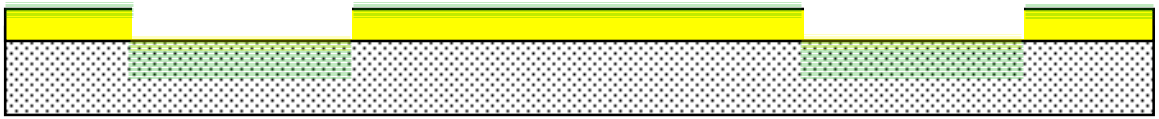
etch oxide



strip pr

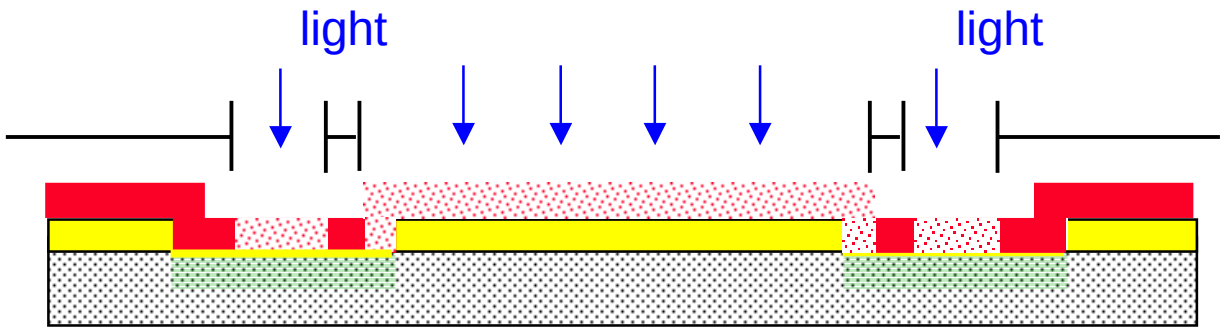


introduce source drain dopants



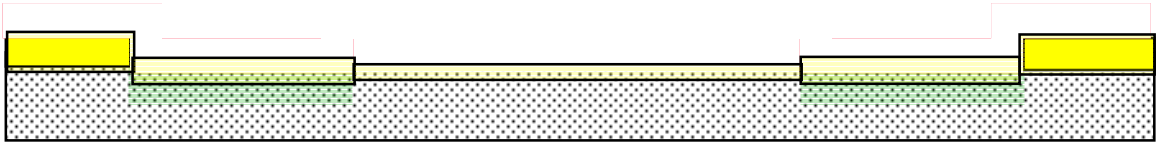
How to make a MOSFET

coat pr, align mask 2, expose mask 2



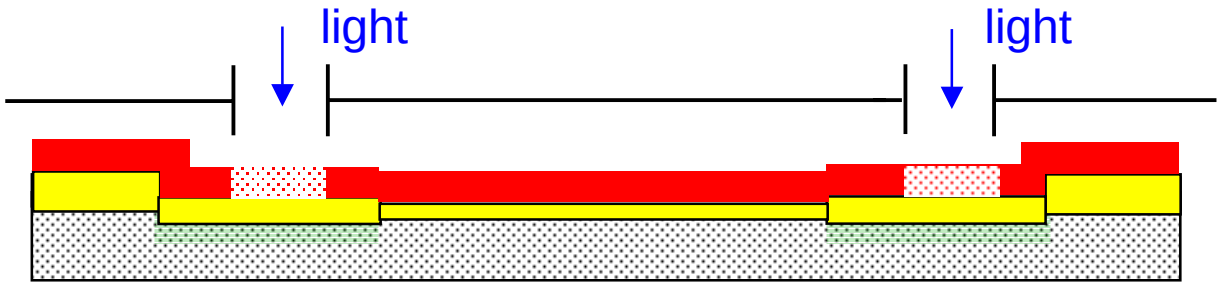
develop pr, etch oxide

strip pr, re-oxidize to form gate insulator

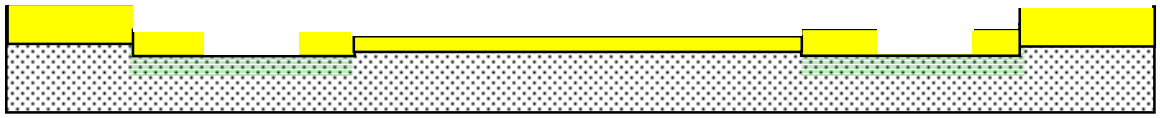


How to make a MOSFET

coat pr, align mask 3, expose mask 3

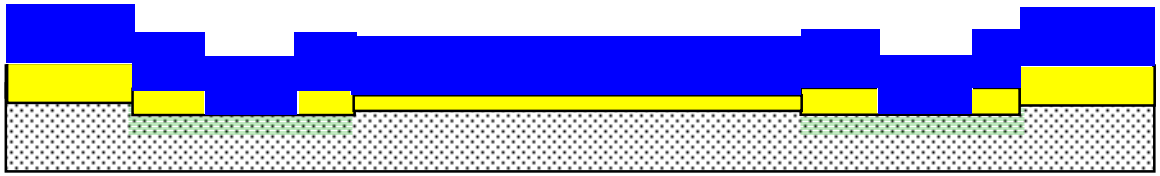


develop pr, etch oxide, strip pr

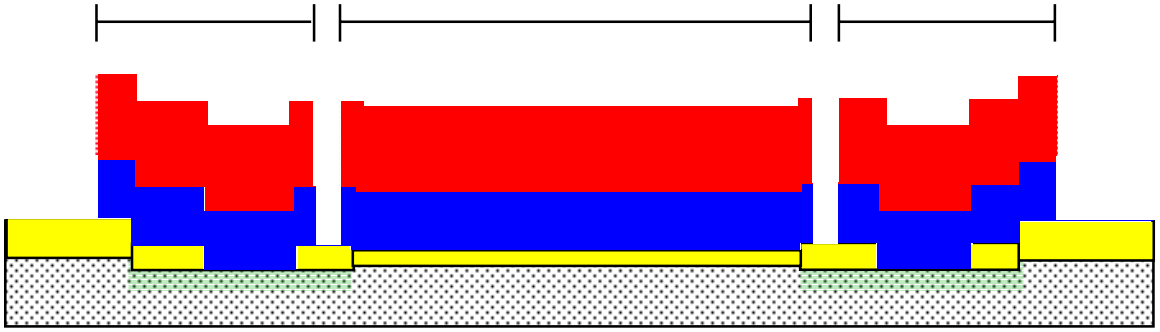


How to make a MOSFET

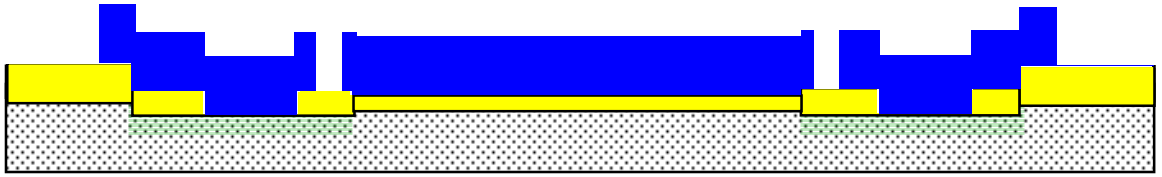
metallize,



coat pr, align mask 4, expose, develop pr, etch metal



strip pr: FINISHED!

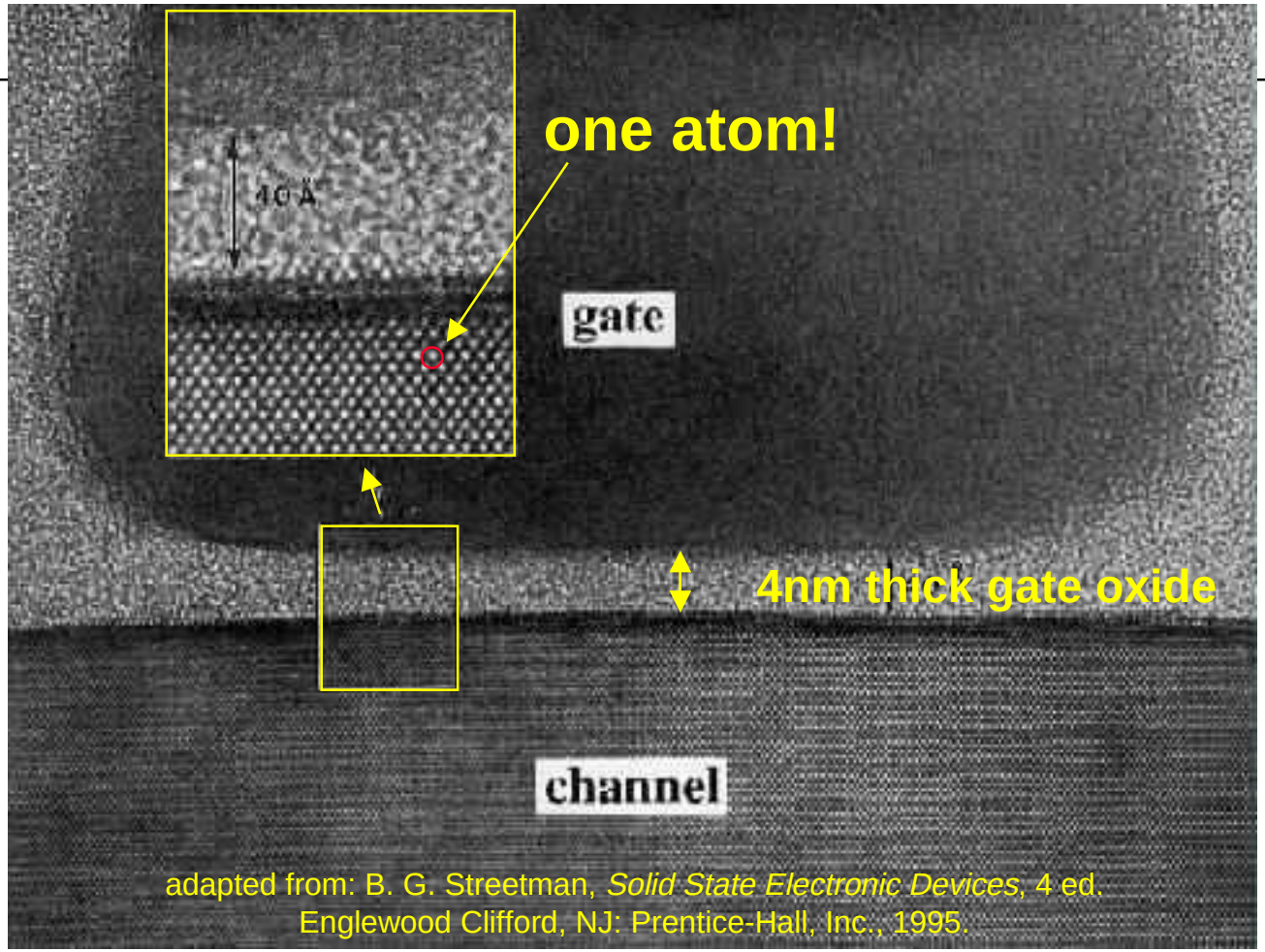


Performance characteristics and the SIA Roadmap (1997)

- **device dimensions**

Year of first product shipment	1997	1999	2001	2003	2006	2009	2012
Technology linewidth (dense lines, DRAM half pitch)	250 nm	180 nm	150 nm	130 nm	100 nm	70 nm	50 nm
isolated lines	200 nm	140 nm	120 nm	100 nm	70 nm	50 nm	35 nm
FET dimensions							
Tox (equiv. SiO_2 thickness)	4 nm	3 nm	2 nm	2 nm	1.5 nm	< 1.5 nm	< 1.0 nm
Lgate							
xj	50 nm	36 nm	30 nm	26 nm	20 nm	15 nm	10 nm
Max number of wiring levels	6	~7	7	7	~8	8-9	9

MOSFET cross section



adapted from: B. G. Streetman, *Solid State Electronic Devices*, 4 ed. Englewood Clifford, NJ: Prentice-Hall, Inc., 1995.

- **modern integrated circuits contain millions of individual MOSFETS, each about 1/100 of a hair in size!**