Bulk crystal growth

• melting points

- silicon: 1420° C
- GaAs: 1238° C
- quartz: 1732° C
- starting material: metallurgical-grade silicon
 - by mixing with carbon, SiO₂ reduced in arc furnace
 - T > 1780°C: SiC + SiO₂ \rightarrow Si + SiO + CO
 - common impurities
 - AI: 1600 ppm (1 ppm = 5 x 10¹⁶ cm⁻³)
 - B: 40 ppm
 - Fe: 2000 ppm
 - P: 30 ppm
 - used mostly as an additive in steel

Preparation of electronic-grade silicon

- gas phase purification used to produce high purity silicon
 - − ~ 600°C

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- − crud + Si + HCl \rightarrow
 - SiCl₄ (silicon tetrachloride)
 - SiCl₃H (trichlorosilane)
 - SiCl₂H₂ (dichlorosilane)
 - chlorides of impurities
- trichlorosilane (liquid at rm temp), further purification via fractional distillation
- now reverse reaction
 - 2SiHCl₃ + 2H₂ (heat) → 2Si + 6HCl
 - after purification get
 - Al: below detection
 - B: < 1 ppb (1 ppb = 5 x 10¹³ cm⁻³)
 - Fe: 4 ppm
 - P: < 2 ppb
 - Sb: 1 ppb
 - Au: 0.1 ppb

Czochralski crystal growth

- silicon expands upon freezing (just like water)
 - if solidify in a container will induce large stress
- CZ growth is "container-less"



images from Mitsubishi Materials Silicon http://www.egg.or.jp/MSIL/english/ msilhist0-e.html



Dept. of ECE, Univ. of Texas at Austin





- critical factor is heat flow from liquid to solid
 - interface between liquid and solid is an isotherm
 - temperature fluctuations cause problems!
 - already grown crystal is the heat sink
 - balance latent heat of fusion, solidification rate, pull rate, diameter, temperature gradient, heat flow
 - diameter inversely proportional to pull rate (typically ~ mm/min)





latent heat of fusion - heat flux (power) released is $L \cdot \frac{dm}{dt} = L \cdot \frac{\rho A dx}{dt} = (L \rho A) v_{pull}$

and pull at , and p / an

critical factor is heat flow from liquid to solid

heat flux (power) balance

heat released as solidifies thermal diffusion in liquid
from hot liquid towards solidification interface thermal diffusion in solid

= from solidification interface towards cooler sides/end of boule

$$(L \rho A) \cdot v_{pull} + \kappa_{liquid} \cdot A \cdot \frac{dT}{dx_1} = \kappa_{solid} \cdot A \cdot \frac{dT}{dx_2}$$

- interface between liquid and solid should be an isotherm
 - temperature fluctuations cause problems!

$$\frac{dT}{dx_1} = 0$$



heat flow balance becomes



- so critical factor is relation between temperature gradient in boule and boule size
 - thermal current proportional to cross sectional area A and v_{pull}
 - if the only heat sink were at the end of the boule:
 - thermal resistance inversely proportional to A, directly proportional to length of boule l
 - temperature change ("voltage") = I_{thermal} R_{thermal}

$$\Delta T = \left[(L \rho A) \cdot v_{pull} \right] \cdot \left[\frac{l}{\kappa_{solid} \cdot A} \right] = l \cdot \frac{L \rho}{\kappa_{solid}} \cdot v_{pull} \quad \Rightarrow \quad \frac{dT}{dx} \approx \frac{\Delta T}{l} = \frac{L \rho}{\kappa_{solid}} \cdot v_{pull}$$

- net effect: just what we got above!
- dT/dx independent of diameter
 diameter doesn't appear!!!



- but most of the heat is lost via radiation from the SIDES of the boule!
 - thermal current still proportional to cross sectional area A \propto (diameter)^2 and v_{\text{pull}}
 - if the heat sink is from sides of boule:
 - thermal resistance inversely proportional to perimeter ∞ diameter,
 - temperature change ("voltage") = I_{thermal} R_{thermal}

$$\Delta T = \left[constant \cdot (diam)^2 \cdot v_{pull}\right] \cdot \left[\frac{constant}{diam}\right] \propto diam \cdot v_{pull} \quad \Rightarrow \quad diam \propto (v_{pull})^{-1} \cdot \Delta T$$

net effect: diameter is inversely proportional to pull rate

Impurities in Czochralski Grown Silicon

- choice of crucible material is crucial:
 - must be stable at high temperatures (~1500° C)
 - carbon: saturates solution and causes poly growth
 - refractories: too much metal in materials
 - quartz: in exclusive use for silicon growth
- dissolution of quartz crucibles into melt is major concern:
 - function of relative velocity between melt & crucible
 - almost all oxygen present in silicon melt is due to the dissolution of the SiO₂ crucible
 - most of this oxygen evaporates in the form of SiO



Doping and segregation effects during crystal growth

- when two dissimilar materials / phases are in contact, the concentration of an impurity across the interface is NOT NECESSARILY CONTINUOUS
 - segregation (distribution) coefficient

$k = \frac{C_s}{C_L}$	element	AI	As	В	0	Р	Sb
	C _{solid} /C _{liquid}	0.002	0.3	0.8	1.25	0.35	0.023

- when a volume of liquid freezes, if k < 1, what is concentration in solid?
 - must be less than in liquid
 - what happens to extra impurities?
 - rejected into melt → increased [impurity] in melt
- if C_o is initial melt concentration, and X is fraction solidified

$$\mathbf{C}_{\mathbf{S}} = \mathbf{k} \cdot \mathbf{C}_{\mathbf{o}} \cdot \left(1 - \mathbf{X}\right)^{\mathbf{k} - 1}$$

k = 0.5, Cliquid = 1e17





Doping and segregation effects during crystal growth

- segregation effects can be used intentionally to purify semiconductor material
 - zone refining consists of repeated passes through the solid by a liquid zone

$$C_{n+1}(x) = C_n(x) \cdot \left[1 - (1-k) \cdot e^{-k \cdot x/L}\right]$$

float zone silicon used for high resistivity





images from Mitsubishi Materials Silicon http://www.egg.or.jp/MSIL/english/msilhist0-e.html





Oxygen in CZ Silicon

- concentrations typically in 10¹⁶ 10¹⁸ cm⁻³ range
 - segregation coefficient k ~ 1.25
 - more in solid than liquid
 - contact area between crucible and melt decreases as growth procedes
 - oxygen content decreases from seed to tang end
- effects of oxygen in silicon
 - ~ 95% interstitial; increases yield strength of silicon via "solution hardening" effect
 - as-grown crystal is usually supersaturated (occurs above about 6 x 10¹⁷)

Oxygen complexes in silicon

- usually donor-like
- two classes of complexes:
 - "old thermal donors"
 - very small silicon-oxygen atom clusters
 - very rapid formation rates in 400-500° C range (≥ 10¹⁰/cm³sec)
 - "new thermal donors"
 - slow formation rate above 500° C
 - slow dissolution rate at high temperature
 - ~10¹³ cm⁻³ @ 2 hours, 900° C
 - ~10¹¹ cm⁻³ @ 2 hours, 1150° C
 - donor behavior possibly due to surface states of large SiO_x complexes

D D C

Gettering in Silicon Wafers

- devices fabricated only in the top five or ten microns of the wafer: use gettering to provide a sink for unwanted defects in the bulk of the wafer
 - gettering sites provide sinks for impurities generated during the processing





- backside damage: (pre-gettering)
 - mechanical damage produces high strain regions
 - impurities nucleate on dislocations; if wafer stresses are kept small during subsequent processing dislocations will remain localized on back

Intrinsic Gettering and Oxygen Precipitates

- wafer starting material:
 - initial oxygen content between ~3.5 and ~8 x 10^{17} cm⁻³
- denuded zone formation:
 - high temperature step (1050° C) reduces interstitial oxygen content via diffusion of O to surface
 - formation of internal gettering sites:
 - low temp step (500-600° C) creates large reserve of small, stable oxygen precipitates
 - higher temperature step (700-900° C) causes growth of larger SiO_x complexes
 - subsequent thermal processing creates dislocation loops associated with SiO_x complexes
 - actual starting material oxygen concentration and process determined by trial device fab and performance evaluation.



Denuded zone

- preferential (decorating) etch used to reveal stacking faults and precipitates
 - OSF: oxidation induced stacking faults



from: Sze, VLSI Technology, 2nd edition, p. 46.

Wafer preparation

- boule forming, orientation measurement
 - old standard: "flat" perpendicular to <110> direction;
 - on large diameter "notch" used instead



- wafer slicing
 - <100> typically within ± 0.5°
 - <111>, 2° 5° off axis

images from Mitsubishi Materials Silicon http://www.egg.or.jp/MSIL/english/msilhist0-e.html



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Wafer prep (cont.)

• lapping

- grind both sides, flatness ~2-3 μm
 - ~20 μ m per side removed
- edge profiling
- etching
 - chemical etch to remove surface damaged layer
 - ~20 μ m per side removed
- polishing
 - chemi-mechanical polish, SiO₂ / NaOH slurry
 - ~25 μ m per polished side removed
 - gives wafers a "mirror" finish
- cleaning and inspection



Wafer specifications

wafer diam.	thickness	thickness variation	bow	warp
150 mm	675µm			
±	±	50µm	60µm	
0.5mm	25µm			
200 mm				
±				
300 mm	775µm			
±	±	= 10µm		= 100µm
0.2mm	25µm			

- warp: distance between highest and lowest points relative to reference plane
- bow: concave or convex deformation

Wafer diameter trends

 desire is to keep number of chips (die) per wafer high, even as die size increases



 challenge: thermal nonuniformities, convection currents become more significant as diameter grows



Wafer specifications





From Sematech document: International 300 mm Initiative, Technology Transfer # 97113407A-ENG

- "next" generation: 300 mm wafer diameter
- 25x25 mm die size
 - yields 89 complete die

Silicon wafer production

- 1999: 4.263 billion square inches, \$5.883 billion
 - \$1.38 per square inch, \$0.21 per square cm
 - 100mm, 150mm: 2.808 billion square inches (65.9% of total)
 - 200mm: 1.441 billion square inches (33.8%)
 - 300mm: 0.014 billion square inches of silicon (0.3%)
- 2000, expected: 4.692 billion square inches, \$6.475 billion
- 2001, expected: 5.204 billion square inches
- 2003, expected:
 - 200mm: 2.892 billion square inches
 - 300mm: 0.112 billion square inches
- from EE Times, "Advanced silicon substrates prices rise as wafer glut eases" by J.Robert Lineback <u>Semiconductor</u> <u>Business News</u> (01/12/00, 2:04 p.m. EST)

Volume Silicon processing costs

• 2001 processing cost date

- reference: ICKnowledge, <u>http://www.icknowledge.com/economics/wafer_costs.html</u>
- advanced CMOS process, ~0.13 micron, 300mm wafers, ~25 mask levels:
 - about \$5 per cm²
 - reference: ICKnowledge, <u>http://www.icknowledge.com</u>
 - model assumes a 30,000 300mm wafer per month fab running at 90% of capacity
 - that's about 21 million cm² / month!
 - about 40 wafer starts per hour
 - 2001 world-wide wafer starts, 8" (200mm) equivalent: ~5 million wafers per month (~1.5billion sq. cm per month)
 - from <u>http://www.semichips.org/downloads/SICAS_Q4_01.pdf</u>
- MOSIS (ref <u>http://www.mosis.org/Orders/Prices/price-list-domestic.htm</u>
 - 1.5 micron cmos ~\$200 per square mm, 5 to 20 parts per lot ⇒ cost ~\$4K- \$1K per cm²
 - 0.18 micron ~\$1-2K per square mm for 40 parts ⇒ cost > ~\$2.5K per cm²

Silicon Oxides: SiO₂

- Uses:
 - diffusion masks
 - surface passivation
 - gate insulator (MOSFET)
 - isolation, insulation
- Formation:
 - grown / "native"
 - thermal: "highest" quality
 - anodization
 - deposited:
 - C V D, evaporate, sputter
- vitreous silica: material is a GLASS under "normal" circumstances
 - can also find "crystal quartz" in nature
- m.p. 1732° C; glass is "unstable" below 1710° C
 - BUT devitrification rate (i.e. crystallization) below 1000° C negligible



- **bridging oxygen**
- \otimes non-bridging oxygen
- silicon
 - network modifier
 - network former
- hydroxyl group