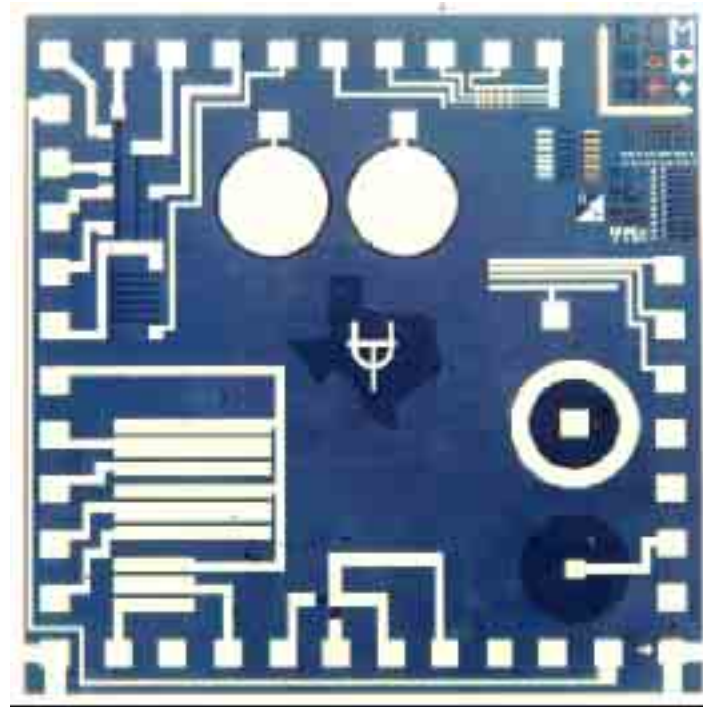


Integrated Circuit Fabrication



Professor Dean Neikirk

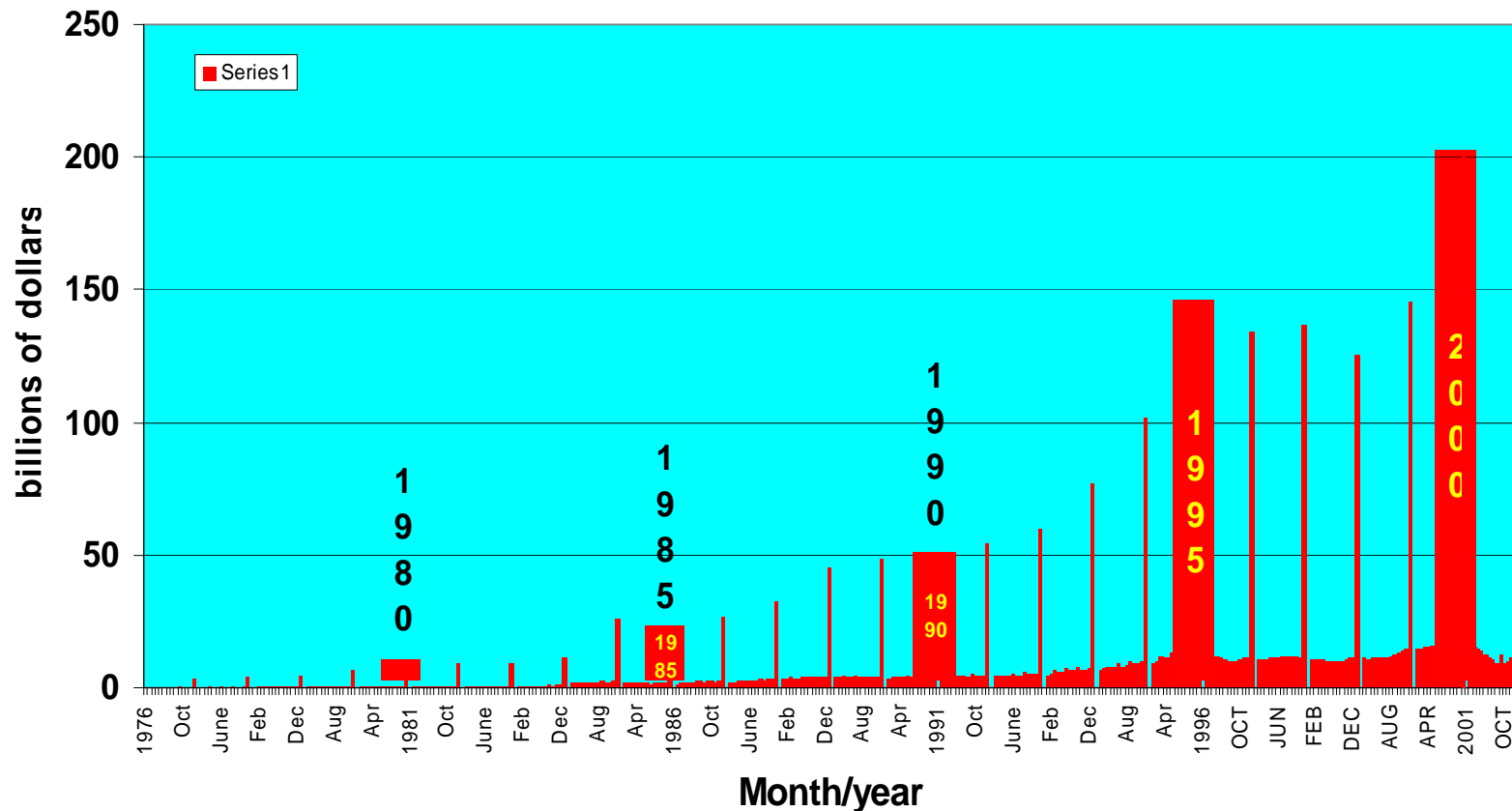
Department of Electrical and Computer Engineering

The University of Texas at Austin

world wide web: <http://weewave.mer.utexas.edu>

Integrated circuits in modern society

World Wide Sales



- **World-wide sales (all semiconductors): over \$150 billion dollars**
- **about 87% ICs, 13% discretetes**

Selected moments in solid-state electronics

- Early semiconductors discovered in 1800's: (PbS, ZnSb, AgS)
- 1874: Ferdinand Braun reported rectification in point contact diodes on PbS. Braun won the 1909 Nobel prize for his work on radio, along with Marconi
- 1906: Silicon used for the first time
- 1911: term "semiconductor" introduced
- 1930's: largely valid theoretical description of rectifying junctions complete
- Dec. 1947: Brattain, Bardeen, & Shockley demonstrated point contact transistor. 1956 Nobel for this work
- Jan . 1948: Shockley has worked out operation (theoretical) of bipolar junction transistor



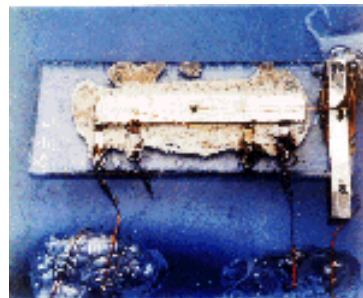
<http://www.tcm.org/html/history/detail/1947-point.html>

Selected moments in solid-state electronics

- 1951: manufacturable technique demonstrated using “grown junctions”
- 1954: photoresist technology applied to transistor fab
- 1954-58: TI monopoly on silicon transistors
- Sept. 1958: Jack Kilby (TI) patents “Solid Circuit,” monolithic Ge Phase-shift oscillator & flip-flop



<http://www.ti.com/corp/docs/kilbyctr/jackbuilt.htm>



<http://www.ti.com/corp/docs/history/firsticnf.htm>



<http://www.tcm.org/html/history/detail/1958-intcirc.html>

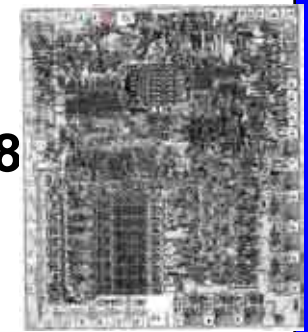
Selected moments in solid-state electronics

- 1959: truly planar IC process by Noyce (Fairchild)

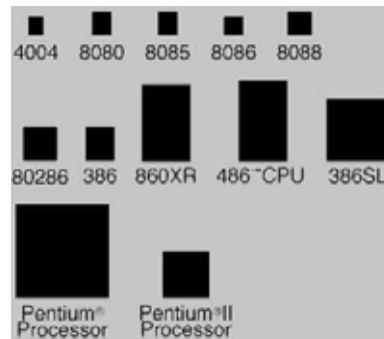
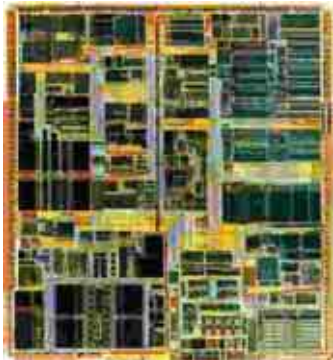


- Early 1960's: Motorola joins "Big Three" (TI, Fairchild, Motorola)
- 1960's: Bipolar versus MOSFET debate rages
- 1966: TI's first MOS IC (binary-to decimal decoder)
- 1968ish: Intel founded by ex-Fairchild employees (Noyce & Moore)

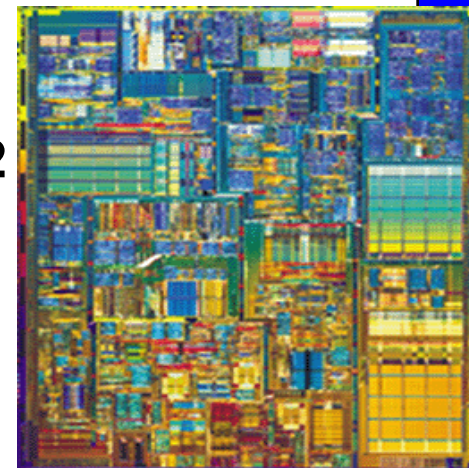
Selected moments in solid-state electronics



- 1971: first “microprocessor”: Intel 4004, 2300 transistors, 108kHz, 13.5 mm²
- 1974: first “PC” (the Altair), Intel 8080 microprocessor, 2MHz, 20mm²
 - 1978: IBM PC, Intel 8086/8088
- 1997: Intel Pentium® II, 7.5 million transistors, 200-300MHz, 209mm²



- 2000: Pentium 4, 42 million transistors, 0.18 microns, 1.5 GHz, 224mm²



http://www.intel.com/intel/intelis/museum/exhibit/hist_micro/hof/hof_main.htm,
also data from: <http://www.icknowledge.com/trends/uproc.html>

other history

- 1967: 2" wafers
- mid-80's: 4" wafers
 - <http://www.national.com/company/pressroom/gallery/historical.html>



ITRS: International Technology Roadmap for Semiconductors

- <http://public.itrs.net/>
 - assessment of the semiconductor technology requirements
 - objectives is to ensure advancements in performance of ics
 - cooperative effort of global industry manufacturers and suppliers, government organizations, consortia, and universities
 - identifies technological challenges and needs over the next 15 years
 - sponsored by the Semiconductor Industry Association (SIA), the European Electronic Component Association (EECA), the Japan Electronics & Information Technology Industries Association (JEITA), the Korean Semiconductor Industry Association (KSIA), and Taiwan Semiconductor Industry Association (TSIA)

ITRS roadmap (2000) fabrication requirements

- dimensional requirements

| “technology node” (nm) | year | min gate length (nm) | equivalent gate oxide thickness (nm) |
|-------------------------------|-------------|-----------------------------|---|
| 130 | 2002 | 85-90 | 1.5-1.9 |
| 90 | 2005 | 65 | 1.0-1.5 |
| 60 | 2008 | 45 | 0.8-1.2 |
| 40 | 2011 | 32 | 0.6-0.8 |

Performance characteristics and the SIA Roadmap (1997)

- transistor count

| Year of first product shipment | 1997 | 1999 | 2001 | 2003 | 2006 | 2009 | 2012 |
|--|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| Memory | | | | | | | |
| bits @ samples/intro | 256M | 1G | * | 4G | 16G | 64G | 256G |
| bits @ production | 64M | 256M | 1G | 1G | 4G | 16G | 64G |
| Bits/cm ² @ sample/intro | 96M | 270M | 380M | 770M | 2.2B | 6.1B | 17B |
| DRAM chip size, mm ² | 100 mm ² | 140 mm ² | 160 mm ² | 200 mm ² | 280 mm ² | 390 mm ² | 550 mm ² |
| Logic (high volume, cost sensitive) | | | | | | | |
| Logic transistors/cm ² (packed, including on-chip SRAM) | 3.7M | 6.2M | 10M | 18M | 39M | 84M | 180M |
| Microprocessor transistors/chip | 11M | 21M | 40M | 76M | 200M | 520M | 1.4B |
| MPU chip size, mm ² | 110 mm ² | 125 mm ² | 140 mm ² | 150 mm ² | 180 mm ² | 220 mm ² | 260 mm ² |
| Logic (low volume; ASICs) | | | | | | | |
| Usable transistors/cm ² | 8M | 14M | 16M | 24M | 40M | 64M | 100M |

Performance characteristics and the SIA Roadmap (1997)

- performance

| Year of first product shipment | 1997 | 1999 | 2001 | 2003 | 2006 | 2009 | 2012 |
|--------------------------------|---------|----------|---------|---------|---------|---------|--------|
| Chip frequency | | | | | | | |
| on chip, local, high perf. | 750 MHz | 1.25 GHz | 1.5 GHz | 2.1 GHz | 3.5 GHz | 6 GHz | 10 GHz |
| on chip, global, high perf. | 750 MHz | 1.2 GHz | 1.4 GHz | 1.6 GHz | 2 GHz | 2.5 GHz | 3 GHz |
| on chip, cost sensitive | 400 MHz | 600 | 700 | 800 | 1.1 GHz | 1.4 | 1.8 |
| chip to board, high perf. | 750 MHz | 1.2 GHz | 1.4 GHz | 1.6 | 2 | 2.5 | 3 |
| Max number of wiring levels | 6 | ~7 | 7 | 7 | ~8 | 8-9 | 9 |

Performance characteristics and the SIA Roadmap (1997)

- device dimensions

| | | | | | | | |
|---|--------|--------|--------|--------|--------|----------|----------|
| Year of first product shipment | 1997 | 1999 | 2001 | 2003 | 2006 | 2009 | 2012 |
| Technology linewidth (dense lines, DRAM half pitch) | 250 nm | 180 nm | 150 nm | 130 nm | 100 nm | 70 nm | 50 nm |
| isolated lines | 200 nm | 140 nm | 120 nm | 100 nm | 70 nm | 50 nm | 35 nm |
| FET dimensions | | | | | | | |
| Tox (equiv. SiO ₂ thickness) | 4 nm | 3 nm | 2 nm | 2 nm | 1.5 nm | < 1.5 nm | < 1.0 nm |
| Lgate | | | | | | | |
| xj | 50 nm | 36 nm | 30 nm | 26 nm | 20 nm | 15 nm | 10 nm |
| Max number of wiring levels | 6 | ~7 | 7 | 7 | ~8 | 8-9 | 9 |

Performance characteristics and the SIA Roadmap (1997)

- wafer, package dimensions

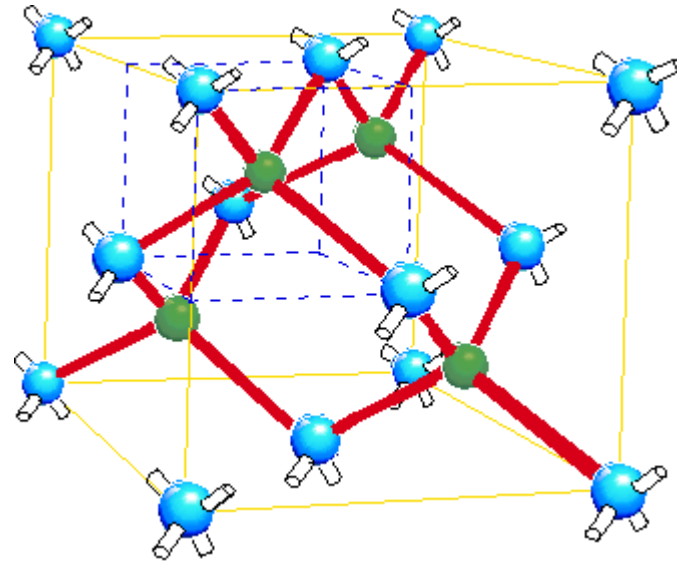
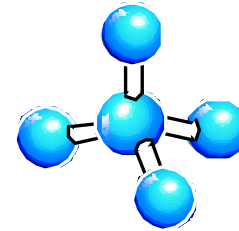
| | | | | | | | |
|---|------------------------------|------------------------------|------------------------------|------------------------------|-------------------------------|-------------------------------|-------------------------------|
| Year of first product shipment | 1997 | 1999 | 2001 | 2003 | 2006 | 2009 | 2012 |
| Lithography field size (mm x mm; mm ²) | 22x22 484 mm ² | 25x32 800 mm ² | 25x34 850 mm ² | 25x36 900 mm ² | 25x40 1000 mm ² | 25x44 1100 mm ² | 25x52 1300 mm ² |
| Wafer diameter (mm) | 200 mm (8") | 300 mm (12") | 300 mm | 300 mm | 300 mm | 450 mm (18") | 450 mm |
| Number of chip I/O's | | | | | | | |
| chip-to-package high performance | 1490 | 2000 | 2400 | 3000 | 4000 | 5400 | 7300 |
| "low cost" | 800 | 975 | 1195 | 1460 | 1970 | 2655 | 3585 |
| Number of package I/Os | | | | | | | |
| ASIC (high perf.) | 1100 | 1500 | 1800 | 2200 | 3000 | 4100 | 5500 |
| MPU, cost sensitive | 600 | 810 | 900 | 1100 | 1500 | 2000 | 2700 |

Silicon Semiconductor Integrated Circuits

- Silicon makes up over 26% of the earth's crust, mainly in the form of silicon dioxide, SiO_2 , more commonly known as **sand** or quartz
- For semiconductor use, the silicon must be purified so that there are no more than about ten impurity atoms to every billion silicon atoms
- Large diameter (> 8 inch), single crystal silicon boules weighing more than 100 lbs are routinely grown from a melt at over 2500°F

What does silicon look like?

- fundamentally, it looks like diamond!
 - each atom bonds to four neighbors in a **tetragonal** configuration
 - the atoms are arranged into a **face-centered cubic** crystal structure



Silicon “wafers”

- To build integrated circuits we use large, very flat ‘wafers’
- Silicon substrate usage
 - ‘84: 2.5 G in² (about 0.6 sq. miles!)
 - ‘86: 1.35 G in²
 - ‘87: 1.99 G in²
 - ‘93: 2 G in²
 - ‘94: 3 G in²
 - ‘95: 3 G in²
 - ‘99: 4.263 G in² @ \$5.883 billion
- Costs
 - raw substrate: about \$1.38 per sq. inch (1999)
 - processed: \$30-\$40 per sq. inch

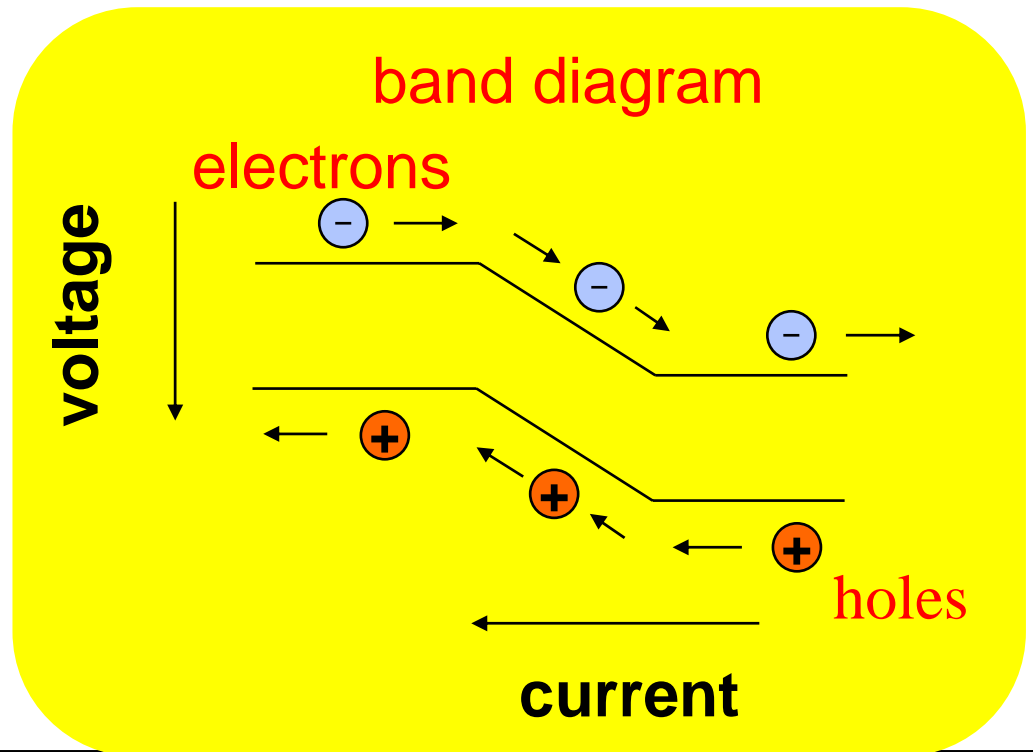
Basic Electrical Terminology

- **Voltage (V)**
 - the externally applied force which drives the flow of charged carriers
- **Current (I)**
 - the number of carriers per second flowing in the electrical circuit
 - $I = \text{constant} \times \text{speed} \times \text{number}$
- **Resistance (R)**
 - a measure of how much force is needed to produce a certain current
 - Ohm's Law: $I \times R = V$

Electrical Conduction in Semiconductors

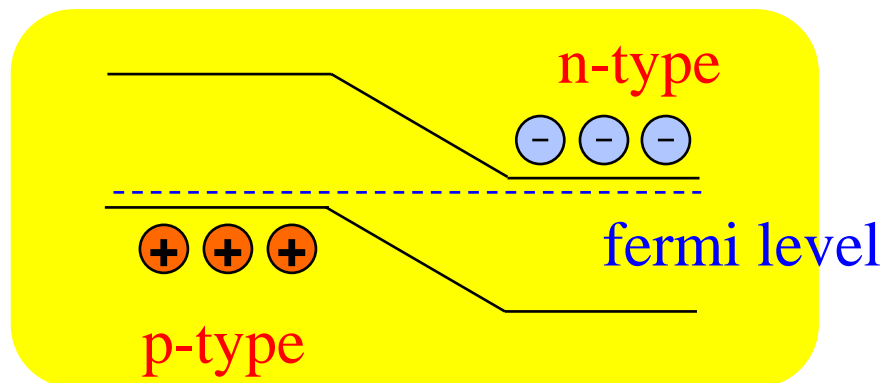
- **Semiconductors**
 - depending on what kind of impurities are incorporated, the charge carriers in semiconductors may be either electrons (called n-type material) or holes (called p-type material); compared to metals (which have only electrons), semiconductors have fairly high resistance

- **Electrons:**
 - negative charge, flow “downhill”
- **Holes:**
 - positive charge, flow “uphill”

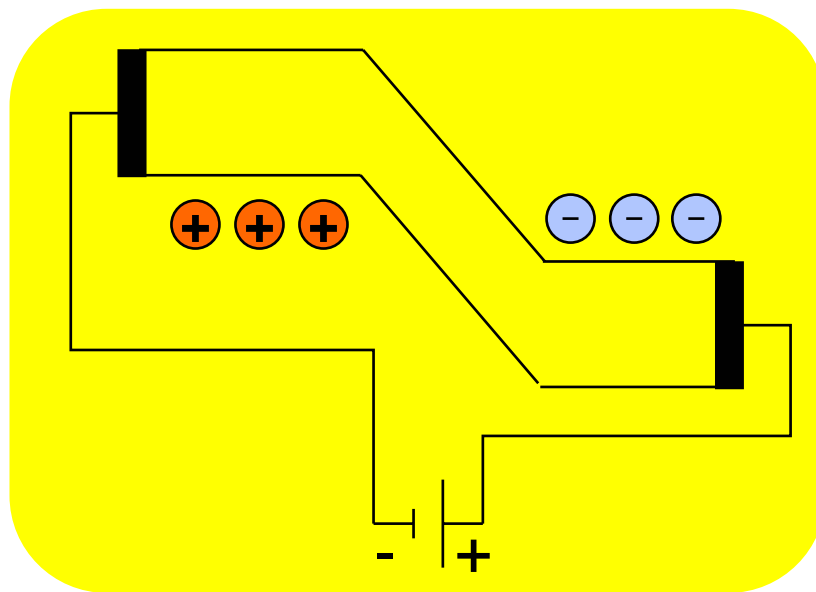


What happens when two different types of silicon touch?

- This is called an “p-n junction”

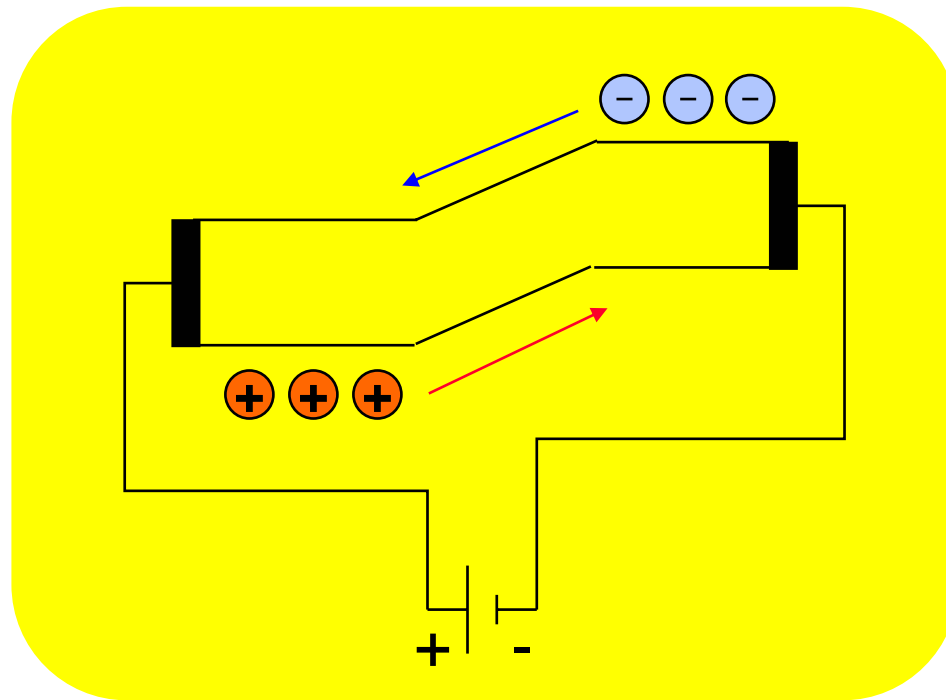


If a positive voltage is applied to the n-type side of the junction the barrier is even higher than it was with no voltage



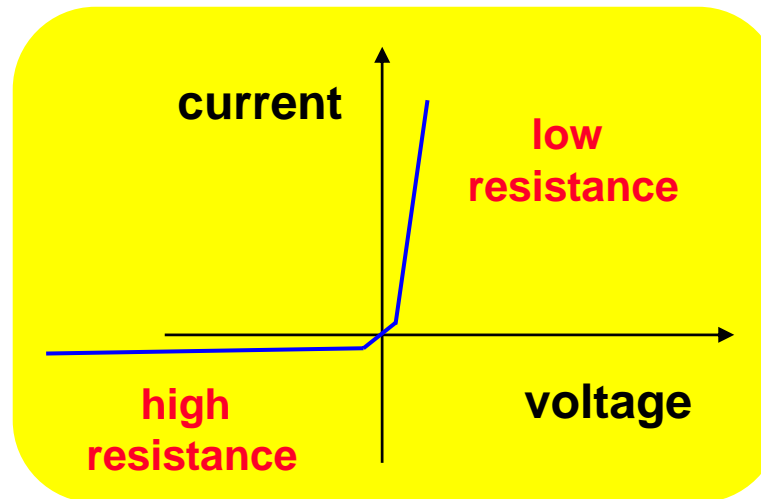
p-n Junctions in Semiconductors

- But if a positive voltage is applied to the p-type side both the electrons and holes can flow:



p-n Junctions in Semiconductors

- Because of the way the barrier changes in a p-n junction, it changes from a low resistance device to a high resistance one, depending on the applied voltage:

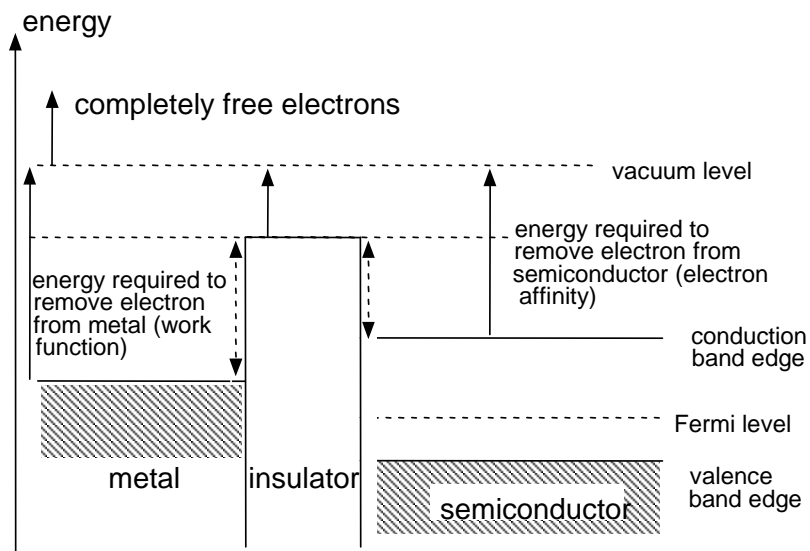


This “asymmetry” in electrical characteristic is required in many integrated circuit devices.

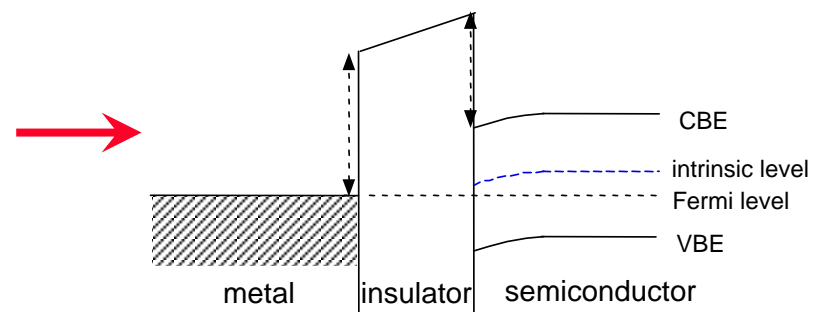
Band diagrams for a metal - insulator - semiconductor (MIS) system

- what happens when you join these three materials?
 - the “field effect” was actually discovered in the early 1900’s (before p-n junctions were known)

in isolation:



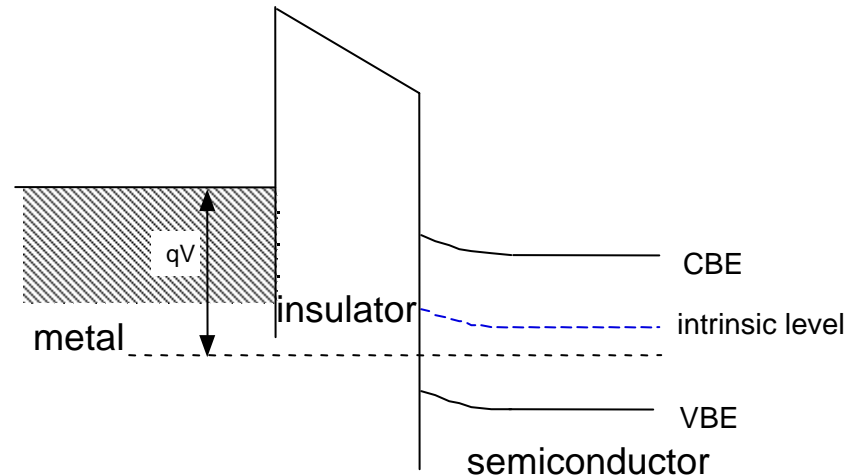
when in contact:



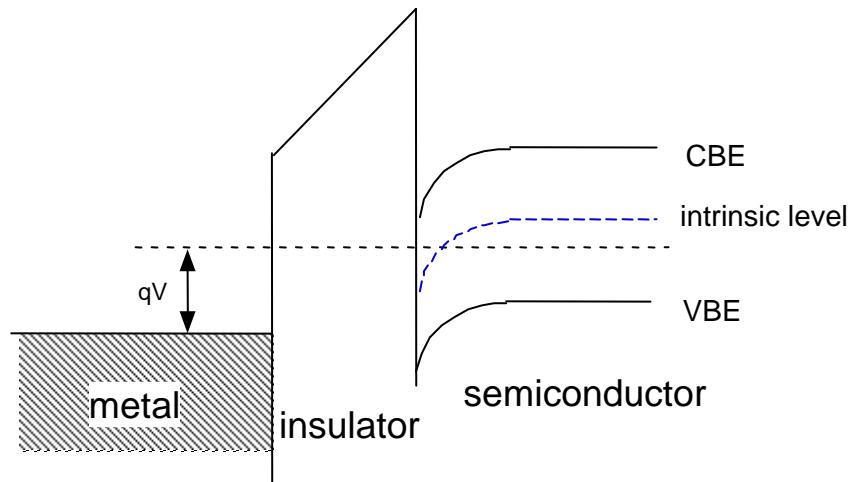
pict

Accumulation and inversion in an MIS system: p-type substrate

- metal biased at voltage $-V$ relative to semiconductor
 - surface is in “accumulation”
 - majority carrier type at surface same as in bulk

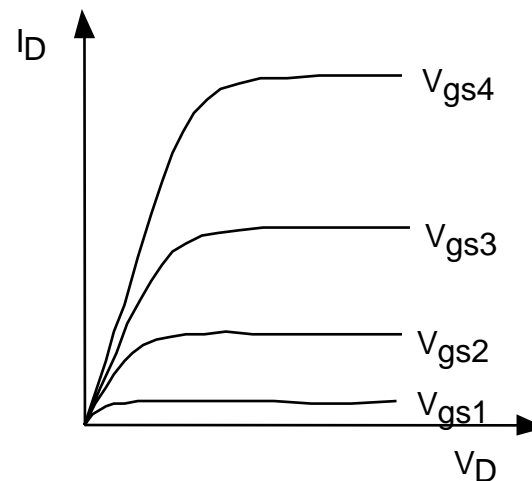
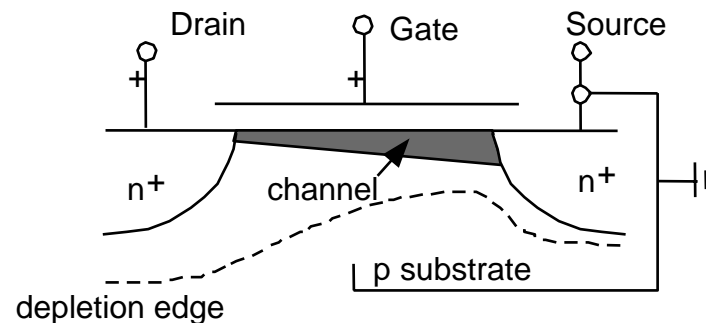


- metal biased at voltage $+V$ relative to semiconductor
 - surface is in “inverted”
 - majority carrier type at surface opposite that in bulk



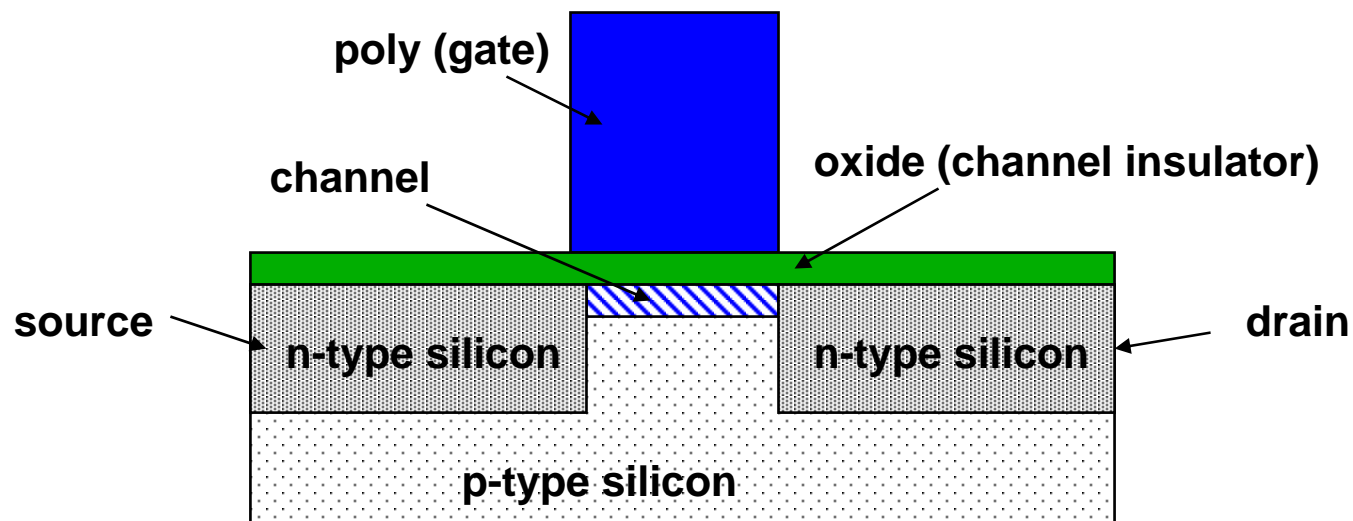
Metal-Oxide Field Effect Transistor (MOSFET)

- to make a device you need
 - insulator and gate metal in close proximity to semiconductor surface
 - **all the action is at the surface!**
 - contact that blocks bulk majority carriers, but not opposite carrier type
 - p-n junction
- four terminal device
 - usual configuration connects source and substrate together



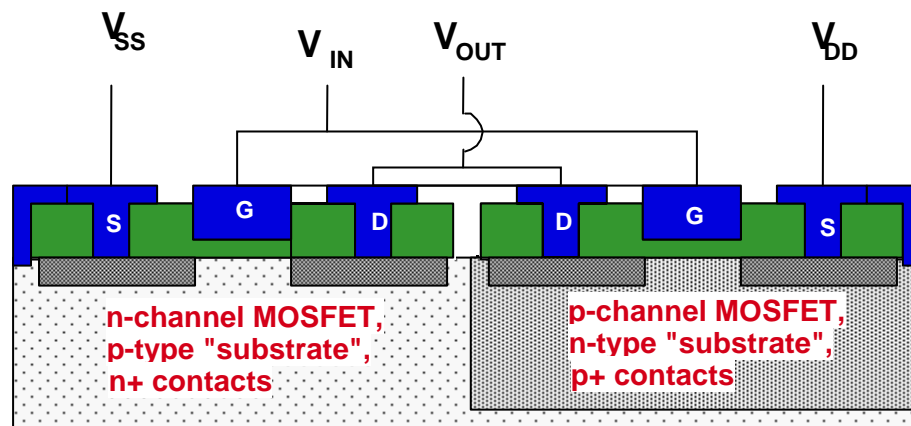
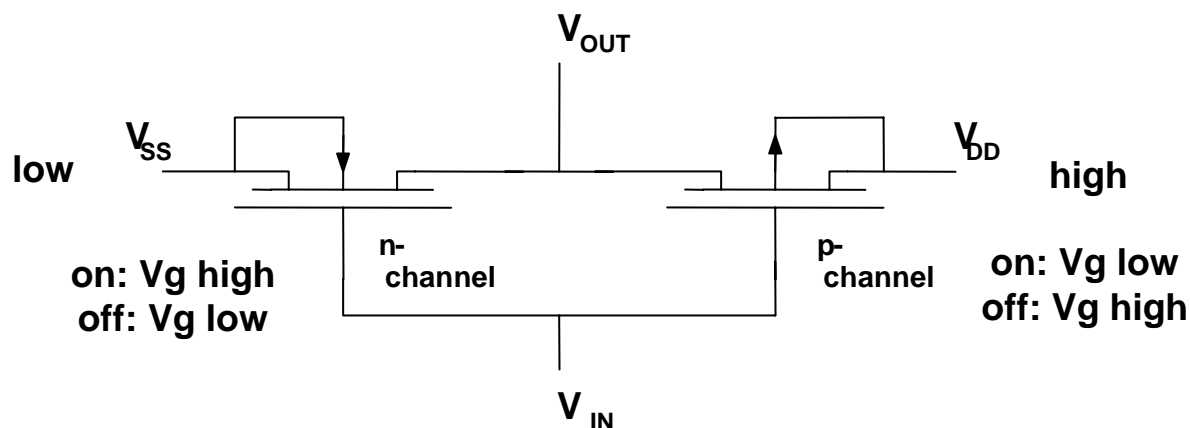
How to make a MOSFET

- What do you need?
 - a good semiconductor (SILICON)
 - a p-n junction (boron-doped Si - phosphorus-doped Si)
 - a good insulator (SILICON DIOXIDE)
 - a good conductor (poly-silicon and aluminum, copper)



CMOS inverter

- need both n- and p-channel devices on the same chip:



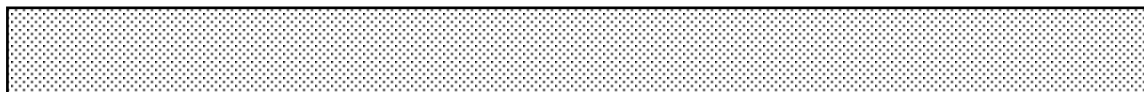
pict

Silicon Device Processing

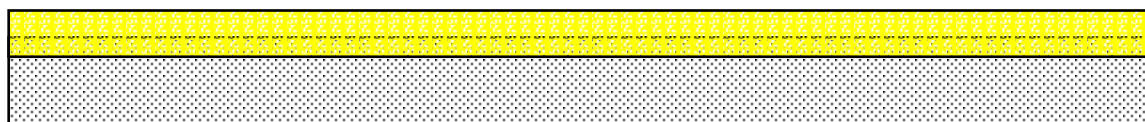
- **The construction of a silicon integrated circuit uses three basic processes:**
 - **Oxidation:**
 - by heating silicon to about 2000° F in oxygen the surface of the silicon becomes silicon dioxide (glass), a very good insulator.
 - **Photolithography:**
 - is a way of producing a pattern of bare areas and covered areas on a substrate. This serves as a mask for etching of the silicon dioxide.
 - **Diffusion:**
 - is a process for the introduction of controlled amounts of impurities into the bare areas on the silicon (as little as one impurity atom per million silicon atoms). This allows the formation of p-n diodes in the substrate.
- **When all these steps are combined, along with metal wires for connections between devices, an integrated circuit can be made.**

How to make a MOSFET

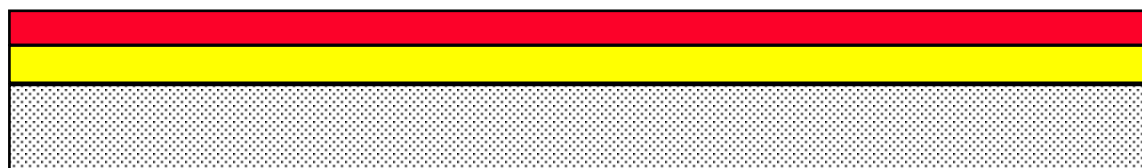
start: bare silicon wafer



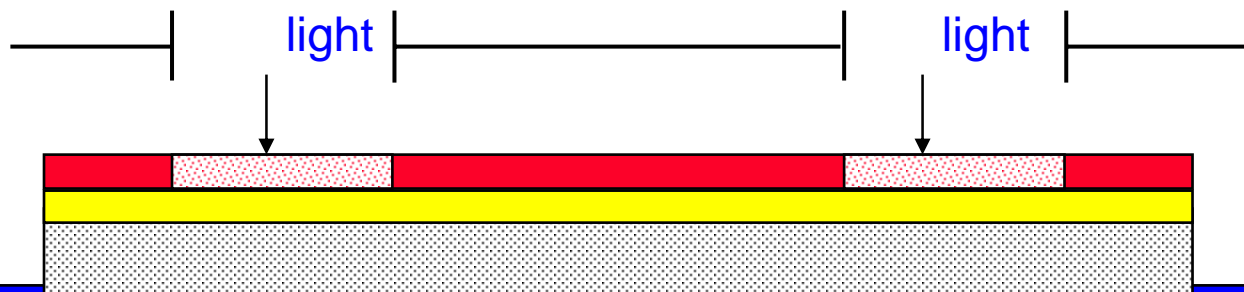
oxidize



apply *photoresist* (pr)

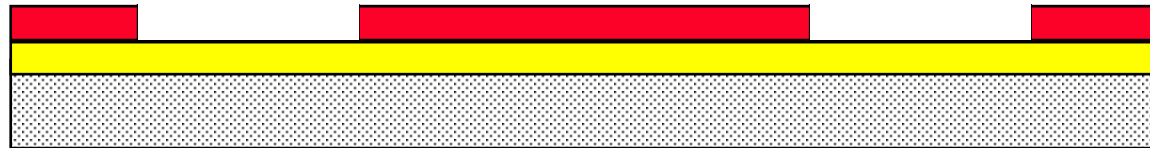


expose mask 1

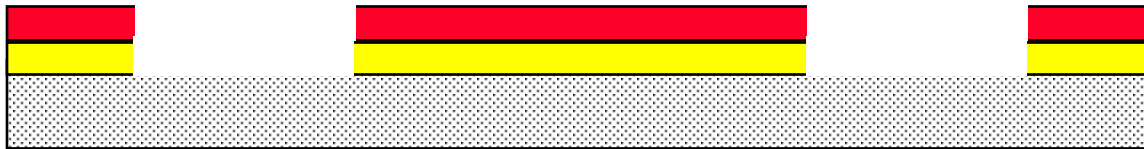


How to make a MOSFET

develop pr



etch oxide



strip pr

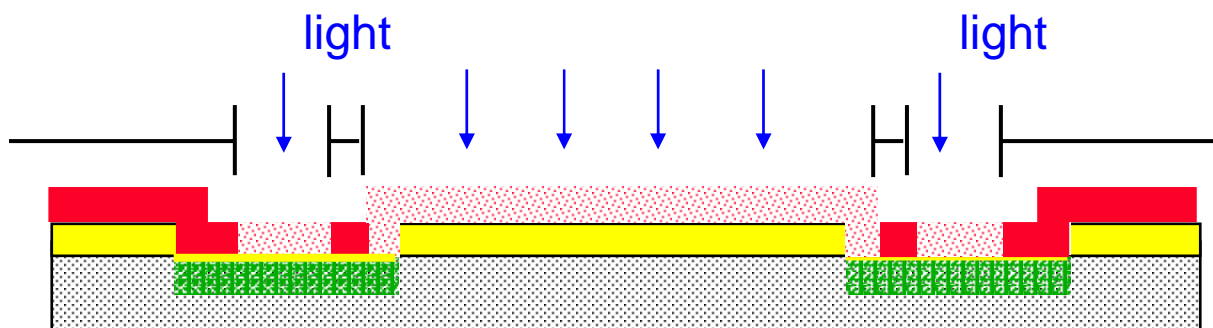


introduce source drain dopants



How to make a MOSFET

coat pr, align mask 2, expose mask 2



develop pr, etch oxide

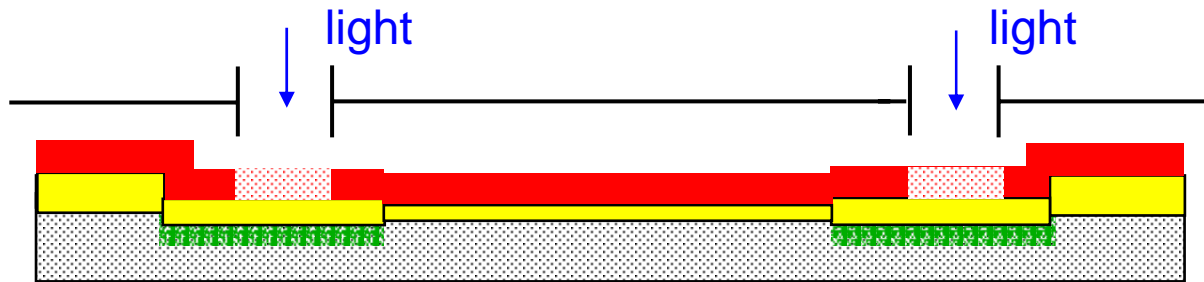


strip pr, re-oxidize to form gate insulator



How to make a MOSFET

coat pr, align mask 3, expose mask 3

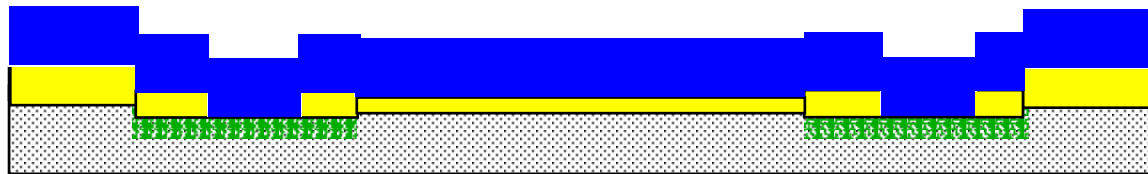


develop pr, etch oxide, strip pr

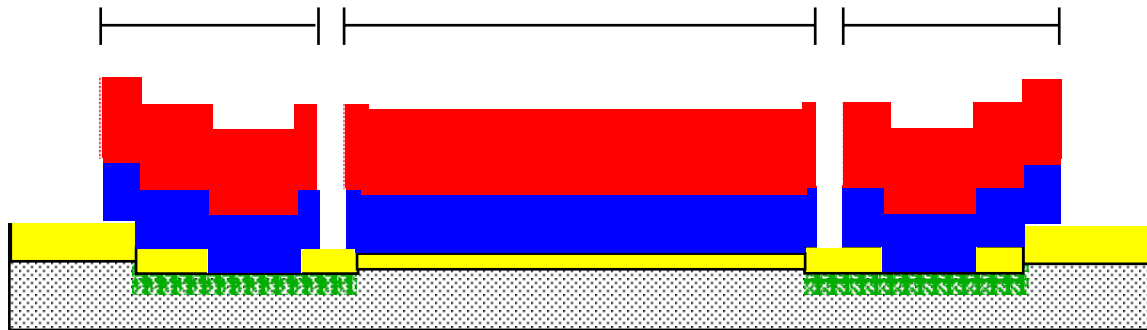


How to make a MOSFET

metallize,



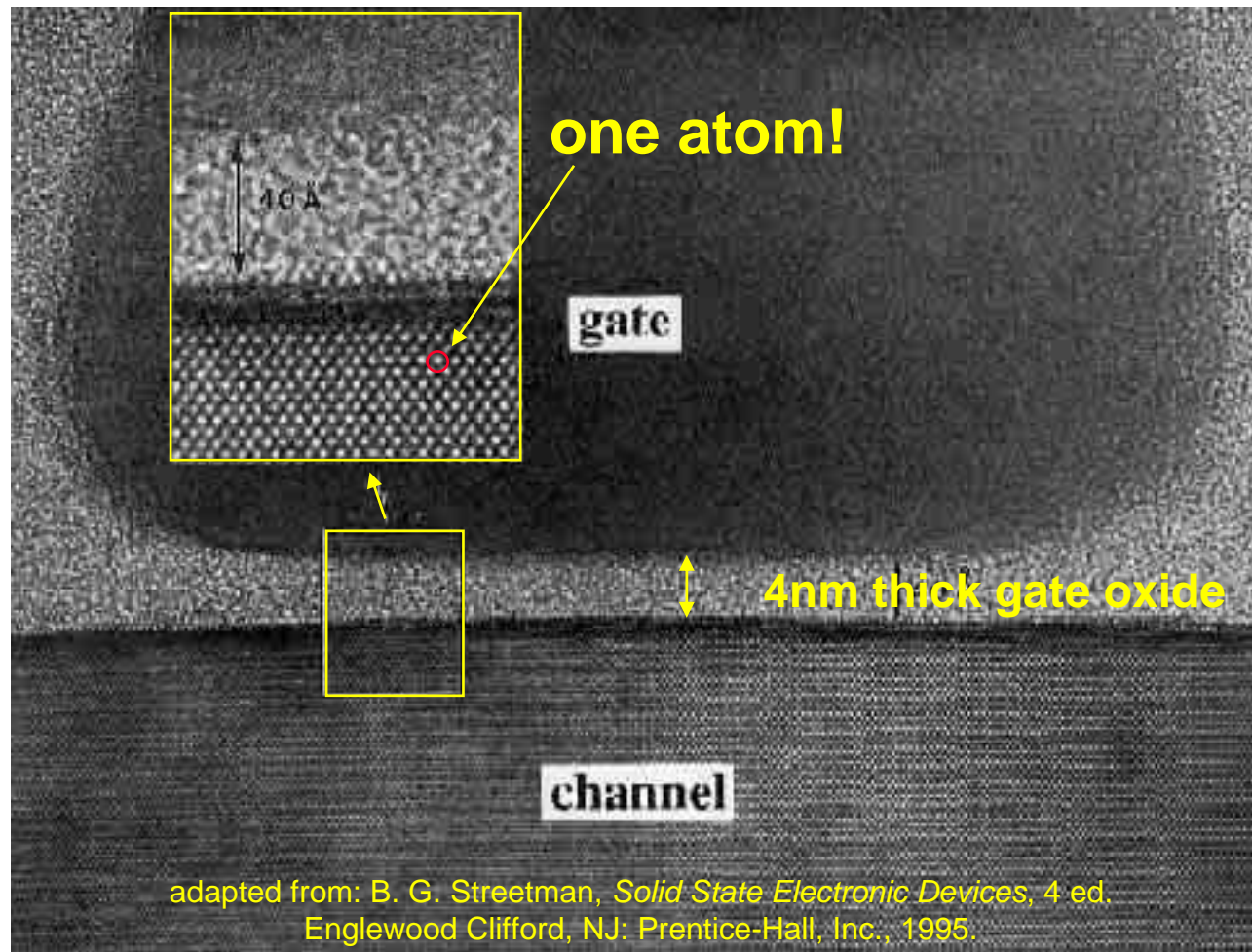
coat pr, align mask 4, expose, develop pr, etch metal



strip pr: FINISHED!



MOSFET cross section



- modern integrated circuits contain **millions** of individual MOSFETS, each about 1/100 of a hair in size!

Silicon wafer production

- 1999: 4.263 billion square inches, \$5.883 billion
 - \$1.38 per square inch, \$0.21 per square cm
 - 100mm, 150mm: 2.808 billion square inches (65.9% of total)
 - 200mm: 1.441 billion square inches (33.8%)
 - 300mm: 0.014 billion square inches of silicon (0.3%)
- 2000, expected: 4.692 billion square inches, \$6.475 billion
- 2001, expected: 5.204 billion square inches
- 2003, expected:
 - 200mm: 2.892 billion square inches
 - 300mm: 0.112 billion square inches
- from EE Times, “Advanced silicon substrates prices rise as wafer glut eases” by J.Robert Lineback [Semiconductor Business News](#) (01/12/00, 2:04 p.m. EST)

Volume Silicon processing costs

- 2001 wafer cost date
 - reference: ICKnowledge, http://www.icknowledge.com/economics/wafer_costs.html
- using the cheapest process flow costing model (5" wafers, 2 micron cmos, two levels) I could easily find:
 - about \$2 per cm²
 - almost all is overhead cost
 - 300mm wafer costs assume a 30,000 wafer per month Fab running at 90% of capacity
 - reference: ICKnowledge, <http://www.icknowledge.com>

| Wafer diam (mm) | Wafer area (cm ²) | technology | processed cost per wafer range (\$) | | processed cost per cm ² range (\$/cm ²) | |
|-----------------|-------------------------------|---------------------------|-------------------------------------|------|--|-----|
| 100 | 78.54 | 2μm, 8-12 masks | 130 | 190 | 1.7 | 2.4 |
| 125 | 122.72 | 2μm, 8-12 masks | 150 | 220 | 1.2 | 1.5 |
| 150 | 176.71 | 2μm-0.8μm, 8-18 masks | 180 | 410 | 1.0 | 2.3 |
| 200 | 314.16 | 0.8μm-0.13μm, 14-26 masks | 480 | 2500 | 1.5 | 8.0 |
| 300 | 706.85 | 0.13μm, 22-26 masks | 3200 | 3600 | 4.5 | 5.1 |

Low volume foundry prices

- **MOSIS** (ref <http://www.mosis.org/Orders/Prices/price-list-domestic.htm>)
 - 1.5 micron cmos ~\$200 per square mm, 5-20 parts ⇒ cost ~\$4K - \$1K per cm²
 - 0.18 micron ~\$1-2K per square mm, 40 parts ⇒ cost > ~\$2.5K per cm²
- **MUMPS** (foundry for simple mems processing)
 - ref: <http://www.memsrus.com/cronos/svcsmumps.html>
 - one die site is 1 cm² !
 - ⇒ cost > \$3K per cm² !

TSMC 0.18 Micron Mixed Signal/RF Process (CM018)

Non-Epitaxial Wafer; Prices are per square millimeter per design and packaging is NOT included.

From <http://www.mosis.org/Orders/Prices/price-list-domestic.htm>

Minimum charge is for a 7.0 mm² area. First lot of 40 parts of one design.

| SIZE (mm ²) | UNIT PRICE | |
|----------------------------|-----------------------------|-----------------------------|
| | <u>STANDARD</u> | <u>DISCOUNT</u> |
| 0 - 7 | \$28,000 | \$25,200 |
| 7 - 10 | \$4,000 * size | \$3,600 * size |
| 10 - 25 | \$20,000 + (\$2,000 * size) | \$18,000 + (\$1,800 * size) |
| 25 - 50 | \$27,500 + (\$1,700 * size) | \$24,750 + (\$1,530 * size) |
| 50 - 75 | \$45,000 + (\$1,350 * size) | \$40,250 + (\$1,220 * size) |
| 75 - 100 | \$56,250 + (\$1,200 * size) | \$50,750 + (\$1,080 * size) |
| 100 - 150 | \$66,250 + (\$1,100 * size) | \$58,750 + (\$1,000 * size) |

Volume Silicon processing costs

- 2001 processing cost date
 - reference: ICKnowledge, http://www.icknowledge.com/economics/wafer_costs.html
- advanced CMOS process, ~0.13 micron, 300mm wafers, ~25 mask levels:
 - about \$5 per cm²
 - reference: ICKnowledge, <http://www.icknowledge.com>
 - model assumes a 30,000 300mm wafer per month fab running at 90% of capacity
 - that's about 21 million cm² / month!
 - about 40 wafer starts per hour
 - 2001 world-wide wafer starts, 8" (200mm) equivalent: ~5 million wafers per month (~1.5billion sq. cm per month)
 - from http://www.semichips.org/downloads/SICAS_Q4_01.pdf
- MOSIS (ref <http://www.mosis.org/Orders/Prices/price-list-domestic.htm>)
 - 1.5 micron cmos ~\$200 per square mm, 5 to 20 parts per lot ⇒ cost ~\$4K- \$1K per cm²
 - 0.18 micron ~\$1-2K per square mm for 40 parts ⇒ cost > ~\$2.5K per cm²



Zincblende crystal structure