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Chapter 1 Introduction

There are a number of novel devices that depend upon quantum tunneling and interference effects. Since some of these device ideas are difficult to test in the laboratory, the need to do optimization and inverse modeling in design of these devices suggests development of more comprehensive simulation tools.

Effective mass approximation-based Schrödinger Poisson simulation tools make it possible to rapidly simulate large device models. Convergence is an issue in part because the density of states function is highly nonlinear in these problems. The tight binding Hamiltonian can be used to do simulations of a range of materials including band mixing between materials. Valley mixing affects carrier concentration and transmission in devices with complex structures. Less rigorous methods based on effective mass approximations may be used to approximate these effects. However, there are differences between simulations based on coupling of effective mass equations and on the tight binding approximation.

One class of novel devices is simulated with these methods. The quantum storage device (QSD) is one of the new class of novel devices based on simulations and laboratory measurements. The addition of simulation methods introduced here add to the understanding of this device. Self-consistent solutions to the Schrödinger and Poisson equations have been widely used to identify both qualitative, and with varying degrees of success, quantitative behavior of Double Barrier Resonant Tunneling Diodes (DBRTDs).[1,2]. Self-consistent solutions are essential because quantum well diodes often incorporate lightly doped layers, and

the resulting space-charge effects can significantly influence device characteristics[3,4].

Chapter 2 Quantum Switching

Chapter 2 .1 Motivation

The semiconductor industry has used the ability to develop smaller and faster devices to fuel the explosive growth in productivity and functionality of electronic products. However, as devices shrink below 0.1 μm in size, physical phenomena must be identified that can produce devices that work as well or better than the larger devices utilized over the last forty years. In particular, quantum devices that work because of their small size, rather than in spite of it, become more attractive. It is critical to explore the potential of this new class of ultra-small devices.

The continued trend in the integrated circuit industry toward smaller individual devices (transistors) has actually become part of the financial structure of the industry. There is a focus in every area of device fabrication toward next generation technologies that scale (shrink) in a favorable way. Unfortunately, the resources and technology required to decrease minimum feature size in each generation of semiconductor devices continues to increase. Industry is now wrestling with fundamental physical device size limitations that threaten to limit further scaling. This suggests that new device building blocks be developed whose ideal size is in the new operating regimes. Many quantum phenomena evidence themselves most strongly in this sub-0.1 μm size range. This gives quantum devices, which may have no intrinsic scaling limitations, a potential role in the future of the industry.

Chapter 2 .2 Definition of Quantum Storage

Quantum storage cells are composed of a device or of several devices which depend upon quantum confinement, tunneling, or an interaction between these phenomena and charge effects or other effects for their operation. Preferably quantum storage cells should be composed of a single device which has multiple electrically distinguishable stable states accessed through one line and set through another. To be useful these memory cells should have terminal characteristics which allow them to drive variable length interconnects with acceptable noise margins and fan out.

Quantum storage based memory may be volatile or non-volatile, static or dynamic as in other types of memory. Non-volatile memory retains its memory state when power is turned off. Static Random Access Memory (SRAM) is an example of volatile static memory. Dynamic Random Access Memory (DRAM) is volatile and dynamic, requiring regular refresh cycles that consume significant amounts of power dissipated as heat. DRAM is significantly slower than SRAM but it is used because of its low cost and high density. There would be an enormous amount of interest in a device with SRAM performance at the cost and densities of conventional DRAM. Quantum storage based memory has potential to accomplish this.

There are two methods of achieving quantum storage. One is to use logic devices whose operation is based on quantum phenomena to make memory circuits. The other is to use a single device that exhibits memory characteristics using quantum phenomena. It is difficult to imagine a single device that is robust

enough to perform all of the functionality of a memory cell so most cases are a hybrid of these two methods. In either case, there is a significant advantage to compatibility with established fabrication methods and with existing linear and digital electronics families.

Chapter 2 .3 Cellular Automaton

There are several examples of quantum phenomena based logic which may be used to make memory. Lent[5-11] has proposed a family of logic based on coupled quantum dots that can be used to make interconnect lines and perform basic logic functions. These are known as Quantum Cellular Automaton (QCA). It is tempting to design devices from low dimensional structures, such as quantum dots whose charge is governed by quantization effects, particularly for digital logic. In order to be small enough to benefit from quantum confinement a quantum dot must be a few hundred nm in diameter or smaller. This makes it difficult to make physical contact between a quantum dot and a metal interconnect. The QCA is a suggested solution.

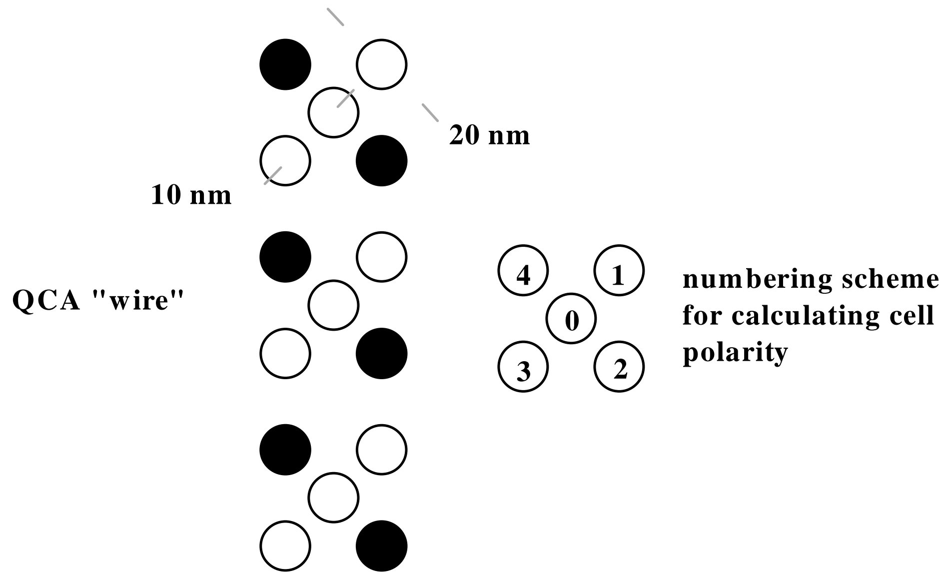

Figure Chapter 2 .1: A QCA wire is shown where the charge state at one end of the array of dots effects the charge distribution at the other. Here dark dots contain charge and clear dots do not. Coulombic forces cause charge to align as shown. In referring to occupied dots the numbering scheme shown is used.

In this scheme each cell is composed of five quantum dots, as shown in Figure Chapter 2 .1. Each dot may be 200 nm across and 100 nm from its nearest neighbor. Interaction between cells is governed by Schrödinger's wave equation

$$H\psi = E\psi \qquad \text{(Chapter 2 .1)}$$

$$H_0^{cell} = \sum_{i,\sigma} E_0 n_{i,\sigma} + \sum_{i,j,\sigma} t_{i,j}\left(a_{i,\sigma} a_{j,\sigma} + a_{j,\sigma} a_{i,\sigma}\right) + \sum_i E_Q n_{i,\uparrow} n_{i,\downarrow} + \sum_{i>j,\sigma,\sigma'} V_Q \frac{n_{i,\sigma} n_{j,\sigma'}}{\left|r_i - r_j\right|},$$

(Chapter 2 .2)

where H is the Hamiltonian, ψ is the wave function solution, E is the energy eigenvalue, E_0 is the onsite energy which is the same for all sites, $n_{i,\sigma}$ is the number operator generating an electron at site i with spin σ, $t_{i,j}$ is the tunneling energy from site i to site j, and E_Q is the coulombic energy required to have two

electrons on the same site of opposite spin. The interactions between cells is predominantly controlled by the coulombic perturbation between neighboring cells so that the Hamiltonian at cell 1 due to cell 2 is given by

$$H^{cell} = H_0^{cell} + H_{12}^{cell}, \qquad \text{(Chapter 2 .3)}$$

where

$$H_{12}^{cell} = \sum_{i,j,\sigma} V_Q \frac{\rho_{2,j} - \rho}{\left|R_{2,j} - R_{1,i}\right|}, \qquad \text{(Chapter 2 .4)}$$

and where ρ is some assumed fixed positive charge to achieve space charge neutrality. The polarity of a cell may be defined as

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{(\rho_1 + \rho_3) + (\rho_2 + \rho_4) + \rho_0}, \qquad \text{(Chapter 2 .5)}$$

where ρ_n is the charge at location n. This is the numbering scheme for calculating polarization of each cell and it has values in the range of -1 to 1. The lowest energy and preferred solution occurs when neighboring cells align themselves with the same polarization. If an initial polarization is supplied by a "driver" to a QCA quantum interconnect, a polarization of 1 or -1 occurs within a couple of cells alignment and continues to subsequent cells[5].

A range of logic circuits have been designed using QCA including fundamental AND and OR gates as well as more complicated circuits like a full adder. It may be dangerous to make assumptions about the state of a cell when the polarizing effects of the driver are removed, say to infinity. Since work is done in reading the state of a cell the very act of determining its state may change the polarity of a cell or entire QCA wire in an unpredictable way. In order to reliably achieve memory functions a memory cell constructed of basic QCA logic

elements may be used without making any assumptions about the volatility of the data.

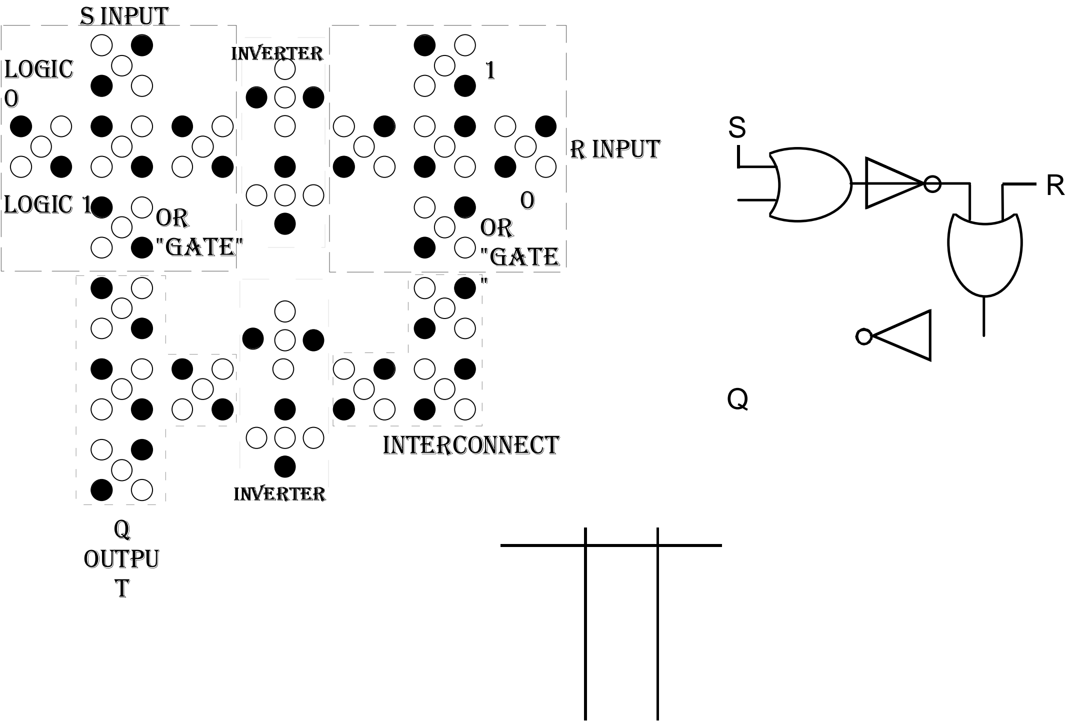

Figure Chapter 2 .2

Figure Chapter 2 .2 shows an SR latch composed of two NOR gates constructed from QCA logic. One NOR gate is in outlined for reference. The cell size is about 0.3 µm by about 0.4 µm. This is a SRAM cell comparable in size to a conventional DRAM cell.

A more critical assessment of this logic family must be considered. This thought experiment is carried out at T=0K. It could be tested at 4K but it would probably have to work at least at 77K (liquid nitrogen) to be useful. For space charge neutrality there must be two holes positive charge on each cell. This

suggests precise placement of two donor dopant ions in the memory cell would be required, where only statistical doping control has been demonstrated. Expected statistical variations in the doping should significantly change the electrical characteristics of each cell. Although direct write methods of photolithograpy do have the resolution required to create these patterns of dots, these methods have not been used for production. At the time of this writing fully functioning QCAs have not been demonstrated in the laboratory.

Chapter 2 .4 **RTD Based Logic**

Another example of a novel family of logic that may be used to create memory is based on Resonant Tunneling Diodes (RTDs). RTDs are ultra high frequency, generally two terminal, majority carrier devices usually built from III/V materials using Molecular Beam Epitaxy (MBE) composed of a heterostructure quantum well. The quantum well is usually on the order of 50 Å in width composed of a sandwich of barrier or high conduction/valence band offset on either side of a low conduction/valence band offset material. These devices are characterized by an “N” shaped I/V curve with a peak where the bias aligns a large carrier population at the contacts with a resonance in the well[12]. A valley or low in the I/V curve occurs when the applied bias aligns a very small carrier population in the contacts with resonances in the quantum well. Since transport is ballistic to the first order, the carriers do not scatter from one energy to another. Tunneling through a quantum well is a quantum phenomenon typically producing peak currents into the hundreds of kilo amperes/cm^2. By classical physics assumptions essentially no current would flow in these devices. Operating by

ballistic transport and having low intrinsic capacitance, they may be assumed to be, and are, high speed devices. The I/V curve of these devices may have negative differential resistance (NDR). An example of the structure and I/V curve are shown in Figure Chapter 2 .3.

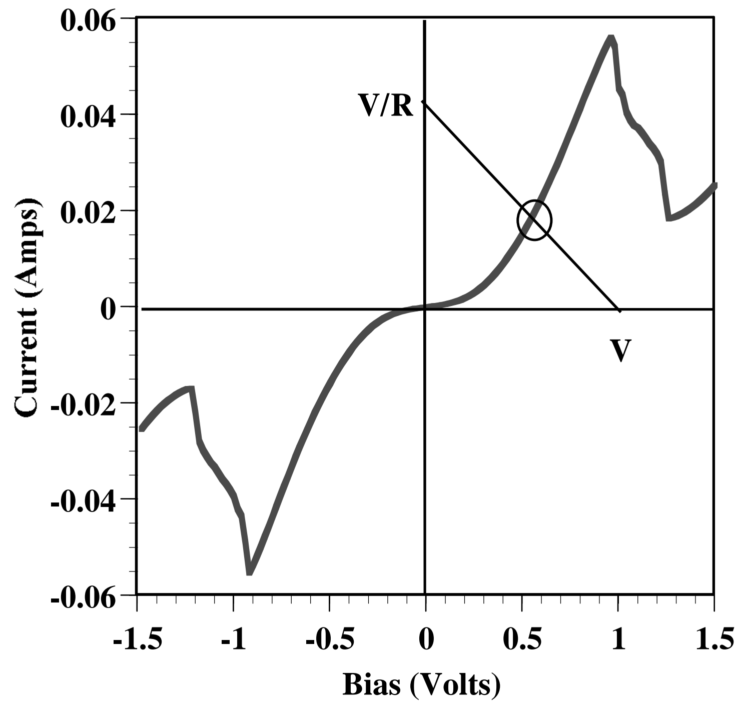

Figure Chapter 2 .3: This is a typical current density versus bias curve for a Double Barrier Resonant Tunneling Diode (DBRTD). Here a load line is shown as well. This is not quantitatively the load line used in this measurement [13].

The switching characteristic used to achieve this memory may fall into three categories. The first category is load line switching, where more than one solution may occur between the I/V characteristics of a nonlinear device and the load line. The history of the operation of the device governs which of these solutions is the operating point. This device may be used to make logic. The

second category is intrinsic bi-stability which occurs in some devices where charge is stored in the device during rising bias and supplied during decreasing bias. This hysteresis loop in the I/V curve causes there to be two possible operating voltages at a given current. Both of these types of logic are volatile. A third category, memory switching, refers to a case in which there are two stable states maintained with no power dissipation and without input, so it is non-volatile. Any of these might be used to create memory devices because they provide multiple operating voltages at the same current, dependent on history.

A number of attempts to make fast RTD based logic devices have been made[14]. These devices are based on load line switching. Load line switching based RTDs maintain their state while under load, but generally have poor terminal characteristics. Various schemes have been used to create a standard memory cell using these devices. A representative scheme is shown in Figure Chapter 2 .4[15]. This design from Texas Instruments employs “ultra-low” current density RTDs which dissipate 50 nW of standby power. These devices are constructed in the InGaAs/InAlAs and InP materials system. Heterostructure Field Effect Transistors (HFETs) are used for the switching transistors. This device is comparable in area to DRAM cells while not requiring a refresh cycle. Access times below 0.5 ns have been demonstrated. This architecture lends itself to vertical integration which aids in achieving high density. Multiple valued logic can also be achieved by using cascaded RTD structures. The device count to perform basic logic functions is much lower because of the use of multi-valued logic.

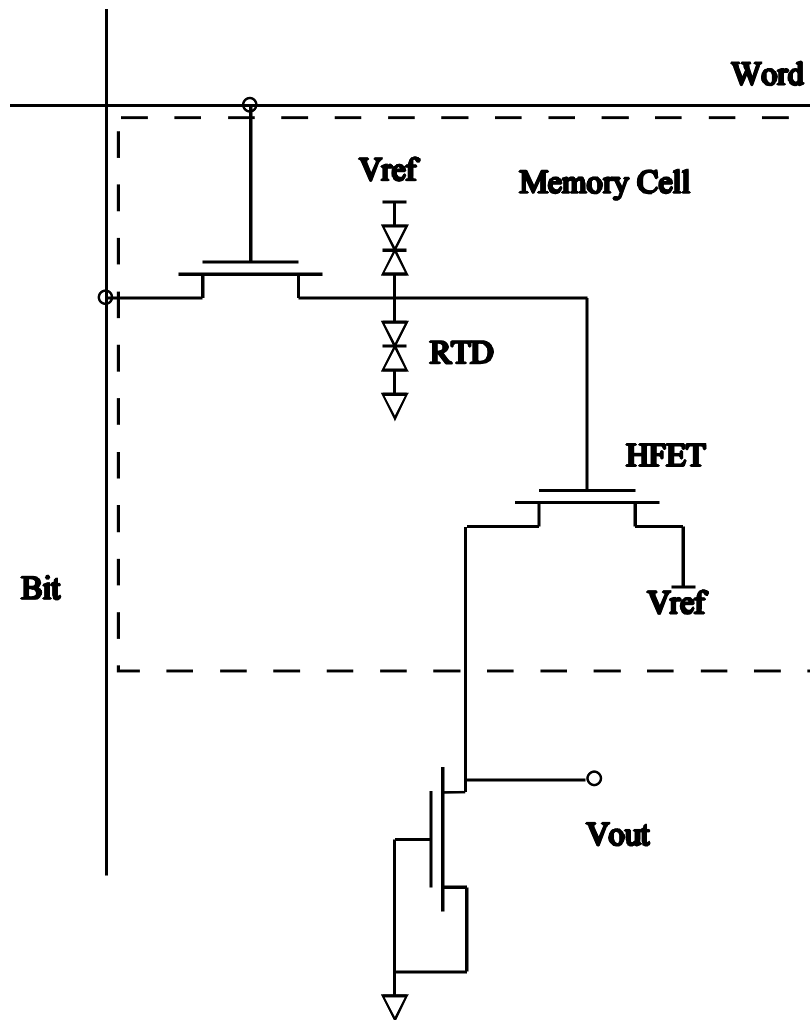

Figure Chapter 2 .4: This is a memory cell based upon a RTD using load line switching[15].

Chapter 2 .5 Memory Switching

A number of memory switching devices have been reported in the literature. Since they are non-volatile and static the device count to create very functional memory cells is low. Langmuir-Blodgett film-metal sandwiches, for

instance, show conductivity changes due to light irradiation or applied voltages[16]. For electrically switchable metal-film-metal structures a preliminary high voltage is applied as a forming procedure and then these devices display memory switching characteristics. A film thickness of 18 nm has been used with an off state resistance of 10^6 Ω and on state resistance of 20-100 Ω. This phenomenon may be caused by structural change in the film during switching. The device is simple to fabricate and is not necessarily incompatible with standard silicon fabrication procedures. One negative possibility is that switching is due to filamentary pathways. Sandwiches of metal-SiO_2 metal have also been observed to show memory effects after a similar forming procedure, but these have been attributed to highly conductive filamentary pathways of heavily doped silicon which form and are destroyed during switching[17].

Typically observations of memory switching are difficult to explain. Charge trapped in interface layers at a metal semiconductor boundary can result in memory switching. Such devices are generally not useful because they are difficult to reproduce. In any case two terminal devices that change resistance when a voltage is applied are difficult to use without supporting active electronics. On/off state resistances must not be ambiguous when observed through an interconnect of varying length/resistance to any particular memory cell.

Flash memory is a conventional type of memory that attempts to use trapped charge in a reproducible way. In this device a floating gate accumulates charge which affects the source drain current characteristics of the device. In Electrically Erasable Programmable Read Only Memory (EEPROM) hot electrons

are used to reset the memory state of the device. For a range of applications these are very useful devices. They have comparatively very long write times and some long term deterioration with the number of write cycles.

A flash memory cell which accumulates charge on a floating quantum dot above the channel has been built by IBM[18]. This device is an excellent example of the concept of a quantum device whose operating principles become more favorable as it becomes smaller. The change in threshold voltage (ΔV_t) resulting from charge trapped in the quantum dot increases as the quantum dot size decreases. This device is interesting because it has very small off currents in the 10 pA (10^{-9} ampere) range, small operating voltages, and potentially excellent scaling characteristics. It is not clear whether write times, which have always been the major drawback for electrically erasable flash memory, will improve in this design.

Chapter 2 .6 Quantum Storage Device

Gullapalli and Neikirk have proposed a method to engineer a charge trap. The Quantum Storage Device (QSD) is a modified quantum well diode that relies on the interaction of the quantum well region with N^- / N^+ / N^- doped layers to achieve its multiple conduction states[19-22]. Unlike other multiple state quantum structures, the QSD has different current versus voltage curves corresponding to the different conduction states. Preliminary experimental findings indicate that these states remain stable even under short circuit conditions and can only be switched from one state to another with the application of bias in excess of certain threshold voltages. Furthermore, calculations using a self-consistent coherent

tunneling model indicate that it is possible to design QSD cells with more than two states, creating the possibility of multi-state logic and multi-bit storage[19-21].

QSDs are functionally dissimilar to Shockley diodes or thyristors, which also change resistance at a break-over voltage but return to the original resistance at low voltage. The distinct differential resistance corresponding to each state in a QSD is retained even at zero bias until another switching voltage is applied, at which point it changes to that associated with the other state, as shown in Figure Chapter 2 .5.

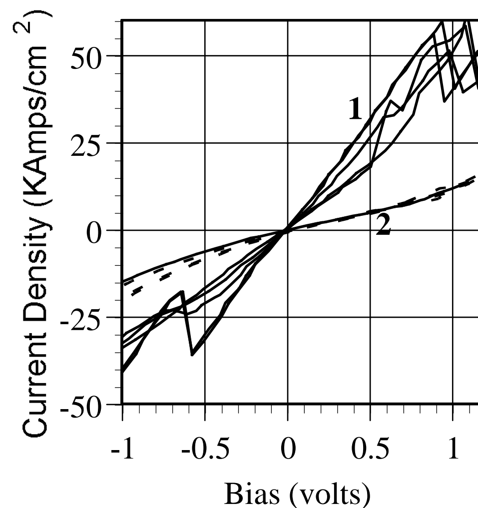

Figure Chapter 2 .5: These curves show several read write cycles of a QSD. The curves are grouped into states "1" and "2". Application of about 1.2 volts switches the device from curve "1" to curve "2". Application of about -1.2 volts switches the device from curve "2" to curve "1".

This multi-state behavior has been shown to occur in two terminal devices with a thin heterobarrier structure in close proximity to a novel $N^- / N^+ / N^-$ doped layer design. A double barrier quantum well structure has been grown in a Varian

Gen II MBE system that consisted of an 18 monolayer (ML) lightly doped n-type (10^{15} cm^{-3}) GaAs quantum well sandwiched between nominally symmetric 6 ML unintentionally doped AlAs barriers. The quantum well structure was surrounded on both sides by an 18 ML n-type (10^{15} cm^{-3}) GaAs layer, 43 ML n^+ ($4x10^{18}$cm^{-3}) GaAs layer, and 65 ML n-type (10^{15} cm^{-3}) GaAs layer. The doping sequence was found to be crucial to device operation. Only devices with quantum interference between a barrier structure and a well with a highly variable charge distribution show evidence of multiple conduction curves. In particular, conventional Double Barrier RTDs (DBRTDs) with monotonically doped layers show no evidence of multi-state behavior.

The device described above possesses memory, in that once the device is placed in one state it will remain in that state over a wide range of bias voltages including zero bias (i.e., the multiple states exist even at zero bias). Once the device is placed on one branch of its I-V characteristic, it will remain on that branch at zero bias. The state of the device at zero bias (which can be sensed via the value of its differential resistance), is determined by whether the device was last switched to the high current curve or to the low current curve. Even when the device is completely disconnected from the bias supply, or its terminals are short circuited, upon re-connection, the differential resistance is unchanged from its pre-set value. In this sense, the device possesses memory of its state, that can be retained without requiring any bias or dissipating any power. Simulations suggest that multi-state behavior occurs in other structures including single and triple

barrier devices as long as a N- / N+ / N- doped layers are in near proximity to the heterobarrier.

The potential advantages of the QSD over existing technologies are significant. First, the QSD can be scaled down to the limit of the photolithography system. From initial findings, it appears that the cell should work at mesoscopic geometries creating the possibilities of extremely high density memory or logic. The QSD has the advantage of operating at room temperature. Furthermore, there is a possibility that the QSD can serve as a static, non-volatile memory element or logic device with zero holding power, since the multiple conduction states are stable for extended periods of time even when completely disconnected from any power supply. Finally, since the QSD is a simple two dimensional structure, memory cells may be stacked on top of each other. This fact, coupled with the possibility of more than two conduction states per cell, offers other possibilities of achieving very high densities.

There are several problems that must be overcome before the QSD is a viable alternative. First, the switching characteristics of these two terminal devices are poor. Attempts have been made to develop a three terminal version by making direct contact to the N^+ layer[23]. Second, write currents are high. Third, on and off resistances are at best a factor of two different. Fourth, resistive memory elements require supporting electronics to make viable memory cells. And finally, the devices that have been made so far have been in the GaAs/AlAs materials system which is costly and difficult to integrate with conventional silicon technology.

Chapter 2 .7 Summary

These devices suggest directions for the next generation of technology. Determining which developments will thrust any particular technology into the forefront is obviously difficult. At any particular instant it is important to be aware of the short comings of proposed new technologies without assuming they are fatal. With that in mind, a critical assessment of these new technologies should be considered[24]. Because of the nature of these devices that may be difficult to do in the laboratory.

In some schemes new novel devices are used in memory cells containing conventional devices in order to improve functionality. It is important to note that the fundamental size limitation of a cell is determined by the largest device in the cell. Although lower device counts would be extremely important, the cell size decrease possible without fundamental changes in the technology of all the components is limited to a few generations.

Interconnects play an increasing part as the bottleneck in performance. Although Lent claims that QCA "wires" do not have the same interconnect limitations, they have not been built. The main advantage of smaller SRAM would be inclusion on the CPU of large amounts of fast memory eliminating or reducing caching requirements. This would require a compatible materials system which is difficult to achieve. As we go to smaller devices, design assumptions must take into account statistical variations inherent in using nano-structures[25].

An evaluation tool for quantum tunneling calculation that can handle a variety of effects would enable review of the physical characteristics of these and

other devices. The QSD, a pathological case, is characterized by tunneling through a heterostructure quantum well, quantum interference, large space charge effects, band mixing, and phonon scattering. Such an evaluation tool would be useful in modeling other devices.