Appendix A

Relative Importance of Injection Region and Drift Region Negative Resistances

Assuming that the injection conductance σ has been chosen to maximize quantum well performance, we can determine under what circumstances transit time effects (with negative resistance given by (2.5)) dominate the intrinsic negative resistance of a quantum well biased into NDR (with negative resistance given by (2.6)). Equation 2.6 yields the optimum value of σ for the quantum well

$$\sigma_{opt}^{QW} = -\omega\varepsilon \tag{A1}$$

Comparing this to (2.8), it is found that quantum well negative resistance is maximized at a value of $|\sigma|$ which is $\sqrt{3}$ larger than that which maximizes the transit time negative resistance. Assuming (A1) is used to determine σ and then applying (2.7) to determine the proper drift angle for the transit time region, the maximum negative resistances available from the two regions of the device are

$$R_{max}^{QW} = \frac{-l}{2\omega\varepsilon} \tag{A2.a}$$

$$R^{tt} = -\frac{\sqrt{2}-1}{2}\frac{v_s}{\varepsilon\omega^2} \tag{A2.b}$$

where R_{max}^{QW} is the maximum available negative resistance from the quantum well, and Rtt is the negative resistance available from the drift region. Requiring that $|Rtt| >> |R_{max}^{QW}|$ yields the condition

$$\omega << \left(\sqrt{2}-1\right)\frac{v_s}{l} \cong 0.4\frac{v_s}{l} \tag{A3}$$

Thus, at a given frequency, if the value of injection conductance is chosen to maximize the quantum well negative resistance, transit time effects will still dominate as long as the frequency is lower than $0.4v_s/l$. Assuming a conservative saturation velocity of 6x106 cm/sec and a typical quantum well length l of 10 nm, transit time effects dominate when the operating frequency is less than approximately 380 GHz. At this frequency a very high injection conductance of -2.7 (Ω-cm)-1 is required to satisfy (A1).

If the value of injection conductance is fixed, rather than being allowed to vary in accordance with (A1), a slightly less restrictive limit can be determined. For a fixed value of σ, we should consider two limiting cases for the negative resistance formulas (5) and (6), corresponding to $\omega << |\sigma|/\varepsilon$ and $\omega >> |\sigma|/\varepsilon$. For low frequencies we have

$$R^{QW} \cong \frac{l}{\sigma} \qquad \text{(A4.a)}$$

and

$$R^{tt} \cong -\frac{v_s \varepsilon}{2\sigma^2} \qquad \text{(A4.b)}$$

where (A4b) is a re-statement of (10). Thus, at low frequencies, the condition to ensure that |Rtt| >> |RQW| is

$$|\sigma| << \frac{v_s \varepsilon}{2\, l} \qquad \text{(A5)}$$

Using the typical values for v_s and l given above, (A5) requires that $|\sigma| << 3.4$ (Ω-cm)$^{-1}$, which is easily satisfied for the all quantum well structures studied to date.

For high frequencies ($\omega >> |\sigma|/\varepsilon$), the limiting values of negative resistance are given by

$$R^{QW} \cong \frac{l\ \sigma}{\varepsilon^2\omega^2} \tag{A6.a}$$

and

$$R^{tt} \cong -\frac{|\sigma|\ v_s}{\varepsilon^2\omega^3} \tag{A6.b}$$

where (A6b) is a re-statement of (2.11). Thus, at high frequencies, the condition to ensure that $|R^{tt}| >> |R^{QW}|$ is

$$\omega << \frac{v_s}{l} \tag{A7}$$

Again using typical values for v_s and l , (A7) leads to the requirement that the operating frequency be less than 760 GHz. Use of (A5) and (A7) provides a more realistic constraint on the requirement that $|R^{tt}| >> |R^{QW}|$ than (A3), since it appears very difficult to achieve values of $|\sigma| > 1\ (\Omega\text{-cm})^{-1}$. Hence, a sufficient condition to ensure that transit time effects dominate the intrinsic quantum well negative resistance is that (A5) and (A7) be satisfied.

Appendix B

Device Processing

In this appendix a summary of the processing steps involved in fabricating quantum well devices is presented. The MBE layers are metallized and subsequently processed using conventional photolithography and wet chemical etching to form devices. The sequence of steps involved using the equipment in our laboratory is as follows:

I. Metallization:

(a) Oxide strip: Etch the chip in a 2:1 solution of $HCl:H_2O$ for 10-20 secs to remove any oxides present on the sample. Clean in DI water. Blow dry.

(b) Metallization: Load the chip in the evaporator and metallize using a sequence of two layers: 1000Å of AuGe (88:12) alloy and 200Å of Ni.

II. Photolithography:

(a) Dehydration Bake: Bake the chip at 125°C for 10 minutes.

(b) Apply Adhesion Promoter: Spin on Microposit adhesion promoter at 4000 rpm for 30 secs.

(c) Apply Photoresist: At the end of this spin cycle repeat step (b) using the Microposit AZ1350J-SF photoresist.

(d) Prebake: Bake the chip at 70°C for 25 mins.

(e) Alignment and Expose: Follow standard instructions to mount the chip and mask in the HTG mask aligner [106] and then align. Clean and dry the mask prior to

alignment. Expose using the UV lamp and check the aligner logbook for exposure times. Demount the chip and mask.

(f) Develop: Develop the chip in a solution of Microposit 452 developer for typically 60 secs. Double rinse in DI water.

(g) Examine the chip under the microscope and measure a few resist patterns using the HMOS Micromeasure system.

(h) Flood Expose: Expose the chip under the UV lamp for 20 secs three times by pausing between exposures for 5-10 secs. Note that the total flood exposure time must be at least as long as the exposure time in step (e).

(i) Post Bake: Bake the chip at 125°C for 20-25 mins.

III. Chemical Etching

(a) Back Side Protection: Mount the chip on a glass slide using white transparent wax to protect the indium coated back side of the chip

(b) Ni etch: Etch the chip in a 1:1:3 solution of HNO_3:HCl:H_2O for 10-15 secs [107]. Rinse in DI water.

(c) Bake the chip at 125°C for 5 mins.

(d) Gold etchant: Etch the chip in a solution of commercial gold etchant (typically a 40g:1g:40ml solution of KI:I_2:H_2O) [107]. Use the etch rate specified by the vendor to set the etch time.

(e) Examine under the microscope to check if the AuGe is fully etched.

(f) Bake the chip at 125°C for 5 mins.

(g) GaAs etch: Prepare a 1:1:8 solution of H_2SO_4:H_2O_2:H_2O that is cooled down to room temperature. This solution is prepared by adding sulphuric acid to water and

allowing it to cool in a water bath. After this solution is cool add the peroxide and cool again. Etch the chip for 60 seconds and examine under a microscope. Continue etching until a 1 µm mesa is obtained.

(h) Demount the chip from the glass slide.

(i) Clean the chip thoroughly in acetone, ethanol, and DI water. Blow dry

IV. Rapid Thermal Annealing:

(a) Anneal the chip in a reducing ambient using forming gas (mixture of 90% nitrogen and 10% hydrogen) at 450°C for 50 secs using the tungsten halogen lamp rapid thermal annealing system.