Chapter 5

Fabrication of micromachined Fabry-Perot cavity pressure sensors

In this chapter the fabrication process for a micromachined Fabry-Perot cavity pressure sensor is described. First, general micromachining techniques will be reviewed. Included in the overview are two micromachining techniques, bulk micromachining and surface micromachining, and their limitations. The limitations of each technique are to be carefully considered when the fabrication process for the Fabry-Perot cavity pressure sensor is designed.

5.1 OVERVIEW OF MICROMACHINING TECHNIQUES

Micromachining technology has been developed dramatically over last two decades due to its versatile application in areas such as microsensors and microelectromechanical systems. Based on well-established IC technology the micromachining utilizes single crystal silicon substrates and deposited or grown layers on the substrate to build three-dimensional microstructures. As a mechanical material for the microstructures, single crystal silicon has excellent mechanical properties, such as a yield strength two times higher than steel, and the Young's modulus very close to that of steel. Also, mechanical hysteresis does not exist since crystal silicon is elastic. Table 5.1 shows important mechanical as well as electrical properties of a single crystal silicon.

The compatibility of the micromaching technology with IC technology enables the use of low-cost and high volume manufacturing processes for

microsensors and microelectromechanical systems. Generally, the processes are classified as either bulk micromachining or surface micromachining techniques. Bulk micromachining techniques employ anisotropic wet etch and wafer bonding to build microstructures. On the other hand, surface micromachining techniques utilize deposited or grown layers on the substrate. In the next two subsections, both techniques are discussed in further detail.

Property	*Measure*
Crystal structure	Diamond (8 atoms per unit cell)
Energy bandgap at 300 K	1.12 eV
Density	2.3 g/cm^3
Relative permittivity	11.7
Melting point	1415 ^oC
Thermal expansion	2.5×10^{-6} $/^oC$
Young's Modulus	1.9×10^{12} $dyne/cm^2$
Yield strength	6.9×10^{10} $dyne/cm^2$
Intrinsic carrier concentration	1.45×10^{10} $/cm^3$

Table 5.1 : Mechanical and electrical properties of a single crystal silicon [1, 2] .

5.1.1 Bulk micromachining techniques

As a subtractive process, anisotropic wet etching has been used for etching single crystal silicon substrates along crystallographic planes. For most wet etchants, the (111) crystallographic planes show a slower etch rate than any other planes. The anisotropy of the etching process allows the fabrication of many microstructures with high aspect ratios (i.e. vertical dimension to lateral dimension). Commonly used anisotropic etchants include ethylenediamine pyrocatechol (EDP) [3, 4] , potassium hydroxide (KOH) [3, 5] , tetramethylammonium hydroxide (TMAH) [6] and cesium hydroxide (CsOH) [7] . To have a high etch rate (e.g., 1 μm/min.), all the etchants mentioned above require elevated temperatures (from $60^{o}C$ to $100^{o}C$). Also, long etch times (typically up to 5 hours) are usually necessary to etch silicon substrates to build deep structures. These processing conditions do not allow the use of photoresist as a mask material because the photoresist layer lifts off due to degradation of adhesion. Either silicon dioxide or silicon nitride has been used as an etch mask for long wet etching at elevated temperatures. For all the etchants mentioned above, the selectivity of either silicon dioxide or silicon nitride to silicon substrate is very high (> 1000), thus the thicknesses of the dielectric layers required to etch a whole silicon substrate (typically 500 μm) are less than 0.5 μm.

Figure 5.1 illustrates an anisotropically etched (100) silicon substrate. Due to orientation dependency of the etch rate, the etched surface is bounded by the (111) planes, which have the slowest etch rate. For the silicon crystallographic structure, the (111) planes meet the (100) plane at an angle of

54.7 degrees. This structure could be produced by all the etchants mentioned above which have a slower etch rate along the (111) direction than the (100) direction. Note that undercuts occur even along the (111) direction for long etching as shown in Figure 5.1. To minimize unwanted undercuts the etch mask patterns need to be aligned along the (110) direction on the surface.

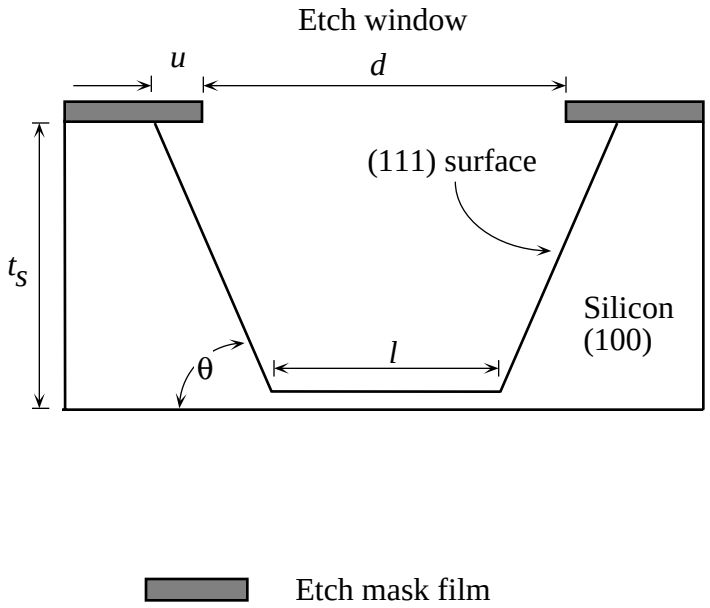


Figure 5.1 : Cross sectional view of an anisotropically etched silicon substrate. Etch mask film could be either silicon dioxide or silicon nitride.

If the patterns are aligned along the (110) direction, the final dimensions of etched structure, for example length *l*, can be calculated using both the etch rate of the (111) direction and the period time of etching. The length *l* and undercut *u* are

$$l = d + u - 2 \cdot \frac{t_s}{tan\theta} \tag{5.1}$$

and

$$u = \frac{\alpha(111) \cdot \xi}{sin\theta} \ , \tag{5.2}$$

where $\alpha(111)$ is the etch rate along the (111) direction, ξ is etch time and θ is equal to 54.7 degrees. The final dimensions must be accurately estimated when the etched patterns are to be used as front-to-back side alignment keys.

Instead of inclined etched walls, vertical etched walls can be formed by using KOH to etch a (110) substrate. Since KOH shows very high anisotropy etch ratio (> 500) of the (110) direction to the (111) direction, the etched area would be confined by the (111) planes, which meet the (110) plane at an angle of 90 degrees. With this property it is possible to generate very tall, densely populated microstructures in a substrate. However, it should be noted that KOH is not fully compatible with MOSFET technology due to possible potassium ion contamination; KOH also needs silicon nitride as an etch mask due to the high etch rate of silicon dioxide in KOH.

To avoid metal-ion contamination due to KOH and the toxic nature of EDP, TMAH (tetramethylammonium hydroxide) has been developed as an anisotropic wet etchant which is fully compatible with MOSFET processing [6] . However, it forms pyramid-shaped hillocks when the TMAH concentration of the solution falls lower than 22 wt.%. TMAH also shows lower crystallographic selectivity of the (100) direction relative to the (111) direction than KOH or EDP.

As implied in equation (5.1), the dimension, particularly thickness, of anisotropically etched microstructures could be mainly determined by the etch time. In practice, controlling only the etch time can not guarantee a target dimension repeatedly since the etch rate of silicon is usually not uniform over the wafer and is also a function of both the composition of the etch solution and operating temperature. To ensure both accurate dimensions of the etched microstructures and repeatability of the process, two etch stop methods have been developed. They use either heavy boron doping or electrochemically-controlled etching. These methods have been the most common techniques used to control the dimensions of silicon microstructures, such as diaphragms and grooves, with high precision.

For a heavily boron-doped silicon substrate the etch rates of both EDP and KOH reduce rapidly [8] . When boron concentration in silicon exceeds about $2\times10^{19}cm^{-3}$, the etch rate of the silicon decreases inversely proportional to the fourth power of the boron dopant concentration. To explain the underlying mechanism several models have been proposed. Palik *et al*. [9] observed that a passivation layer of SiO_x was formed on the surface of the boron-doped silicon substrate by using *in-situ* ellipsometric measurements in a KOH solution. The passivation layer is thought to be responsible for the reduction of the etch rate. Seidel *et al*. [10] proposed that the primary cause of the etch stop is the interrupted dissolution reaction due to lack of free electrons at the silicon surface. High boron doping concentrations reduces the number of free electrons near the silicon surface which leads to less generation of hydroxide ions that are required to etch silicon.

Etch stop is also achieved by applying a voltage between a lightly doped silicon substrate and the KOH solution. The etch rate decreases when the silicon substrate is biased above a certain voltage with respect to the KOH solution. This voltage is called the passivation potential (PP) and beyond it the etch rate drops rapidly due to an anodic oxide growth on the silicon surface [11] . This phenomenon has been widely employed to make diaphragms with a precisely controlled thickness by applying a reverse bias to a *p*-*n* junction formed inside the substrate. As far as the *p*-*n* junction exists, the reverse bias is mostly dropped across the junction, leading to etching of the *p* -type silicon. When the silicon is etched away and the *p*-*n* junction is destroyed, the potential of the remaining silicon then exceeds the passivation potential and etching stops. It is also suggested by the phenomenon that the etch rate could be locally controlled by generating a space-dependent potential distribution inside a wafer. Kwa *et al* [12] demonstrated fabrication of suspended masses and diaphragms with different thicknesses in a wafer by applying voltages to several contacts on one side of a lightly doped silicon substrate.

As an additive process, the wafer bonding technique has been used to build three-dimensional microstructures. The wafer bonding technique was originally developed for the fabrication of bipolar transistors [13] and manufacturing of SOI (Silicon On Insulator) integrated circuits [14, 15]. Bonding between silicon and silicon or between silicon dioxide and silicon dioxide has been developed for those applications. For silicon dioxide bonding, the surface of a wafer is pretreated with RCA solution (a mixture of NH_4OH and H_2O_2) to attach hydroxyl (OH) groups on the surface. When the polished sides of two

wafers are brought in very close contact, an attractive chemical interaction force develops between the wafers due to hydrogen bonds. On the other hand, for silicon bonding van der Waals forces are thought to be the dominant attractive forces since there are very few OH groups on the hydrophobic silicon surface. To achieve atomic level bonding, high temperature treatment (typically above $900\,^{o}C$) should follow after the two wafers are brought into very close contact by the attraction forces.

For microsensors and microelectromechanical systems, the wafer bonding technique has been modified to allow lower temperature processing and different interfacial layers, like silicon nitride [16, 17] . Those modifications are essential to allow the wafer bonding process to be done after fabrication of signal conditioning circuits for microsensors and microelectromechanical systems. Quenzer *et al*. [17] demonstrated wafer bonding at low temperatures (from 200 ^{o}C to 400 ^{o}C) by spining either ammonia silica solutions or sodium silicate on silicon wafers coated with either silicon dioxide or silicon nitride.

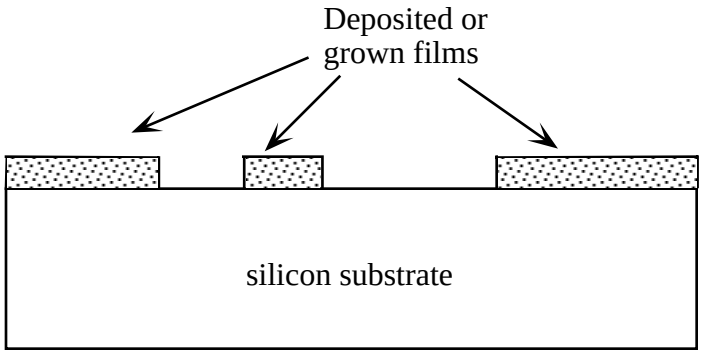
Using the bulk micromachining techniques described above, new microdevices, such as an accelerometer using piezoresistance [18] and a membrane pump [19] , have been realized. Also, the techniques have improved the performance of existing devices, for instance in a monolithic RF amplifier [20] .

5.1.2 Surface micromachining techniques

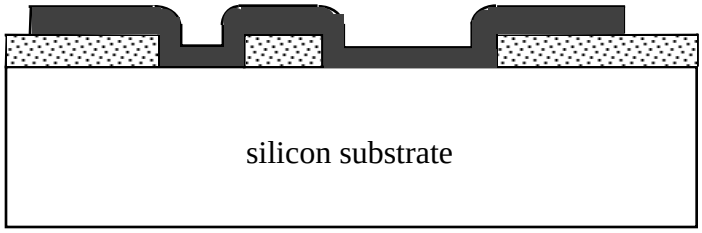
Surface micromachining techniques utilize deposited or sputtered films on a silicon wafer to build three-dimensional microstructures rather than building the

microstructures in the silicon wafer itself. The basic procedure of the surface micromachining technique is illustrated in Figure 4.2. First, a sacrificial layer is deposited and patterned on a silicon wafer (Figure 4.2(a)). Either a single layer or multiple layers are deposited to overcoat the sacrificial layer. After stacking films on the wafer, the top layers, which will be structural layers later, are patterned to expose the sacrificial layer to a layer-selective etching process (Figure 4.2(b)). The next step is etching the sacrificial layer selectively, leaving the free-standing structural layers behind (Figure 4.2(c)). Using these techniques cantilever beams or diaphragms can be fabricated without etching the underlying silicon substrate. Also, the vertical dimension of such microstructures, including the space gap of free-standing structures, can be precisely controlled by the thickness of the deposited or grown films.

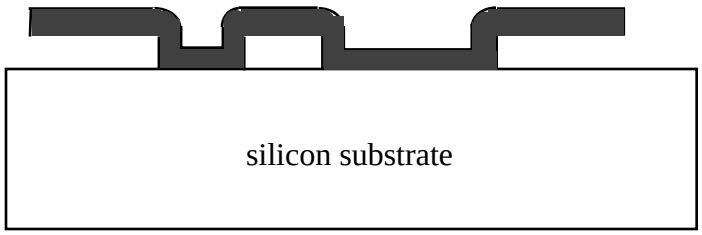
Among a variety of films used for surface micromachining techniques are polysilicon, silicon dioxide, silicon nitride, polyimide and nickel-iron permalloy [21, 22] . Selection of a sacrificial film depends on both the structural layers and the selectivity of the etching process.



(a) Deposition and patterning a sacrificial layer



(b) Deposition and patterning structural layers

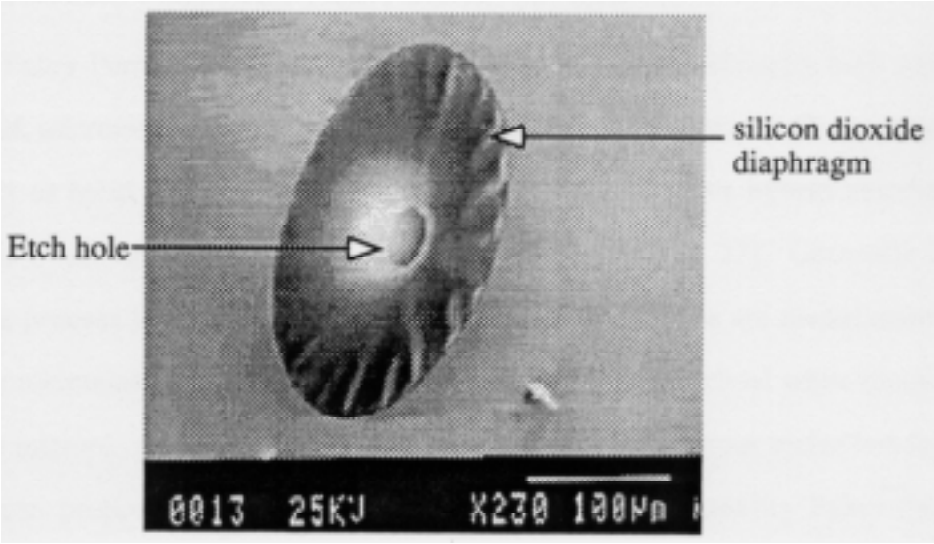


(C) After etching sacrificial layer

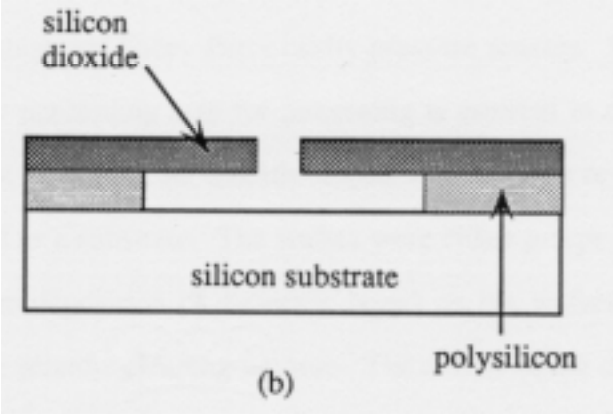
Figure 5.2 : Basic procedure of surface micromachining technique.

As mentioned earlier in chapter 4, micromachined structures suffer from residual stress built up during subsequent processing steps or the deposition process. The residual stress results in cracking or buckling of the microstructures released from the substrate. Figure 5.3 shows a 2000 Å thick silicon dioxide diaphragm which has buckled due to compressive stress. The silicon dioxide was deposited using low temperature ($450^{o}C$) LPCVD on a sacrificial polysilicon layer, which was later etched away using KOH. To reduce the residual stress of the microstructures multiple film stacks have been used. The composite structure compensates the residual stress by stacking films under tensile stress and films under compressive stress together.

Another problem associated with surface micromachining techniques is sticking of free-standing microstructures after rinse and dry steps following the sacrificial layer etching step. The sticking is thought to occur when the rinse solution evaporates. The thickness of the sacrificial layer is typically a few microns and thus an attractive force develops due to capillary action when the rinse solution dries. The attractive force tends to draw microstructures toward the underlying substrate. It was observed that once the microstructures are stuck to the substrate, it is very difficult to separate them. The most common method to avoid this problem is to use rinse solutions with low surface tension, such as methanol or *n*-hexane, as a final rinse [23] . Other methods, such as modifying surface termination [24] or using plasma etching to etch the sacrificial layer [25] , have been demonstrated.



(a)



(b)

Figure 5.3 : A buckled silicon dioxide diaphragm prepared with low temperature LPCVD. (a) SEM photograph of the top view ; (b) cross section.

5.2 PROCESS FOR FABRY-PEROT CAVITY SENSOR

Fabry-Perot cavity pressure sensors have been monolithically built using both bulk micromachining and surface micromachining techniques. Conventional methods to build Fabry-Perot cavity pressure sensors involve hybrid assembly which is a combination of etch-back and wafer bonding [26, 27] . Generally the bonding process leads to low yield when Fabry-Perot cavities are manufactured, because maintaining parallel as well as planar mirrors is not trivial while bonding the two mirrors. Integrated micromachining techniques, without wafer bonding, have been proposed and developed for self-aligned high quality Fabry-Perot cavity pressure sensors [21, 28] .

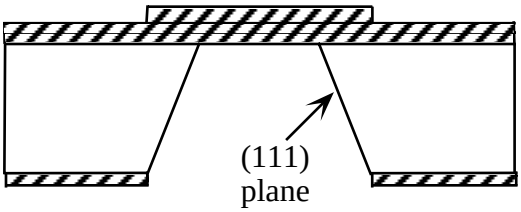
Figure 5.4 illustrates the process flow performed in our laboratory for monolithically integrated Fabry-Perot cavity pressure sensors. For simplicity, the photolithography processing step for patterning is omitted in this section and is fully described in Appendix B. Lightly doped 4-inch single crystal (100) silicon wafers were used as a substrate. The wafers were either p-type or n-type and 300 μm thick. Before deposition of dielectric layers on the wafers, the wafers were cleaned using the piranha cleaning process. The details of the cleaning procedure are given in Appendix C. After the piranha cleaning, multiple dielectric films were deposited using Low Pressure Chemical Vapor Deposition (LPCVD). The multiple film stack consists of two silicon nitride layers cladding a silicon dioxide layer and will be the bottom diaphragm (mirror) of the Fabry-Perot cavity (Figure 5.4(a)).

Silicon nitride was formed by reaction of ammonia (NH_3) and dichlorosilane ($SiCl_2H_2$) at the relative gas flow rate of 3.5:1 at 800^oC and 220 mTorr. Silicon dioxide was formed by reaction of silane (SiH_4) and oxygen (O_2) at the relative gas flow rate of 3:4 at 450^oC and 110 mTorr. To monitor the thickness of deposited films accurately, two bare wafers were placed into the two slots adjacent to the slot the wafer with the devices was in.

The thickness of each layer was chosen in such a way that the Fabry-Perot cavity is mechanically reliable, i.e., it should not buckle or crack, and must also give the desired optical response for a specific application. As shown in chapter 3, the residual stress of a multiple film stack is a critical factor to buckle or crack the stack when the stack is released from a substrate. It was observed that excessive tensile or compressive stress results in cracks or buckling in the released stack, respectively. The total residual stress of the stack could become slightly under tension by adjusting the thickness of each layer. This allows the mirror to remain flat when it was released from the substrate.

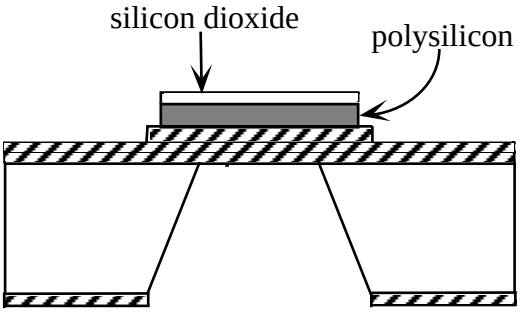
Multiple film stack1 consisting of two silicon nitride layers cladding a silicon dioxide layer

(a)



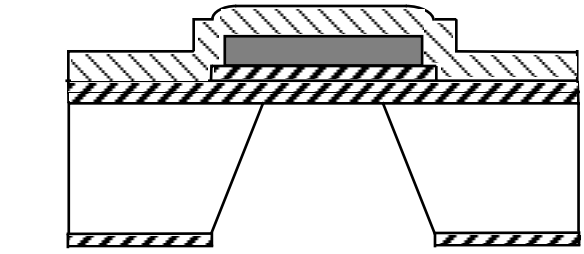
anisotropically
etched silicon

(b)



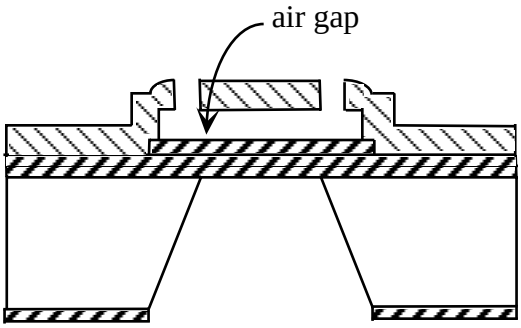
(c)

Figure 5.4 : Schematic process flow for monolithically integrated Fabry-Perot pressure sensor.



Multiple film stack2 consisting of the same layers as stack1 but different thickness

(d)



After etching sacrificial layer

(e)

Figure 5.4 : continued.

To design the optical characteristics of a Fabry-Perot cavity its application should be determined. For example, suppose the Fabry-Perot cavity is used as a bandpass filter. The mirrors of the cavity should be designed in such a way that the finesse of the cavity, which is inversely proportional to the band half-width at

resonance, becomes high. For pressure measurement, the mirrors of the cavity should be designed to give as large as possible a change in the optical response, e.g., reflectance or transmittance, for a full range of pressure to be measured.

Taking both the mechanical reliability and the optical response into account, two 1600 Å thick silicon nitride layers and a 4600 Å thick silicon dioxide layer were deposited as a bottom mirror. After the deposition of the bottom mirror, the dielectric film stack on the back side of the wafer was patterned using Reactive Ion Etching (RIE) to form etch windows for subsequent wet etching. With a pre-patterned photoresist mask, the silicon dioxide and silicon nitride layers were dry-etched using CF_4 and O_2. The relative gas flow rate of CF_4 and O_2 was 2:1 and the gas pressure inside the chamber was 50 mTorr. To have a highly anisotropic etch, a 370 *V* DC bias was applied to the sample inside the chamber. With 100 *W* RF (radio frequency) power, the etch rate of silicon dioxide and silicon nitride was observed to be about 700 Å/min. and 1000 Å/min., respectively.

After patterning the etch windows, the silicon substrate was anisotropically etched using either KOH or EDP to form the dielectric film diaphragm. Etching was carried out without stirring in a glass vessel at 80 ^{o}C. A reflux condenser unit was used to avoid the changes in the concentration of the etch solution during etching. Each wafer was lying inside the glass vessel. The etch rate of (100) silicon was about 1 μm/min. in both solutions. The etch rate of the silicon nitride was observed to be about 20 Å/hour in KOH and negligible in EDP. Both etchants were commercially obtained [29] . KOH-based etchant consists of KOH and water, i.e., the KOH concentration is 40 % weight. EDP-

based etchant consists of 450 *g* pyrocatechol, 800 *ml* water, and 3000 *ml* ethylenediamine [29] .

As shown in Figure 5.1, the final lengths of the dielectric diaphragm were determined by the etch time, the etch rate of (111) direction and the thickness of a silicon substrate. To have 50 μm and 100 μm square diaphragms, 475 μm and 525 μm diameter circles were patterned in the dielectric layers on the back side of a 300 μm thick wafer. The circle patterns produce square holes, which are automatically aligned in the (110) direction, as shown in Figure 5.5. This occurrs because the etch rate of the (111) direction was much slower than the (100) direction and perpendicular cuts along the intersection of the (111) planes and the (100) substrate surface became the (110) planes. For the (100) silicon wafer the (110) planes formed a square on the surface of the silicon substrate. Thus, alignment of the patterns in the (110) direction on the surface of the substrate could be avoided by using circular patterns.

The maximum size of the bottom diaphragm is limited by the size of the optical fiber which will be used as an interconnect and inserted from the back side of the wafer. To make the fiber contact on the (111) planes as shown in Figure 2.7, instead of directly contacting the bottom diaphragm, the size of the diaphragm should be smaller than the diameter of the fiber, which is typically larger than 100 μm.

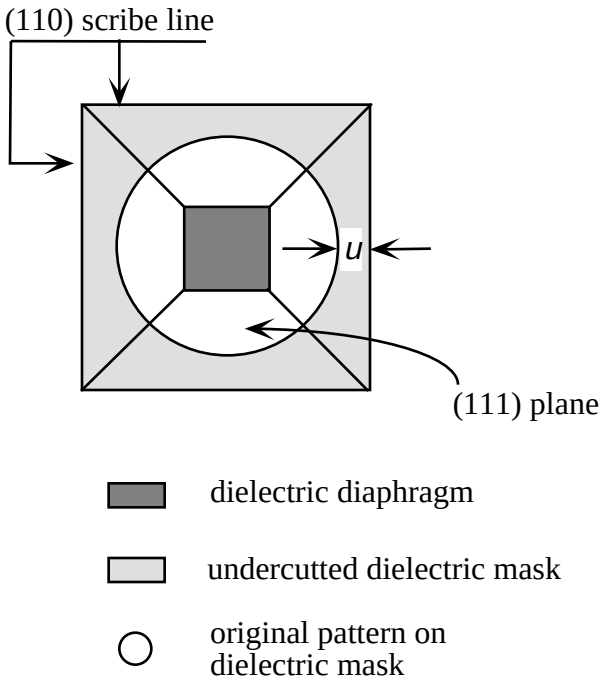


Figure 5.5 : Anisotropically etched (100) silicon substrate with a circular pattern. u is undercut obtained using equation (5.2).

The actual size of the diaphragms usually deviated from the designed value due to non-uniformity of the etch rate and thickness variation of the silicon wafers. Typical wafer-to-wafer variation in the thickness of the silicon wafers, for which the nominal thickness was 300 μm, was ±25 μm. This variation in thickness would result in ±35 μm variation in the length of a diaphragm. In addition to the variation in the thickness of wafers, etching along (111) direction should be considered since the undercut (u) shown in Figure 5.1 is not negligible

for long etch time (up to 5 hours). It was observed that the undercut was about 7 μm for a 5 hour etch process. This indicates that the ratio of the etch rate of (100) to (111) is about 40.

After making the bottom diaphragm, alignment keys were patterned with respect to the bottom diaphragm on the front side of the wafer before deposition of the polysilicon layer. This step is quite necessary to make it possible to find the bottom diaphragm after the deposition of the polysilicon layer. Otherwise, the bottom diaphragm can hardly be seen from the front side of the wafer after the deposition of the polysilicon layer. Even with 0.5 μm thick polysilicon layer most of the light is reflected from the top of the polysilicon or absorbed inside the polysilicon layer, making it impossible to align a mask with respect to the bottom diaphragm from the front side of the wafer. To pattern the alignment keys in the dielectric layers, the dielectric layers were dry-etched with a pre-patterned photoresist mask using RIE for 1 minute under the conditions described above. Figure 5.4(b) shows the dry-etched dielectric layers which are aligned to the bottom diaphragm.

Before deposition of the polysilicon, the wafer was cleaned using an RCA cleaning. When KOH was used as wet etchant, double RCA cleanings were performed to avoid possible light metal (e.g., potassium) contamination of the LPCVD furnace. Details of the cleaning procedure are given in Appendix C. After cleaning the wafer, polysilicon and silicon dioxide were deposited on the front side of the wafer. To prevent deposition on the back side of the bottom diaphragm, a dummy wafer was placed in the same slot as the wafer with devices to cover the back side of the wafer. A 6000 Å thick polysilicon layer was

deposited by LPCVD at 650 ^{o}C using silane (SiH_4). Deposition of a silicon dioxide layer followed. The silicon dioxide was used as an etch mask when the polysilicon layer was patterned using KOH. A photoresist layer could be used as an etch mask if the polysilicon layer is patterned using a dry etch, such as RIE. However, it was observed that a cleaner surface after etching the polysilicon was obtained when a wet etch was used. Figure 5.4(c) shows the patterned polysilicon and silicon dioxide which are aligned to the bottom diaphragm. Note that the size of the polysilicon pattern on the front side of the wafer is larger than that of the bottom diaphragm. This structure allows only one of the mirrors in the cavity to move when differential pressure is applied to the cavity.

After patterning the polysilicon layer, the wafers were cleaned using RCA cleaning. During the RCA cleaning, the silicon dioxide on the polysilicon was removed using buffered hydrofluoric acid (BHF). The next step is overcoating the pre-patterned polysilicon with another dielectric film stack, which consisted of two 600 Å thick silicon nitride layers cladding a 4200 Å thick silicon dioxide layer. This dielectric stack forms the top mirror and is freed after etching the polysilicon layer. Under the same conditions described above, silicon dioxide and silicon nitride were deposited on the front side of the wafer using LPCVD (Figure 5.4(d)). Again, the thickness of each film was chosen to reduce the total residual stress of the stack.

It was observed that the total residual stress of the top diaphragm should be even smaller so as to not crack the diaphragm because the etch windows, which are in the top mirror for etching the sacrificial layer, play a role as stress concentrators. Due to the etch windows, the stress of the diaphragm is not

uniform over the whole area of the top diaphragm. The localized stress induced by the etch windows could be much bigger than an average value of the residual stress. The stress concentration is a function of both the shape of the etch window and relative position of each window [28] . The stress concentration resulted in cracks in the film stack when the localized stress became bigger than the yield strength of a film in the stack. To reduce the effect of localized stress concentration, geometries without sharp corners were used as etch windows.

After the deposition of the top mirror, a photoresist layer was patterned for the etch windows to allow access to the sacrificial layer. The etch windows were formed in the top mirror using RIE. Upon removal from RIE chamber, the sacrificial layer, i.e. polysilicon, was etched using KOH. Etch rate of the polysilicon was 1 μm/min. at 75 ^{o}C. Both the top diaphragm and the bottom diaphragm were freed after etching the sacrificial layer as shown in Figure 5.4(e). The wafers were then rinsed in DI water.

To avoid sticking problems, the wafers were rinsed with methanol before being dried. As discussed in the last section, final rinse with low surface tension liquid was observed to help prevent sticking problems. As an illustration, Figure 5.6 shows a collapsed top diaphragm, which is stuck to both the substrate and the bottom diaphragm. Before being etched by KOH, the thickness of the polysilicon sacrificial layer was 0.5 μm. The cavity was rinsed in only DI water without a subsequent methanol rinse before being dried.

A complete Fabry-Perot cavity pressure sensor without sticking and cracking is shown in Figure 5.7. The cross sectional view of the device illustrates excellent step coverage of the deposited films and flatness of the top dielectric

film stack released from the silicon substrate. The dark region in the top mirror represents the silicon dioxide undercut in KOH. Since silicon dioxide is etched in KOH at a rate of a few tens of nanometers per minute, a few microns of silicon dioxide was laterally undercut during the etching of the sacrificial layer.

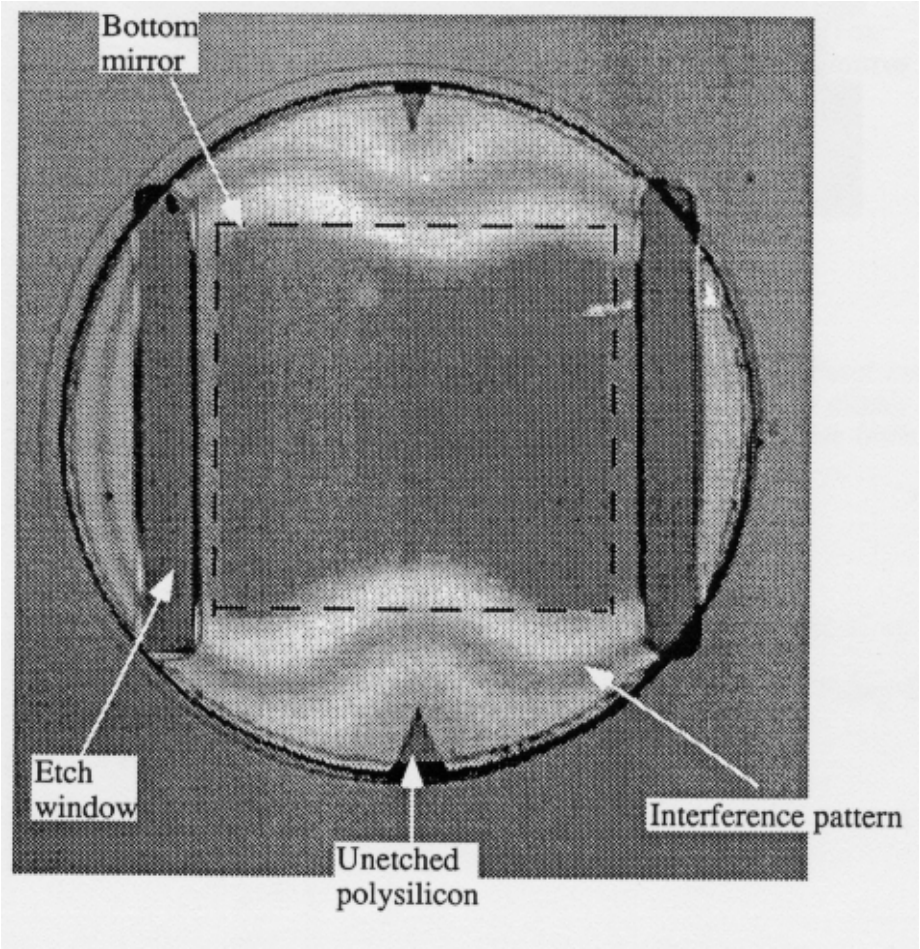


Figure 5.6 : SEM photograph of a Fabry-Perot cavity suffering from sticking. The top diaphragm collapsed onto the bottom diaphragm and the substrate. The interference pattern indicates bending of the top diaphragm.

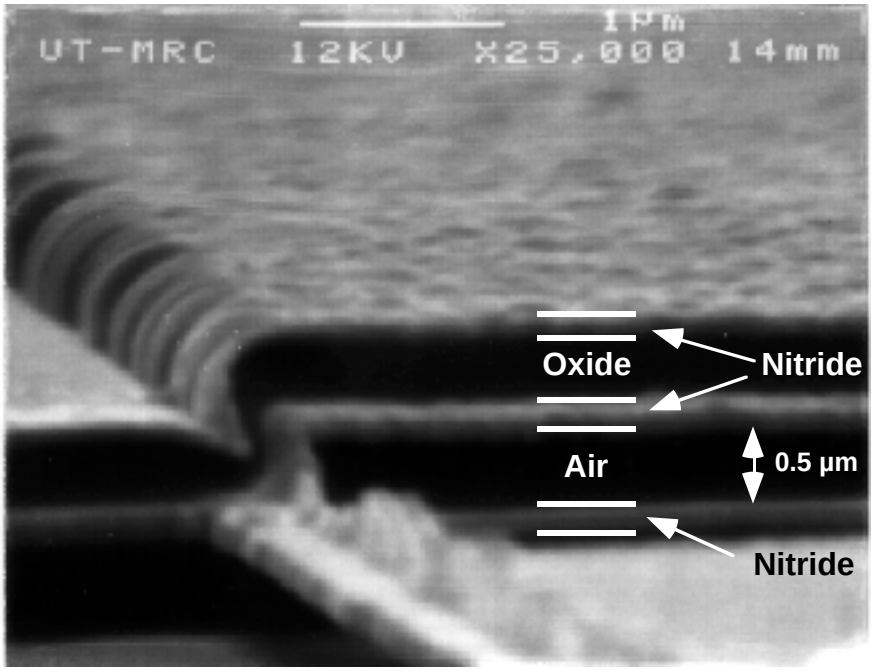


Figure 5.7 : SEM photograph of a cross section of a complete Fabry-Perot cavity pressure sensor. Note that the deposited films for the top mirror have excellent step coverage and a flat surface after release from the substrate.

After sucessfully fabricating the devices, each device was diced using a scriber for measurements. All processing steps described for the Fabry-Perot cavity pressure sensor are summarized in Figure 5.8.

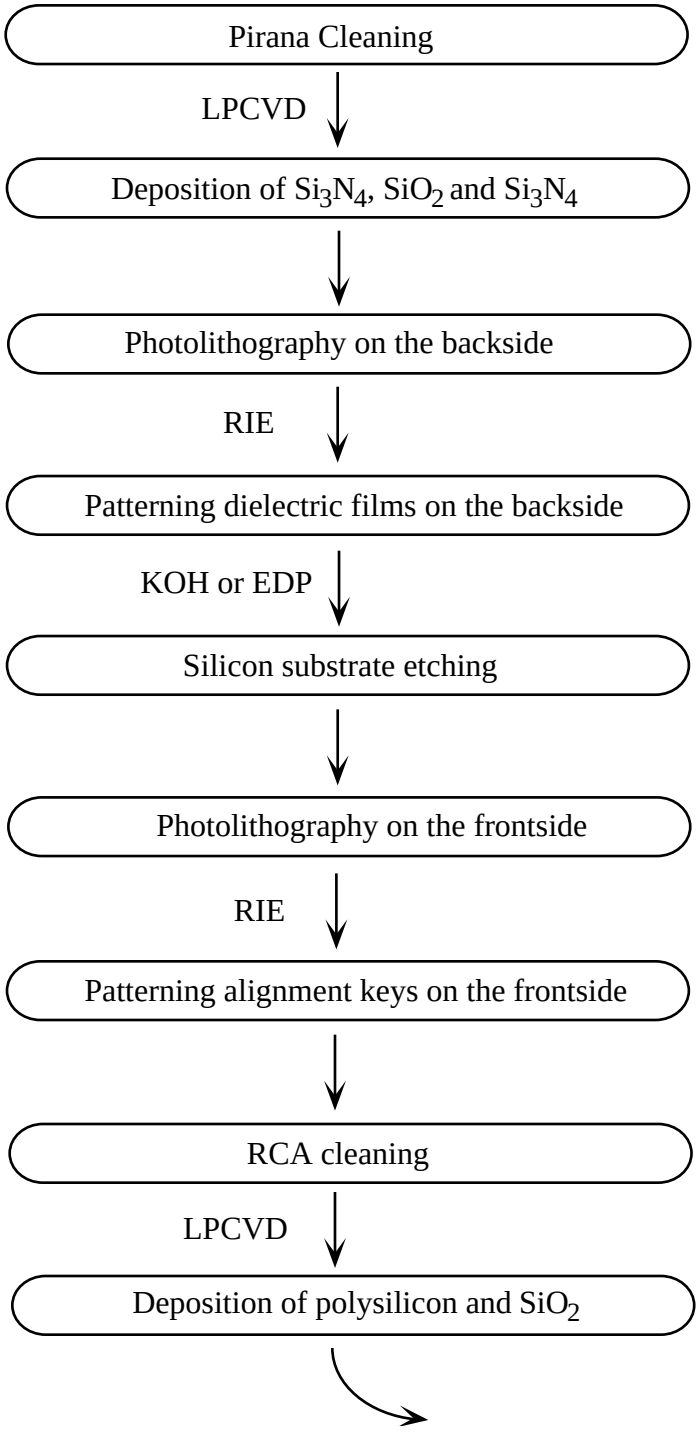


Figure 5.8 : Process flow chart for micromachined Fabry-Perot pressure sensor.

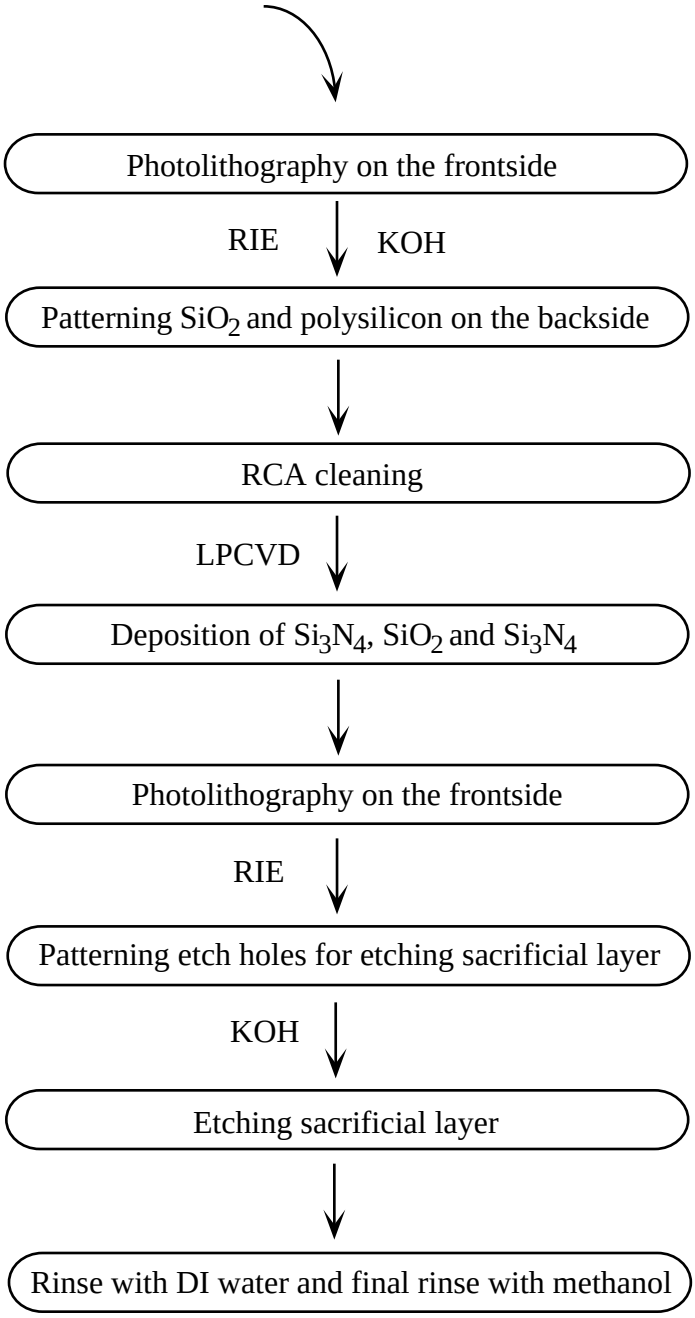


Figure 5.8 : continued.

5.3 SUMMARY

Monolithically integrated Fabry-Perot cavity pressure microsensors have been developed using both bulk micromachining and surface micromachining techniques. The fabrication process allowed us to build a high quality Fabry-Perot cavity without wafer bonding. This should lead to higher yield and more precise performance of the pressure microsensor. The gap between the two mirrors was accurately controlled by the thickness of the sacrificial layer. As discussed in chapter 2, an optimal design of this type sensor, which gives high manufacturing yield with accurate performance, could be realized by using this fabrication technique. Also, since the whole process for the Fabry-Perot cavity pressure microsensor was fully compatible with standard IC technology, the cost of each device could be low due to high-volume production.