EFFICIENT SERIES IMPEDANCE EXTRACTION USING EFFECTIVE INTERNAL IMPEDANCE

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EFFICIENT SERIES IMPEDANCE EXTRACTION USING EFFECTIVE INTERNAL IMPEDANCE

by

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DISSERTATION

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To my lovely wife Eunjoung Kim and son John (Kwang-Bok) Lee

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As semiconductor device speeds continue to increase it is becoming more critical to accurately model the parasitic effects of the interconnects (both on-chip and off-chip) between the digital circuit elements. The simulation of signal propagation along the interconnects using SPICE or some other circuit simulator is desirable. Therefore, electrical circuit representation of the interconnects (i.e., an equivalent electrical circuit representation of the physical interconnect) is required. A critical part of such extraction is the determination of the series impedance produced by finite conductivity wires and power/ground planes. For instance, resistance and inductance are frequency dependent due to the skin and proximity effects. Such frequency dependent effects can be determined using Maxwell's equation solvers, but using this approach as the first step in parameter extraction is computationally intensive, and frequently too slow. Faster and more efficient geometry-to-circuit extraction is necessary for regular lossy transmission lines and complex three dimensional structures.

This dissertation presents an efficient and accurate quasi-static methodology of evaluating the series impedance of interconnects based on the effective internal

impedance. Three effective internal impedance models are developed, which pre-characterize the internal behavior of conductors and assigns a complex impedance to the surface of the conductor. Therefore, the effective internal impedance replaces the conductor interior by a surface, and considerably saves computation time. This approach must be coupled with an electromagnetic field solver. For example, the conformal mapping technique can be combined with the effective internal impedance; here this approach is applied to various planar transmission lines, and shown to be numerically efficient and reasonably accurate. The effective internal impedance is more effectively incorporated with the surface current integral equations, the efficiency and accuracy of this technique is examined in this dissertation through several two and three dimensional structures of inter-chip interconnects, e.g. multichip modules (MCM) and print circuit boards (PCB), and comparisons are made to the rigorous quasi-static techniques of the volume filament technique (VFM) and the partial element equivalent circuit method (PEEC). The methodology using the effective internal impedance is shown to be fast and accurate and to be integrable with various circuit simulators.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES