

**MOLECULAR BEAM EPITAXIAL GROWTH AND FABRICATION OF  
MICROWAVE AND PHOTONIC DEVICES FOR HYBRID  
INTEGRATION ON ALTERNATIVE SUBSTRATES**

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1993

This work is dedicated to my father, James Jhy-Yuan Tsao, my mother, Vicki I-shien Wei Tsao, my brother Allen Tsao, my sister, Debbie Tsao and my wife,  
Jenn Fen Liu Tsao

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by

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In recent years, there has been considerable work on improving the high frequency and output power properties of double barrier resonant tunneling diodes (DBRTDs) which exhibit negative differential resistance (NDR) in their DC current-voltage (DC-IV) characteristics. Structural device parameters such as quantum well, barrier, and spacer layer thicknesses significantly impact the peak-to-valley current ratio (PVCR), the peak current density ( $J_p$ ), the difference between the peak voltage and the valley voltage ( $\Delta V$ ), and the difference between the peak current density and the valley current density ( $\Delta J$ ). Furthermore, variations in the dopant profiles, thickness of the spacer layers, and the contact resistance can significantly alter device characteristics. Optimization of the ohmic contacts to the DBRTDs was investigated. The impact of barrier asymmetries in AlAs/GaAs and AlAs/AlGaAs/GaAs DBRTD structures were studied. Through the use of an AlGaAs/AlAs "chair" barrier or composite barrier, a PVCR of 6.3 was measured. The impact of intentional small barrier thickness asymmetries on the DC-IV characteristics of AlAs/GaAs high current density DBRTDs was also examined. The thickness of the asymmetric barrier is adjusted nominally in increments of a half-monolayer based on growth rates using Reflection High Energy Electron

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The typical current densities of AlAs/GaAs DBRTDs are in the range of 20 kA/cm<sup>2</sup> - 100 kA/cm<sup>2</sup>. As a result of the significant device heating that can occur, the Epitaxial Lift Off (ELO) technique was used to remove the DBRTDs from their original substrates for subsequent hybrid integration to hybrid substrates of higher thermal conductivity. The ELO technique was used to create optically controlled Schottky contacted coplanar waveguide (CPW) phase shifters which are bonded to transparent substrates. In a similar fashion, ELO light emitting diodes (LED) such as AlGaAs/GaAs double heterostructure and multi-quantum well LEDs have been grown and hybrid bonded to transparent and pre-patterned substrates.

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- 
- Liu87 H.C. Liu, "Resonant tunneling through single layer heterostructures," Appl. Phys. Lett., Vol. 51, No. 13, pp. 1019-1021, 1987.
- Liu87 H.C. Liu, "Resonant tunneling through single layer heterostructures," Appl. Phys. Lett., Vol. 51, No. 13, pp. 1019-1021, 1987.
- Ada85 S. Adachi, "GaAs, AlAs, and Al<sub>x</sub>Ga<sub>1-x</sub>As: Material parameters for use in research and device applications," J. Appl. Phys., Vol. 58, No. 3, pp. R1-R29, 1985.
- Col76 D.J. Colliver, Compound Semiconductor Technology, Artech House, Inc., Editor, pp. 241-247, B.S. Perlman, "Pulsed Heat Conduction in a Layered Semiconductor-Metal Transferred Electron Oscillator Geometry," RCA Review, pp. 637-667, 1969.
- IsT91 M.S. Islam, A.J. Tsao, V.K. Reddy, and D.P. Neikirk, "GaAs on Quartz Coplanar Waveguide Phase Shifter," IEEE Microwave and Guided Wave Letters, Vol. 1, No. 11, pp. 328-330, 1991.