Chapter 5

Intentional Barrier Asymmetries in AlAs/GaAs Double Barrier Resonant Tunneling Diodes

5.1 Introduction

In recent years, there has been considerable work on improving the high frequency [*BrS91*] and output power properties of double barrier resonant tunneling diodes (DBRTDs) [*ReT90*]. Corresponding models and simulations have helped to direct device structure design as well as understanding some of the more fundamental issues regarding current transport through these devices. Structural device parameters such as quantum well, barrier, and spacer layer thicknesses significantly impact the peak-to-valley current ratio (PVCR), the peak current density (J_p), the difference between the peak voltage and the valley voltage (ΔV), and the difference between the peak current density and the valley current density (ΔJ). Furthermore, variations in the dopant profiles and the thickness of the spacer layers can also significantly alter device characteristics.

Intentionally induced structural asymmetries have been proposed and studied in AlAs/GaAs DBRTDs and AlGaAs/GaAs DBRTDs for a variety of reasons. Ricco and Azbel proposed that under bias, the electric field destroyed the symmetry of two symmetric barriers, and thus reduced the resonance in the device [*RiA84*]. To negate the effects of the asymmetry caused under bias, it was suggested that the entry barrier that the electron traverses first be made thinner with respect to the exit barrier that the electron traverses last. For purposes of examining issues of bistability and tunneling processes in DBRTDs, barrier thickness asymmetries have been incorporated [*AlE88*] [*GoT88*] [*RoG90*] . Typically these thick AlGaAs barriers were highly asymmetric such that they differed in thickness by more than a couple of monolayers. Inducing an asymmetry between the barrier heights of two AlGaAs barriers has been made [*ZaG88*] .

In our nominally grown symmetric AlAs/GaAs structures, a slight asymmetry is seen in the DC-IV characteristics where the PVCR is higher, the V_p is lower and J_p lower in the reverse bias, which corresponds to the electron traveling through the top AlAs barrier first, as shown in Figure 5.1.

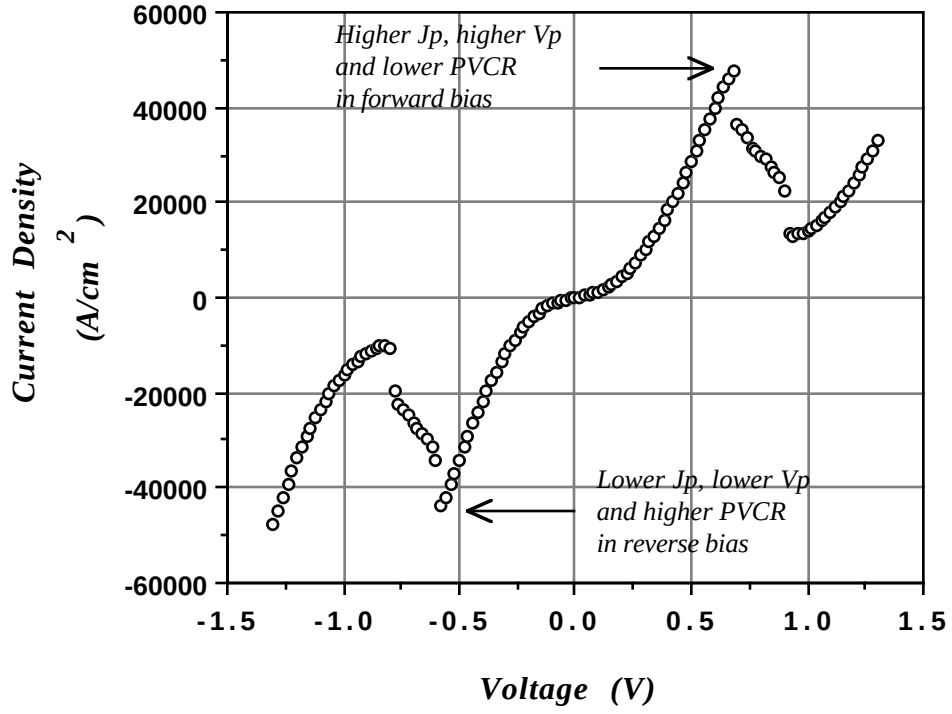

Figure 5.1: Measured J-V characteristics for a baseline, nominally symmetric AlAs/GaAs DBRTD. Slight asymmetries in the J-V characteristics are observed where the J_p is higher, the V_p is higher, and the PVCR is lower, all in the forward bias mode (Forward bias here implies the electron traverses the bottom AlAs barrier first.)

This asymmetry could not be fully explained fully using models which consider interface roughness at the inverted (GaAs on AlAs) and normal (AlAs on GaAs) interfaces [*LiC88*] . These models predict that when there is electron injection through the bottom AlAs barrier first (the normal interface first), the PVCR is higher than when there is electron injection through the top AlAs barrier first (the inverted interface). In the measurements taken in this research, the experimental results showed the exact opposite. Thus, there was some basis for believing that there was

some physical asymmetry in the device structure induced by MBE growth. Specifically, the V_p and J_p in the above J-V curve seem to indicate a slightly thicker top AlAs barrier. Therefore, an initial experiment was to find out how much asymmetry existed in the baseline AlAs/GaAs DBRTDs by intentionally varying the top AlAs barrier thickness. In this chapter, the impact of intentional small barrier thickness asymmetries on the characteristics of AlAs/GaAs DBRTDs, where the thickness of the asymmetric barrier is adjusted nominally in increments of a half-monolayer based on growth rates using RHEED intensity oscillations will be presented. Comparisons with simulations will also be presented. In addition, a DBRTD structure which utilizes a composite AlGaAs/AlAs "chair" barrier that was grown, processed and tested by this author will be presented. This device structure addresses the issues concerning inelastic tunneling and improved PVCRs.

5.2 Half-monolayer scale barrier asymmetries in AlAs/GaAs DBRTDs

The basic surface preparation of the substrate, MBE growth, and fabrication of the devices in this set of experiments follows the discussion presented in Chapter 4. Specific to this experiment, though, were the half-monolayer growths. Here the top AlAs barrier thickness was intentionally varied on the order of a half-monolayer, based on growth rates as determined from RHEED intensity oscillations. Growth rate calibrations were performed immediately before and after growth of the actual devices. The AlAs growth rates were 0.25 ML/sec or 0.30 ML/sec, while the growth rate for the GaAs spacer layers and GaAs well was 0.4 ML/sec. On six different samples, the bottom AlAs barrier and GaAs quantum well growth times were set to produce nominal layer thicknesses of 6ML and 18ML, while the top AlAs barrier growth time was adjusted to produce nominal layer thicknesses of 5, 5.5, 6, 6.5, 7, and 8 monolayers, (MBE Runs# 1021, 1525, 1523, 1526, 1020, and 1524, see appendix 1 for all J-V data), respectively. On one sample, the top AlAs barrier and the GaAs quantum well had nominal layer thicknesses of 6ML and 18ML respectively, while the bottom AlAs barrier thickness was increased to 7ML. See Figure 5.2 for a cross-sectional diagram of the device structures grown by MBE.

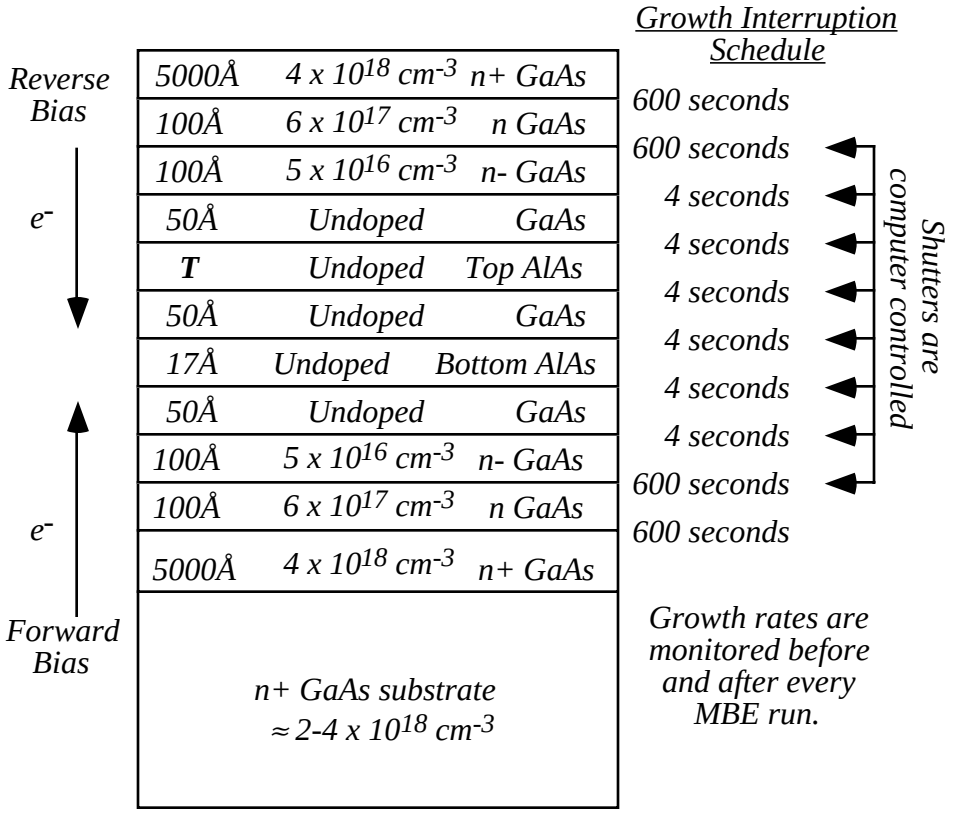

Figure 5.2: Illustration showing the cross-sectional layer structure of the AlAs/GaAs DBRTDs used to examine the impact of intentional barrier thickness asymmetries on the DC-IV characteristics. Note reverse bias implies electron injection through the top AlAs barrier first, whereas forward bias implies electron injection through the bottom AlAs barrier first. The top AlAs barrier thickness, T, was altered to produce nominal layer thicknesses of 5.0, 5.5, 6.0, 6.5, 7.0, and 8.0 ML.

After growth, all DBRTD structures were processed in the same fashion as described in Chapter 4. Briefly, before metallization, the photolithographically pre-patterned material was etched in a 2:1 $HCl:H_2O$ solution in order to remove surface oxides and to improve ohmic contact adhesion. An array of 5μm to 45 μm diameter Ni/AuGe/Ni/Au frontside contacts were defined using the lift off. Using the frontside contacts as an etch mask, the device structures were mesa isolated using an

8:1:1 H_2SO_4:H_2O_2:H_2O etch. Finally, the device structures were annealed at 450˚C for 30 sec.

Experimental and simulation results are summarized in Figures 5.3 and 5.4. In the simulations, an AlAs effective mass of $0.11m_e$ in the Schrödinger-Drift/diffusion and $0.09m_e$ in the Schrödinger-Poisson models provided the best fit to the experiments. Since these devices were measured at room temperature, it is unreasonable to expect that these simple models take into account all the mechanisms which affect the J-V characteristics. Ideally, low temperature measurements should be made when extracting a fitted AlAs effective mass [*LaA92*]. These experimental results were compared to simulations not to obtain close fits by using the AlAs effective mass as a fitting parameter, but to observe how much the J-V characteristics changed when varying the AlAs barrier thickness and by using a fitted AlAs effective mass that is within reason compared to the literature [*LaA92*] . The change from the band edge value of $0.15m_e$ to $0.09m_e$ has been attributed to strong renormalization of the Γ electron effective mass in the AlAs [*Brde90*] . Figures 5.3 and 5.4 show that for biases ("reverse" bias) such that electrons are incident on the top AlAs barrier first, the peak current density drops dramatically as this width is varied from 5 to 8 monolayers . For electron injection through the fixed-thickness bottom barrier first ("forward" bias), the variation is significantly less. Figure 5.5 shows similar behavior for the peak voltage in forward and reverse bias. Both the simulation and experimental results show that thickness variations in the entry barrier have a much larger impact on DC-IV characteristics than thickness variations in the exit barrier.

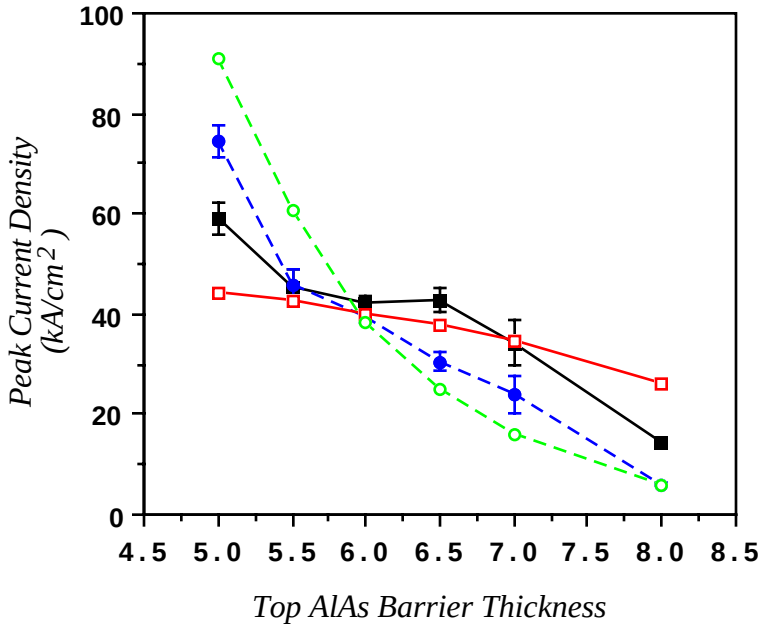

Figure 5.3: Peak current density vs. top AlAs barrier thickness for both simulation and experimental results. (- - ● - -): Electron injection through variable thickness top AlAs barrier first; (- - ○ - -): Simulation results (from **Schrödinger-Drift/diffusion**) for electron injection through variable thickness top AlAs barrier first; (——■——): Electron injection through 6ML bottom AlAs barrier first; (——□——): Simulation results for electron injection through 6 ML bottom AlAs barrier first. An AlAs effective mass of $0.11m_o$ was used in the simulations. One-sigma error bars are included for experimental data. The simulations shown here were run on a device simulator written by D.R. Miller.

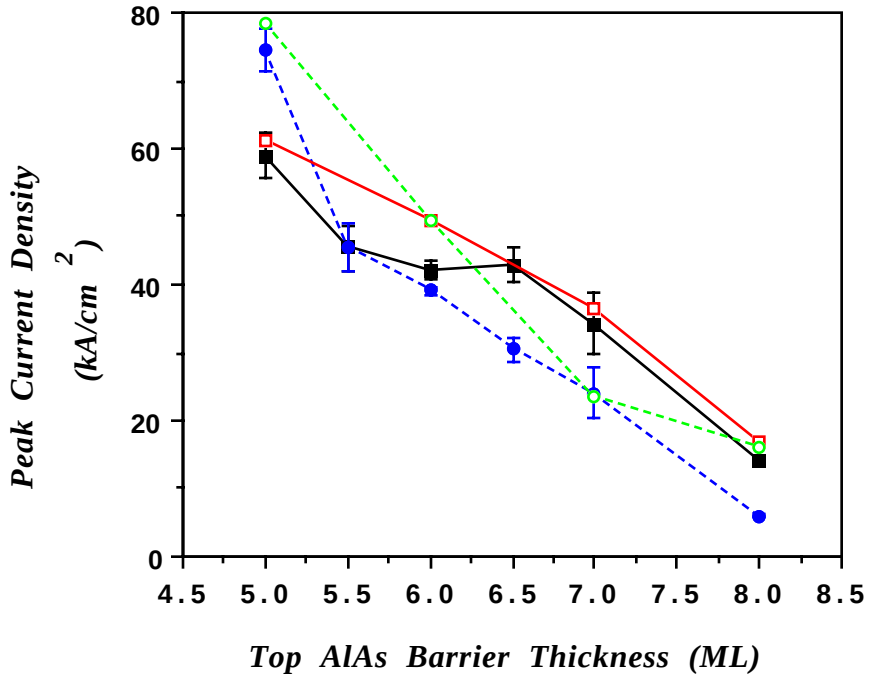

Figure 5.4: Peak current density vs. top AlAs barrier thickness for both simulation and experimental results. (- - ● - -): Electron injection through variable thickness top AlAs barrier first; (- - ○ - -): Simulation results (from **Schrödinger-Poisson**) for electron injection through variable thickness top AlAs barrier first; (——■——): Electron injection through 6ML bottom AlAs barrier first; (——□——): Simulation results for electron injection through 6 ML bottom AlAs barrier first. An AlAs effective mass of $0.09m_o$ was used in the simulations. One-sigma error bars are included for experimental data. The simulations shown here were run on a device simulator written by K.K. Gullapalli.

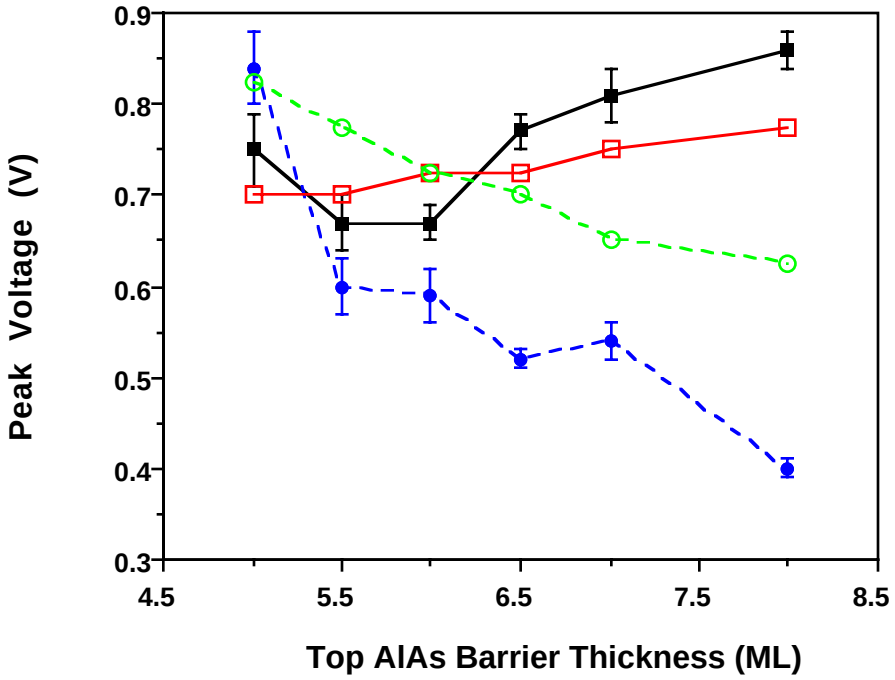

Figure 5.5: Peak voltage vs. top AlAs barrier thickness for both simulation and experimental results. (- - ● - -): Electron injection through variable thickness top AlAs barrier first; (- - ○ - -): Simulation results (from **Schrödinger-Drift/diffusion**) for electron injection through variable thickness top AlAs barrier first; (——■——): Electron injection through 6ML bottom AlAs barrier first; (——□——): Simulation results for electron injection through 6 ML bottom AlAs barrier first. One-sigma error bars are included for experimental data. The simulations were run on a device simulator written by D.R. Miller.

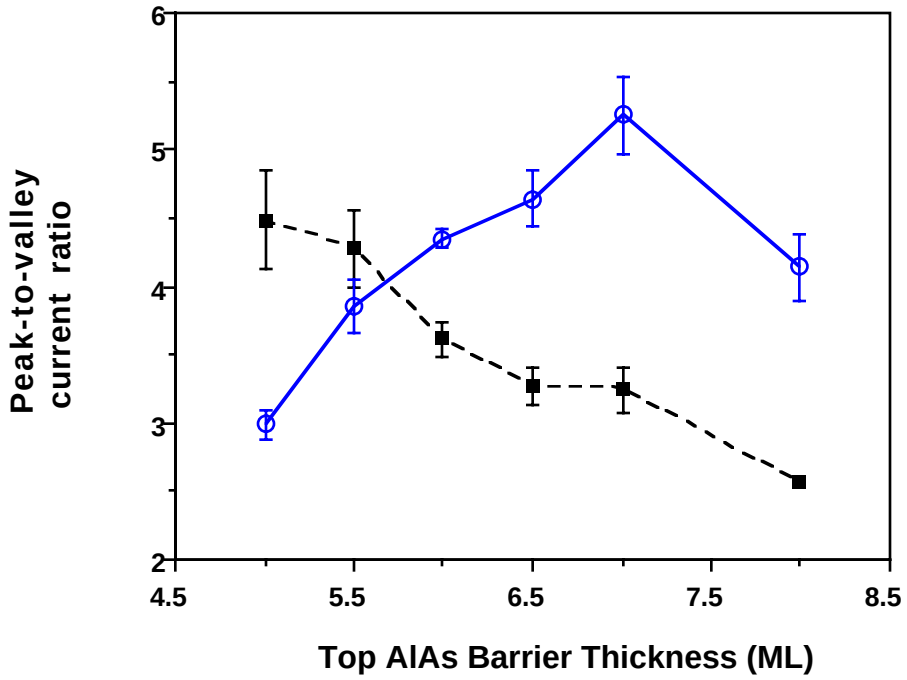

Figure 5.6: Peak to valley current ratio vs. top AlAs barrier thickness for experimental results. (—○—): Electron injection through variable thickness top AlAs barrier first; (- - ■ - -): Electron injection through 6ML bottom AlAs barrier first. One-sigma error bars are included for this experimental data.

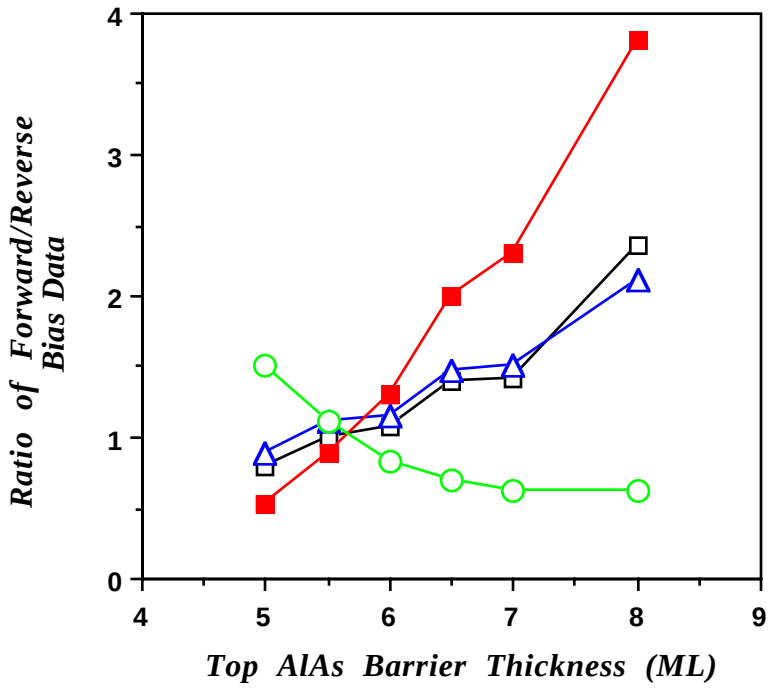

Figure 5.7: Ratio of the forward and reverse bias DC-IV parameters versus the top AlAs barrier thickness. This graph displays the asymmetry in DC-IV parameters as top AlAs barrier thickness is varied. The device with a 5.5 ML top AlAs barrier is shown to be most symmetric. (—□—): Ratio of the forward and reverse bias peak current densities, J_{pf}/J_{pr}. (—■—): Ratio of the forward and reverse bias valley current densities, J_{vf}/J_{vr}. (—○—): Ratio of the forward and reverse peak-to-valley ratios, $PVCR_f/PVCR_r$. (—△—): Ratio of the forward and reverse bias peak voltages, V_{pf}/V_{pr}.

Figure 5.6 shows that structural asymmetries also have a significant impact on peak-to-valley current ratio. Significantly higher PVCRs were observed when the electrons passed through the thicker barrier first, regardless of whether the thicker barrier is on the top or bottom of the GaAs well. As the top AlAs barrier thickness was varied from 5 ML to 7ML, an increase in the PVCR in the reverse bias case (electron injection through the top AlAs first) was seen. This trend did not continue, however, as the top AlAs barrier thickness was increased to 8ML. It is believed that as the thickness increased from 7ML to 8ML inelastic Γ_{GaAs}-X_{AlAs} tunneling effects may become significant, which tends to degrade the PVCR. Note that the trends observed here only apply to the devices with the exact same doping profiles and spacer layer thicknesses. The 7/18/6 monolayer AlAs/GaAs DBRTD demonstrated a PVCR of 5.6 in reverse bias, which is the highest reported to date in the literature for a simple AlAs/GaAs DBRTD. As stated previously in Chapter 4, for high frequency, high r.f. output power oscillators, the PVCR is not as important as ΔJ and ΔV, but the high PVCR is indicative of the maximum possible quantum interference effects that can occur using this specific material system. It is from this point of view that the high PVCRs are noteworthy. See appendix 1 for a summary of all J-V data.

The amount of DC-IV asymmetry in each of the devices is summarized by taking the ratios of the forward and reverse bias data, as shown in Figure 5.7. Interestingly, the device that exhibited the most symmetric characteristics was not the nominally 6/18/6 monolayer DBRTD, but rather the 5.5/18/6 monolayer DBRTD. This indicates that there may be an MBE growth asymmetry of unknown origin which causes the AlAs barrier grown after the GaAs quantum well to be approximately half a monolayer thicker than the barrier grown before the well.

Furthermore, a sample was run where the bottom AlAs barrier thickness was varied while the top AlAs barrier thickness was held constant at 6 ML (MBE Run# 1120, See Appendix 1). The bottom AlAs barrier thickness was 7 ML, giving a 6/18/7 structure. From the DC-IV measurements on this device, it is seen that J_p is now higher in the reverse bias mode and the V_p and PVCR are higher in the forward bias mode. These results follow the trends of the six samples described above.

5.3 Asymmetric Barriers Utilizing AlGaAs/AlAs/GaAs "Chair" Barriers

Inelastic tunneling through a Γ-X discontinuity, described in section 4.4 of Chapter 4, significantly contributes to the valley current in AlAs/GaAs DBRTDs which one may expect since the Γ_{GaAs}-Γ_{AlAs} offset is 1.04 eV and the Γ_{GaAs}-X_{AlAs} offset is 0.19 eV. Furthermore, the inelastic tunneling is more predominate in the valley where the electrons have more energy. Thus, one way to achieve improved PVCRs is to reduce to the inelastic tunneling in the AlAs/GaAs DBRTD.

The AlGaAs/AlAs "chair" barrier was conceived of by Cheng and co-workers as a way to reduce inelastic tunneling and obtain improved PVCRs in AlAs/GaAs DBRTDs [*ChH90*] . In this structure, a four monolayer $Al_{0.14}Ga_{0.86}As$ layer was placed adjacent to the bottom outer edge of an 7 ML/18 ML/7 ML AlAs/GaAs/AlAs quantum well structure. If the device structure is biased such that the electron traverses the "chair" barrier first, then a lower peak current density, J_p, would be expected. In addition, when the device is biased at V_v, the valley voltage, the "chair" barrier acts to reduce coherent tunneling through the Γ_{GaAs}-Γ_{AlAs} discontinuity since the "effective" barrier that the electron must tunnel is now thicker with the "chair" barrier and also acts to reduce the inelastic tunneling through the Γ_{GaAs}-X_{AlAs} discontinuity. This reduced inelastic tunneling can be anticipated since the Γ_{GaAs}-$X_{AlGa_{0.14}A_{s0.86}}$ discontinuity (0.42eV) is much higher than the Γ_{GaAs}-X_{AlAs} discontinuity (0.19eV).

Since implementation of the "chair" barrier reduces the peak current density, an AlGaAs/AlAs/GaAs "chair" barrier DBRTD was grown with slightly thinner barriers than those chosen by Cheng, et.al.. This device structure utilizes a 4 ML $Al_{0.20}Ga_{0.80}As$ "chair" adjacent to 6 ML/18 ML/6 ML AlAs/GaAs/AlAs quantum well structure, similar to the "baseline" DBRTDs used in this study. See Figure 5.8 for a cross-sectional layer schematic of this structure.

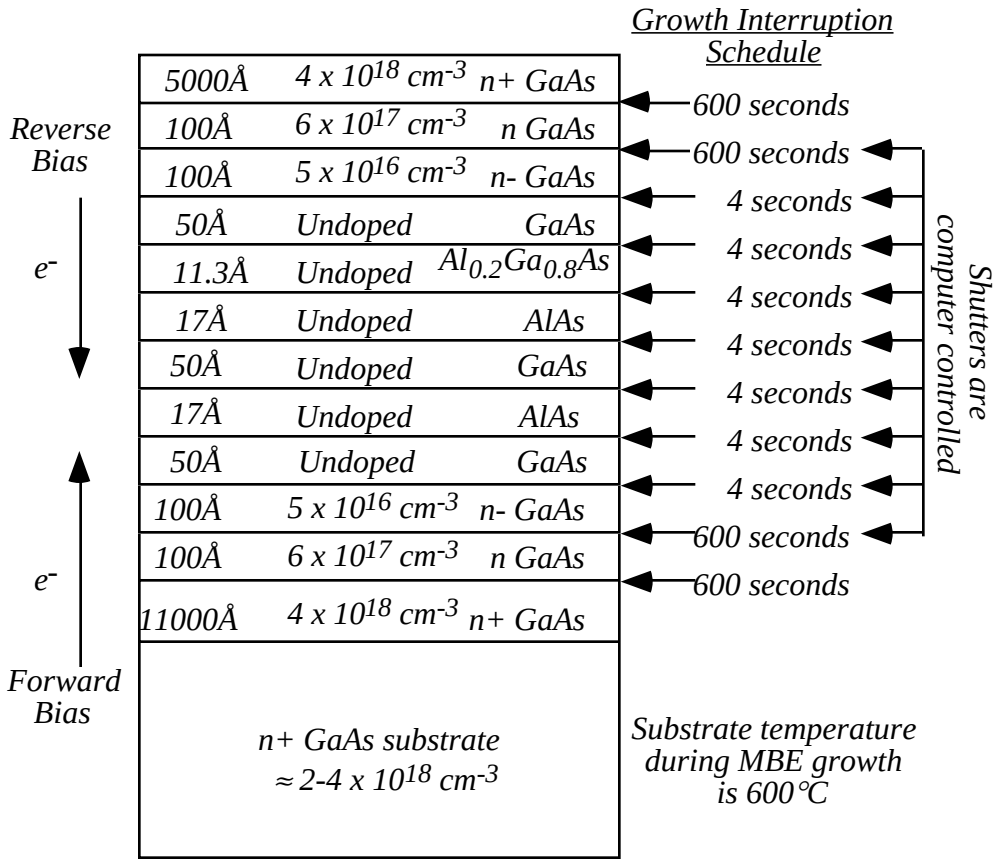

Figure 5.8: Cross-sectional diagram of the $Al_{0.20}Ga_{0.80}As$/AlAs/GaAs "chair" barrier DBRTD used in this study. The $Al_{0.2}Ga_{0.8}As$ "chair" was placed on the top AlAs barrier based on the higher PVCRs obtained when the "baseline" DBRTDs were reverse biased. Note that minor corrections have been made in the doping profiles and layer thicknesses in this cross-sectional diagram .

The conduction band profile for the $Al_{0.20}Ga_{0.80}As$/AlAs/GaAs "chair" barrier DBRTD is given in Figure 5.9.

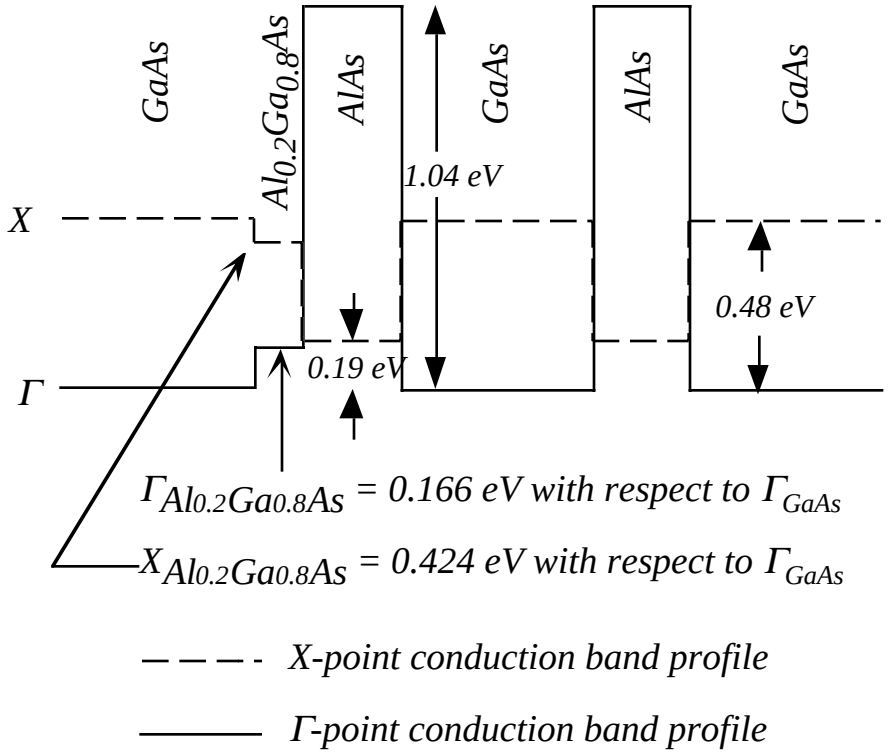

Figure 5.9: Conduction band profiles of both the Γ-point and the X-point minimums for the $Al_{0.20}Ga_{0.80}As$/AlAs/GaAs "chair" barrier DBRTD. All energies shown are in reference to the Γ-point of GaAs. The offset values for GaAs/AlAs are from Liu [*Liu87*] and $Al_{0.2}Ga_{0.8}As$/GaAs from Adachi [*Ada85*] .

Note that from the earlier discussion in section 5.2, it was decided to grow the "chair" barrier on top of the quantum well since higher PVCRs were normally observed when the electrons moved through the top AlAs barrier first. The MBE growth, fabrication, and DC-IV testing for this "chair" barrier DBRTD were performed by A.J. Tsao [*ReT90B*] using the methods as described earlier in Chapter 4. The results obtained by this author are shown in comparison to a "baseline" AlAs/GaAs DBRTD in Table 5.1. From the DC-IV measurements, an average PVCR in the reverse bias mode (reverse bias implies electrons traversing the "chair"

barrier first) for the "chair" barrier DBRTD of 6.0 ± 0.1 was obtained with a high of 6.3.

	Baseline AlAs/GaAs DBRTD.		AlAs/GaAs DBRTD with $Al_{0.2}Ga_{0.8}As$ Chair Barrier.	
Highest Peak to Valley Current Ratio	3.9 (Reverse Bias)		**6.3** (Reverse Bias)	
Average Values	Reverse Bias	Forward Bias	Reverse Bias	Forward Bias
Peak to Valley Current Ratio	3.7 ± 0.2	3.4 ± 0.2	6.0 ± 0.13	3.4 ± 0.15
Peak Voltage V_p (V)	0.93 ± 0.02	0.98 ± 0.03	0.47 ± 0.02	0.72 ± 0.02
ΔV (V)	0.33 ± 0.03	0.33 ± 0.05	0.30 ± 0.02	0.33 ± 0.03
Peak Current Density J_p (kA/cm^2)	52.4 ± 4.1	53.2 ± 4.2	31.3 ± 4.1	44.9 ± 5.3
Valley Current Density, J_v (kA/cm^2)	14.4 ± 1.3	15.8 ± 1.2	5.2 ± 0.6	13.3 ± 1.4
ΔJ (kA/cm^2)	38.0 ± 3.2	37.4 ± 3.5	26.1 ± 4.7	31.6 ± 6.7

Table 1: Comparison of J-V data for a "baseline" AlAs/GaAs DBRTD and the AlGaAs/AlAs/GaAs "chair" barrier DBRTD. Note that the "chair" barrier DBRTD obtained a PVCR of 6.3 at room temperature, which remains the highest PVCR to date for an AlGaAs/GaAs DBRTD. Both of the above devices were grown by MBE, processed, and DC-IV tested by A.J. Tsao.

This PVCR of 6.3 remains the highest PVCR obtained at room temperature for an AlGaAs/GaAs DBRTD. Furthermore, with the 6 ML AlAs barriers used in this study, as opposed to the 7 ML AlAs barriers used by Cheng, et.al., higher current densities were realized making this device more useful in possible oscillator applications. A comparison between the J-V characteristics of a "baseline" DBRTD and the "chair" barrier DBRTD is shown in Figure 5.10.

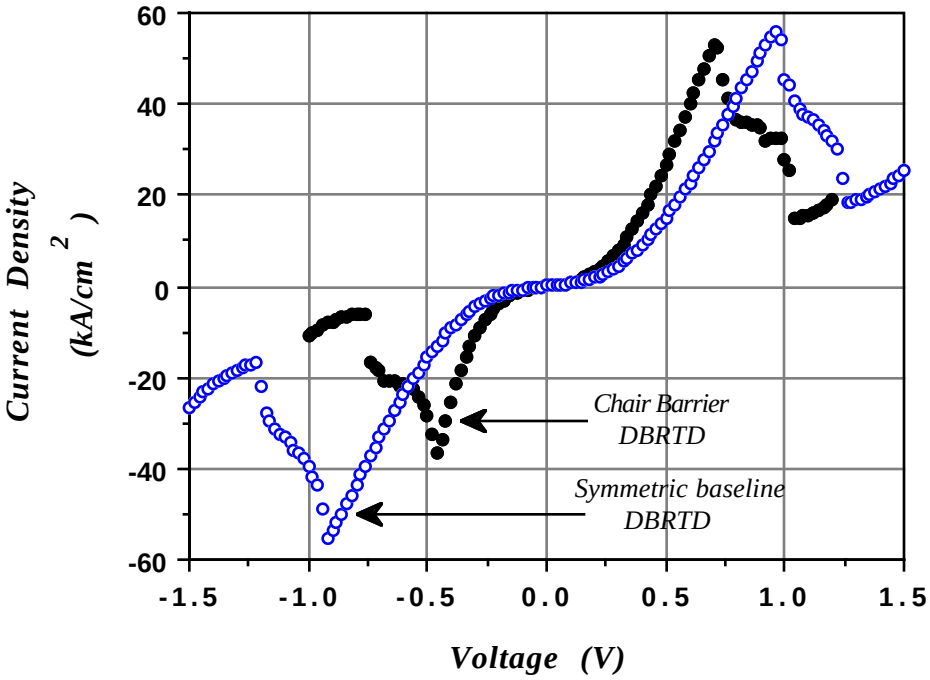

Figure 5.10: Measured J-V curves for a standard "baseline" AlAs/GaAs DBRTD and the AlGaAs/AlAs/GaAs "chair" barrier DBRTD, taken by this author. Note that in the reverse bias mode, the "chair" barrier DBRTD has a slightly smaller J_p than the standard DBRTD.

5.4 Use of an AlGaAs/AlAs/GaAs "Chair" Barrier in a QWITT Diode

As a result of the high peak-to-valley current ratios (PVCRs) obtained on the chair barrier DBRTD, mentioned earlier in section 5.3, an attempt was made to implement a similar type structure in an AlAs/GaAs QWITT. For this type of device to be useful, though, the ΔJ must be high, regardless of the PVCR. In other words, if the PVCR is improved but the current density of the device goes down, as observed in the "chair" barrier DBRTD in section 5.3, then there are no real gains in terms of using this device in an oscillator type application. Thus, in this study, the "chair" barrier itself was altered in an attempt to retain the beneficial features of this

composite barrier while increasing the current density of the device. To obtain this increase in current density, the AlAs portion of this composite barrier was made thinner by one monolayer (2.83Å), from ≈17Å down to ≈14.2Å. In addition, the $Al_{0.3}Ga_{0.7}As$ portion of the composite barrier was also made thinner by one monolayer, from ≈11.3Å to ≈ 8.5Å. From section 5.2, it is obvious that a one monolayer thinner barrier will result in a significant increase in the current density of the device, especially when the electron enters the thinner barrier first. The cross-sectional diagram of this device is shown in Figure 5.11.

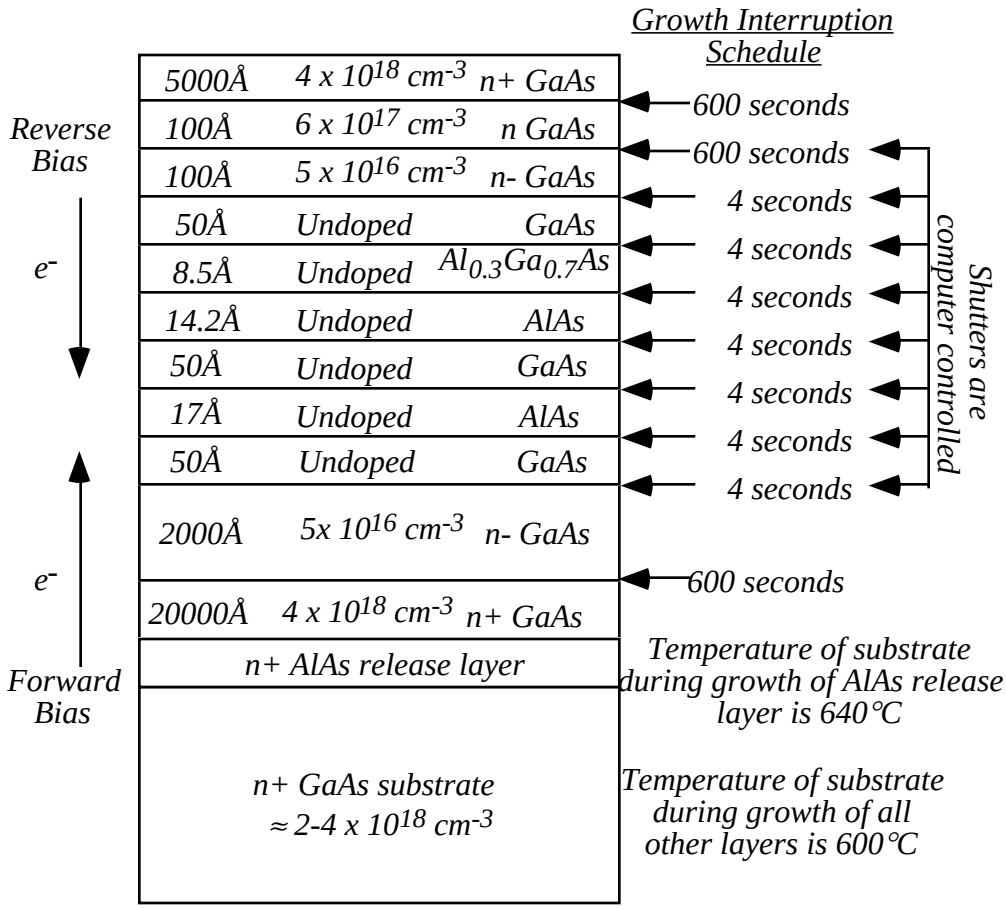

Figure 5.11: Cross-sectional diagram of the $Al_{0.30}Ga_{0.70}As$/AlAs/GaAs "chair" barrier QWITT discussed in this section. Here both the AlAs and $Al_{0.3}Ga_{0.7}As$ portions of the chair barrier were thinned by one monolayer to examine the impact on the measured J_p and PVCR.

The purpose of the AlAs release layer shown in Figure 5.11 will be explained in Chapter 6, section 6.3. It has minimal impact on the measurements to be described. The important J-V characteristics measured from this device are summarized in table 5.2.

Device Structure	Peak Voltage, V_p (V)	$\Delta V=V_p-V_v$ (V)	Peak Current Density, J_p (kA/cm^2)	PVCR
Chair Barrier QWITT (Forward Bias)	0.61 ± 0.07	0.36 ± 0.05	46.8 ± 1.5	3.0 ± 0.1
Chair Barrier QWITT (Reverse Bias)	-2.71 ± 0.1	-0.98 ± 0.09	-64.4 ± 1.9	3.8 ± 0.2

Table 5.2: Characteristic J-V data for a "chair" barrier QWITT structure.

From the above characteristics, the current densities are significantly higher than the baseline AlAs/GaAs QWITTs, described in Chapter 4, section 4.5. In addition, the ΔJ for this structure, in the reverse bias mode or "QWITT" mode, was ≈ 47 kA/cm^2 which is higher than typical ΔJ_s of ≈ 30 kA/cm^2 for the baseline AlAs/GaAs QWITT. The peak voltages, V_ps, of this device in the QWITT mode are slightly higher than those of the baseline structures. In this study, the chair barrier helped maintain a reasonably high PVCR and ΔJ as both components of the chair barrier were thinned by one monolayer.