Chapter 6

Application of the ELO Technique to Microwave and Photonic Devices

6.1 Introduction

The epitaxial lift off (ELO) method, already discussed in Chapter 3, has been shown to be an important processing technique that has allowed manipulation of extremely thin epitaxial films. It has also allowed the hybrid integration of devices from different material systems on a common alternative substrate. Hybrid integration with transparent substrates allows optical contact to the back of the device which is usually not accessible with common substrate thinning methods such as back-lapping. Hybrid integration with alternative substrates with higher thermal conductivity is useful for devices with high power dissipation. Furthermore, hybrid integration with Si substrates opens up the opportunity to integrate high quality, unstrained AlGaAs/GaAs devices with Si devices.

In this chapter, work will be presented on $Al_xGa_{1-x}As$/GaAs heterostructure devices that have been separated from their GaAs substrates and bonded to alternative substrates. DC-IV characteristics will be taken on AlAs/GaAs double barrier resonant tunneling diodes (DBRTDs) and quantum well injection transit (QWITT) diodes both before and after ELO. Furthermore, a discussion of the specific contact resistivity of the ohmic contacts formed on the backside of the ELO layers will be presented. The benefits of bonding various devices to transparent substrates will also be presented. These devices include an optically controlled coplanar waveguide structure and double heterostructure and multi-quantum well type light emitting diodes (LEDs).

6.2 Epitaxial Lift Off of AlAs/GaAs DBRTDs and Integration with Alternative Substrates using In-based Bonds

As discussed in Chapters 4 and 5, the AlAs/GaAs DBRTDs and QWITTs that have been grown, fabricated and tested in this research exhibit very high current densities that typically range from 20 kA/cm^2 to 100 kA/cm^2. With these high current densities, one can expect that the "junction" temperatures of these devices reach fairly high temperatures. These high temperatures can increase inelastic tunneling,

especially in AlAs/GaAs devices, and other thermionic based components of the overall current already discussed in Chapters 4 and 5. Increased inelastic tunneling contributes to a rise in the valley current and a reduction in the peak-to-valley current ratio (PVCR) of DBRTDs and QWITTs. Experimentally, the valley currents and PVCRs of AlGaAs/GaAs DBRTDs have been monitored as a function of temperature[*HuI87*] [*VaL89*] [*ShX91*]. Currently, there are no models which can accurately predict the overall characteristics of a DBRTD. The mechanisms which occur in the NDR region and into the valley are specifically not well understood at this time. In Chapter 5, an AlGaAs/AlAs chair barrier was utilized to reduce the valley current and increase the PVCR. In this section, through the use of ELO, the effects of placing the high current density AlAs/GaAs DBRTD and QWITT on alternative substrates of higher and lower thermal conductivity are examined. Without going through the thermal model, at least it is intuitive that the "junction" or in this case, the quantum well should be placed as close to a substrate of higher thermal conductivity as possible. With this goal in mind, ELO is an ideal tool for placing the "junction" of a device very close to an alternative substrate. Furthermore, a simple thermal model is used as a guide.

The first AlAs/GaAs DBRTD that has been lifted off its GaAs substrate was bonded to an In/AuCr coated glass slide. Since the two-terminal device structures that are fabricated in this process are not planarized, the n+ GaAs substrate is normally used as the second terminal, as shown in Figure 3.2. This first ELO AlAs/GaAs DBRTD was actually grown on a semi-insulating substrate and therefore could not be tested before ELO. A typical cross-sectional diagram of this device is shown in Figure 6.1. Since this sample could not be tested before ELO, the DC-IV characteristics of this device will be compared to DBRTDs with the exact same layer structures as this sample.

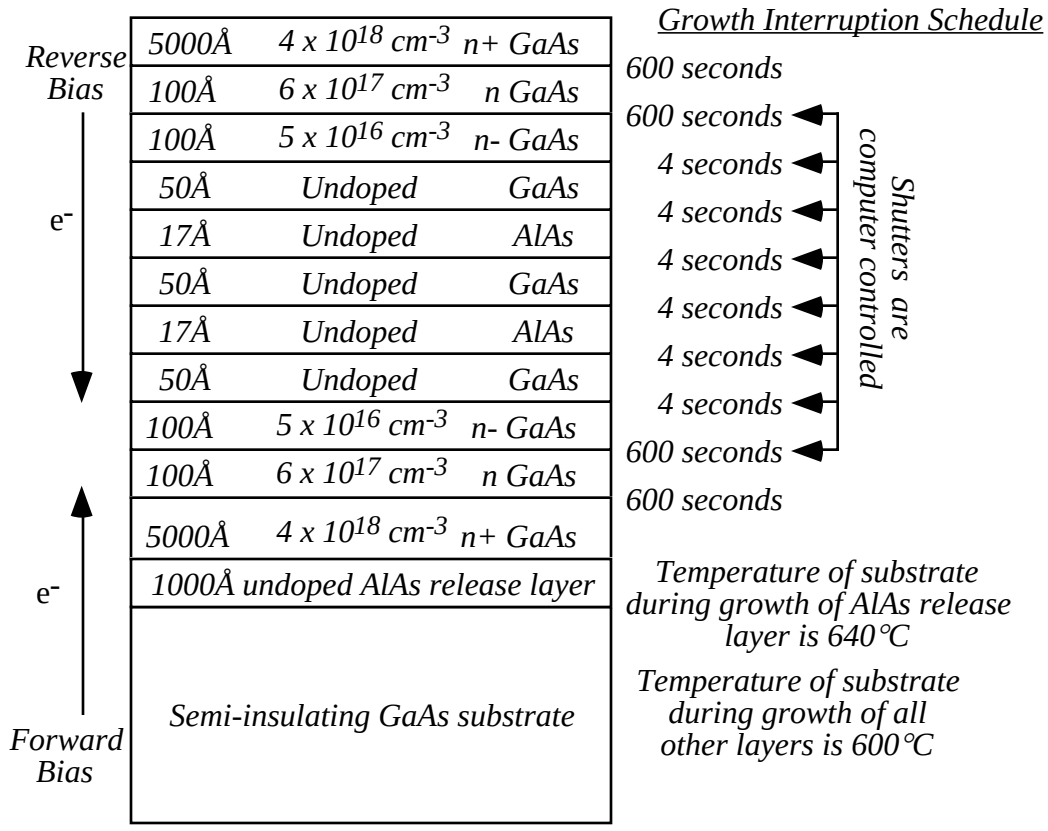

Figure 6.1: Cross-sectional diagram of the layer structure for the first ELO AlAs/GaAs DBRTD (MBE Run# 1043) grown in this study. Note that this sample was grown on a semi-insulating substrate and therefore could not be tested before ELO. Subsequent DBRTDs (MBE Run#1376) and QWITTs (MBE Runs# 1437 and 2028) were grown on n+ GaAs substrates with heavily n+ doped AlAs release layers.

The topside ohmic contact metallization was evaporated onto the pre-patterned sample using the fabrication procedures in Chapter 4, section 4.8. The sample was then mesa isolated, making sure that the mesa isolation etch did not penetrate the 5000Å n+ GaAs layer just above the AlAs release layer. The mesa etch used was a 8:1:1 H_2SO_4:H_2O_2:H_2O etchant. The ohmic contacts are then annealed at 450°C for 30 seconds. After complete processing, the samples were prepared for ELO as described previously in Chapter 3. As shown in Figures 3.3 and 3.4, since the quantum well of these DBRTDs also contain AlAs layers, it is very important to

protect them by ensuring complete coverage of the edge of the mesas with the Apiezon W black wax. After the ELO DBRTDs have lifted-off from the GaAs substrate, they were transferred onto an In/Au/Cr coated glass slide. The top indium metallization on the slide was 2000Å thick. The samples, still wet from a DI-H_2O rinse, were then placed on the metallized slide. The DBRTD/slide combination was placed overnight in a vacuum bag, which provides about 10^5 Pa (15 lb/in^2) of uniform pressure to the top of the sample. Afterwards the samples were baked in an oven at 90°C to remove any moisture and to obtain better adherence to the indium metallized slide. Subsequently, the lift off device was placed on a hot plate at 100°C to obtain direct heating of the back of the glass slide. Slight deformation of the black wax carrier did occur which resulted in a few cracks in the ELO film. After cooling, the Apiezon W wax was removed with trichloroethane (TCA), with the ELO DBRTDs remaining on the In/Au/Cr glass slide. The ELO DBRTDs were then annealed at 350°C for 150 seconds in order to form an alloyed In/GaAs ohmic backside contact [*LaK84*] . The purpose on the Au is to help reduce the sheet resistance of the composite In/Au/Cr since this layer must now be used as the 2nd terminal to the ELO DBRTD. The Cr is used to ensure that the composite metallization adheres to the glass slide.

Upon completion of processing the devices were tested using a Keithley 230 programmable voltage source and a Keithley 195A digital multimeter controlled by an IBM PC-AT. The results shown here are for devices approximately 3-5 μm in diameter. The ELO DBRTDs were tested with a two-probe arrangement with one probe touching the topside contact and the other probe touching the In/Au/Cr metallization on the glass slide.

The current density-voltage (J-V) characteristics (average and standard deviation) for both structures are summarized in Table 6.1. Also a typical forward bias J-V characteristic of the ELO DBRTD is plotted together with forward bias J-V characteristics of the baseline DBRTDs in Figure 6.2. Forward bias is defined as electron injection from the backside contact through the quantum well to the topside contact.

	ELO DBRTD		Baseline DBRTD	
Parameters	**Forward Bias**	**Reverse Bias**	**Forward Bias**	**Reverse Bias**
Peak Voltage, V_p	0.97± 0.03	0.81 ± .03	0.72 ± .07	0.64 ± .06
V_p - V_v, ΔV	0.11 ± .02	0.13 ± .03	0.3 ± .06	0.26 ± .05
Peak Current Density J_p (kA/cm^2)	45 ± 6	42 ± 5.5	52.1 ± 4.7	51.3 ± 4.4
J_p - J_v, ΔJ	27.4 ± 4.7	28.9 ± 4.3	38.6 ± 4.6	39.3 ± 4.5
Peak-to-Valley Current Ratio	2.6 ± 0.17	3.2 ± 0.22	3.9 ± 0.4	4.3 ± 0.5

Table 6.1: Characteristic J-V data for the ELO DBRTD (MBE Run# 1043) and a standard baseline DBRTD. Note the higher peak voltage, lower ΔV, lower ΔJ, and lower PVCR of the ELO DBRTD.

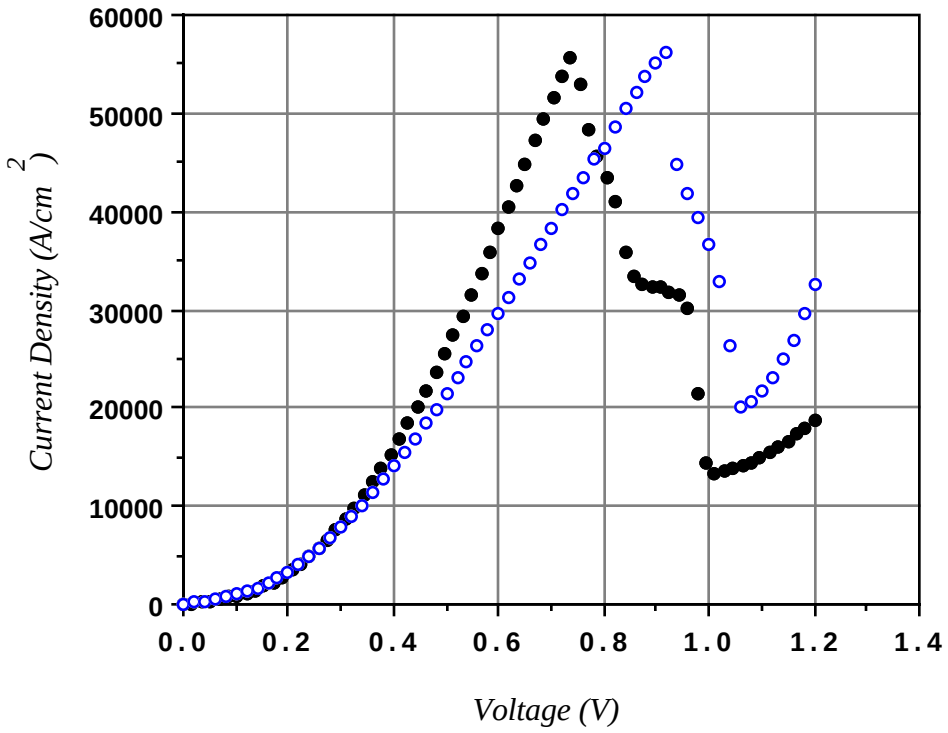

Figure 6.2: Typical forward bias J-V characteristics for the ELO DBRTD and a baseline DBRTD. The closed circles are the measurements taken for a baseline AlAs/GaAs DBRTD and the open circles are the measurements taken for an ELO AlAs/GaAs DBRTD. Note in the J-V characteristic of the ELO DBRTD on In/AuCr/glass that the valley current profile the ELO DBRTD rises faster and the PVCR and the ΔV are reduced.

As is evident from Figure 6.2, the ELO DBRTD exhibited NDR with J-V characteristics comparable to the baseline DBRTDs. Slight degradations in the key electrical parameters (PVCR, ΔV, and ΔJ) of the ELO DBRTD may be attributed to a poor backside ohmic contact and the observed faster rise in its valley current. As stated earlier, the valley current is a function of the temperature dependent inelastic tunneling that occurs in AlAs/GaAs DBRTDs. The possible rise in temperature may be due to the fact that the ELO DBRTD was mounted on a metallized glass substrate, which actually produces a higher thermal resistance than the n^+ GaAs substrate of the baseline DBRTDs. Although the specific contact resistivity of the backside ohmic

contacts cannot be determined directly from these structures, it has been approximated indirectly from a program which can extract current density-electric field, J-E, curves from measured DC-IV characteristics [*Mil90*] . Since the σ of the quantum well is known, as well as the doping concentrations and layer thicknesses, one can approximate the specific contact resistivity of the backside ohmic contact. Using this program, the specific contact resistivity of the backside contact was 8 $x10^{-6}$ Ω-cm^2. Although the electrical contact to the device was satisfactory, the mechanical and thermal contact to the substrate were quite poor. As with all thin films, it is difficult to quantitatively evaluate the amount of adhesion between the ELO film and its substrate. A primitive test is to use a "Scotch" tape test. The ELO DBRTDs on In did not survive the tape tests. In fact, as shown in Figure 6.3, since mechanical contact to the substrate was poor, it is probable that the thermal contact was also poor resulting in a higher thermal resistance between the substrate and the device.

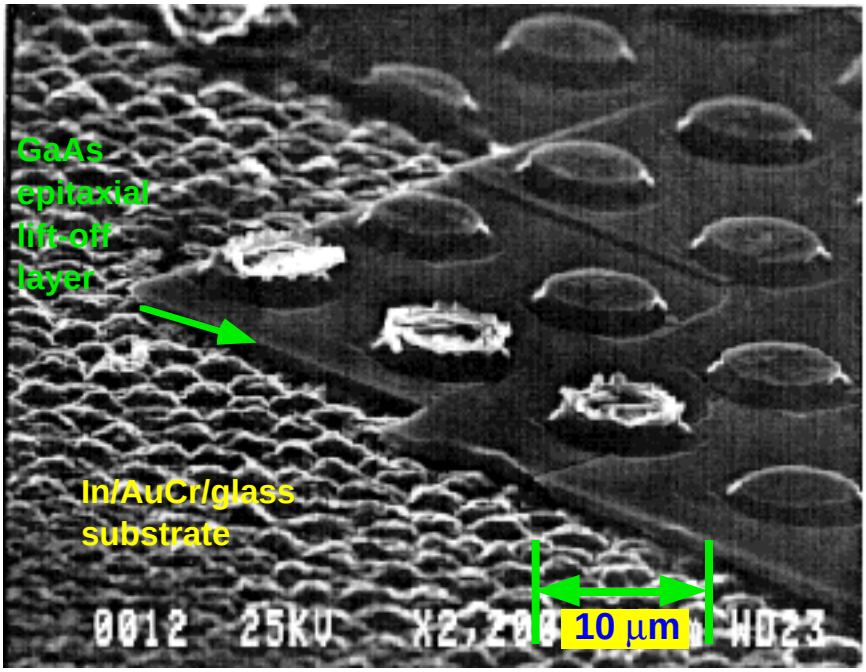

Figure 6.3: SEM micrograph of an ELO device bonded to an In/AuCr coated glass substrate after an anneal at 350°C. Note the roughness of the In at the edges of the ELO film. This type of bond did not survive a "Scotch" tape test.

Thus, from this initial experiment, it was found that possible improvements could be made on these ELO DBRTDs if an alternative substrate of higher thermal conductivity was used. In addition, a better mechanical and thermal bond are required for better reliability and thermal contact to the substrate. Furthermore, improved lower specific contact resistivities are needed to remove parasitic series resistance in the device measurements which reduce ΔV. Note that the extracted backside specific contact resistivities presented on the previous page for the In-based backside contacts and the other ohmic backside contacts to be presented later represent the best possible or a lower limit on the backside specific contact resistivity. The choice of alternative substrates for the AlAs/GaAs DBRTDs is made based not only on their thermal conductivities, but also on their pre-existing surface smoothness, whether they are optically smooth and are amenable to VDW bonding. Therefore, an attempt was made to bond a similar ELO DBRTD to a Si substrate coated with the same In/AuCr metallization to provide an ohmic contact to the backside of the ELO layer. Similar results were observed on an another ELO AlAs/GaAs DBRTD (MBE Run# 1376). This DBRTD utilizes the same structure seen in Figure 6.1 except that the substrate is n+ GaAs and there is now a 500Å AlAs release layer that is very heavily doped n-type. With such an arrangement, the ELO DBRTD can be tested both before and after ELO so that the effects of the integration of the ELO AlAs/GaAs DBRTD to another substrate can be observed. The J-V characteristics for this DBRTD before and after ELO are summarized in Table 6.2.

	BEFORE ELO MBE Run # 1376		AFTER ELO MBE Run # 1376	
Parameters	**Forward Bias**	**Reverse Bias**	**Forward Bias**	**Reverse Bias**
Peak Voltage, V_p	0.76 ± 0.02	-0.65 ± 0.02	0.98 ± 0.05	-0.82 ± 0.03
V_p - V_v, ΔV	0.24 ± 0.01	-0.23 ± 0.02	0.08 ± 0.03	-0.07 ± 0.03
Peak Current Density J_p (kA/cm^2)	63.3 ± 3.0	-57.7 ± 2.6	57.2 ± 5.4	-50.7 ± 4.4
Valley Current Density, J_v	15.9 ± 1.7	-12.8 ± 0.6	19.0 ± 2.1	-14.4 ± 1.3
Peak-to-Valley Current Ratio	4.0 ± 0.3	4.5 ± 0.2	3.0 ± 0.1	3.5 ± 0.03

Table 6.2: Characteristic J-V data for an AlAs/GaAs DBRTD (MBE Run# 1376) both before and after ELO. Again note the higher peak voltage, lower ΔV, lower ΔJ, and lower PVCR of the ELO DBRTD. Although the device was bonded to Si, a reduction in the valley current density was not seen. As shown in Figure 6.3, it is believed that the mechanical and thermal contact to the backside of the ELO DBRTD did not provide an improvement over the original substrate.

From the data in Table 6.2, it was observed that bonding an ELO DBRTD to an In/AuCr coated Si substrate, with its higher thermal conductivity and smoother optical polish, still did not provide an adequate mechanical, thermal, or electrical ohmic contact to the new substrate. Again, as in the previous sample mentioned earlier (MBE Run# 1043), the valley current density was higher and the ΔV and the PVCR were reduced. Assuming a σ of 0.3 (1/Ω-cm) for the quantum well, the extracted specific contact resistivity of the backside contact is 9.5×10^{-6} Ω-cm^2. Furthermore, this type of bond did not survive a simple "Scotch" tape test. As a result of the unsatisfactory bonds to various In coated substrates, an alternative bonding medium was required that could provide both a better ohmic contact to the backside of an ELO device and an improved mechanical bond to the alternative substrate. The

previously mentioned silver epoxies in Chapter 3 did not provide reasonable ohmic contacts and required long cure times at temperatures near the softening point of the Apiezon W black wax.

6.3 Epitaxial Lift Off of AlAs/GaAs QWITTs and Integration with Alternative Substrates using Pd-based Bonds

An improved bonding method to alternative substrates, as discussed in Chapter 3, section 3.7, incorporates Pd as the bonding medium [*YaS91*] . Although these bonds provide very good mechanical bonds to the alternative substrates, the electrical ohmic contacts quoted were not impressive. In an effort to test these bonds to alternative substrates, several AlAs/GaAs QWITT structures with n+ AlAs release layers were grown on n+ GaAs substrates and processed based on the standard process flows described in Chapters 3 and 4.

The first device structure described here is an ELO AlAs/GaAs DEM-QWITT. The J-V characteristics of this device, before ELO, have already been described in Chapter 4, section 4.10. Since the AlAs release layer is very heavily doped n-type, measurements could be taken before ELO. A cross-sectional layer structure of this device is shown in Figure 4.12. After complete device characterization, the samples were separated from the GaAs substrate and bonded to a Pd/AuCr coated Si substrate. During the vacuum bag bonding procedure, as described in Chapter 3, section 3.6 and 3.7, the pressure was maintained at 15 lb/in^2 and the temperature was kept at 50°C overnight. Upon removal of the Apiezon W black wax, the device was tested again with the following J-V characteristics summarized in Table 6.3. No alloy was attempted initially to improve the backside ohmic contacts.

	BEFORE ELO MBE Run # 2028		**AFTER ELO MBE Run # 2028**	
Parameters	**Forward Bias**	**Reverse Bias**	**Forward Bias**	**Reverse Bias**
Peak Voltage, V_p	1.01 ± 0.04	-7.5 ± 0.41	1.2 ± 0.05	-6.7 ± 0.7
V_p - V_v, ΔV	0.20 ± 0.00	-4.9 ± 0.36	0.17 ± 0.04	-3.0 ± 0.6
Peak Current Density J_p (kA/cm^2)	21.4 ± 0.8	-14.1 ± 1.2	21.6 ± 0.6	-13.9 ± 0.4
Valley Current Density, J_v	14.3 ± 0.8	-6.5 ± 0.6	13.5 ± 0.4	-4.6 ± 0.1
Peak-to-Valley Current Ratio	1.5 ± 0.1	2.2 ± 0.3	1.6 ± 0.01	3.0 ± 0.1

Table 6.3: Characteristic J-V data for an AlAs/GaAs DEM-QWITT (MBE Run# 2028) both before and after ELO. Note that the PVCR is actually higher and the valley current lower after ELO, in both bias modes. The ΔV has decreased after ELO, indicating that the backside ohmic contact has an overall higher series resistance.

A schematic showing a typical mesa isolated ELO device bonded to Pd/AuCr coated Si substrate is shown in Figure 6.4.

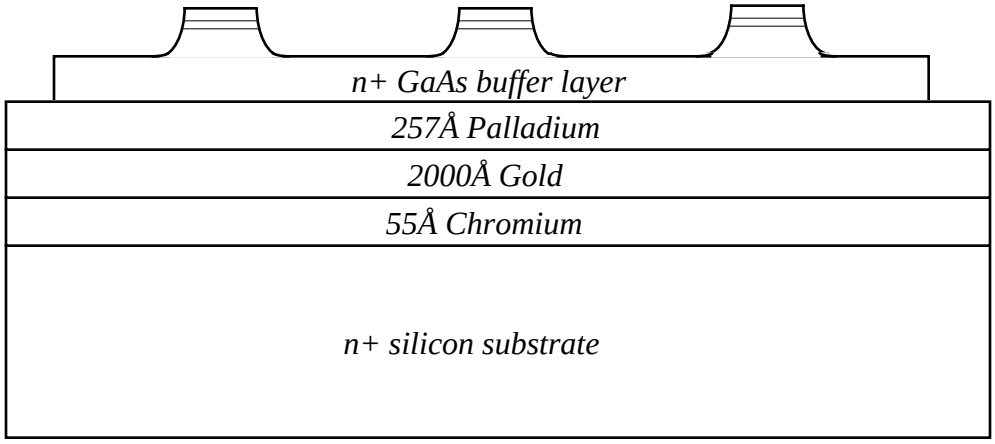

Figure 6.4: Illustration showing a mesa isolated ELO DBRTD or QWITT bonded to a Pd/AuCr coated silicon substrate. This bond is initially created using a vacuum bag/oven combination which provides the proper pressure/temperature combination to cause a solid phase reaction between the GaAs and Pd to form Pd_4GaAs.

The utilization of Pd as a bonding medium has allowed extremely reliable bonds with very good mechanical and thermal contact to the Si substrate. From the DC-IV characteristics, it was observed that the PVCR and J_V did not degrade and in fact improved slightly. From discussions of the temperature dependence of the valley current, in section 4.6, and inelastic tunneling, in section 4.4, it is possible that the AlAs/GaAs DEM-QWITT is operating at a slightly lower temperature and therefore exhibits a lower J_V and higher PVCR. The ΔV was reduced after ELO, possibly indicating that the contact resistance of the backside contact was higher than before ELO. This result is qualitatively consistent with the high specific contact resistance reported by Yablonovitch and co-workers using Pd bonds [*YaS91*]. The morphology of the edges of the ELO layer and Pd appear to be very clean, with no gaps or bumps at the interface, as shown in Figure 6.5.

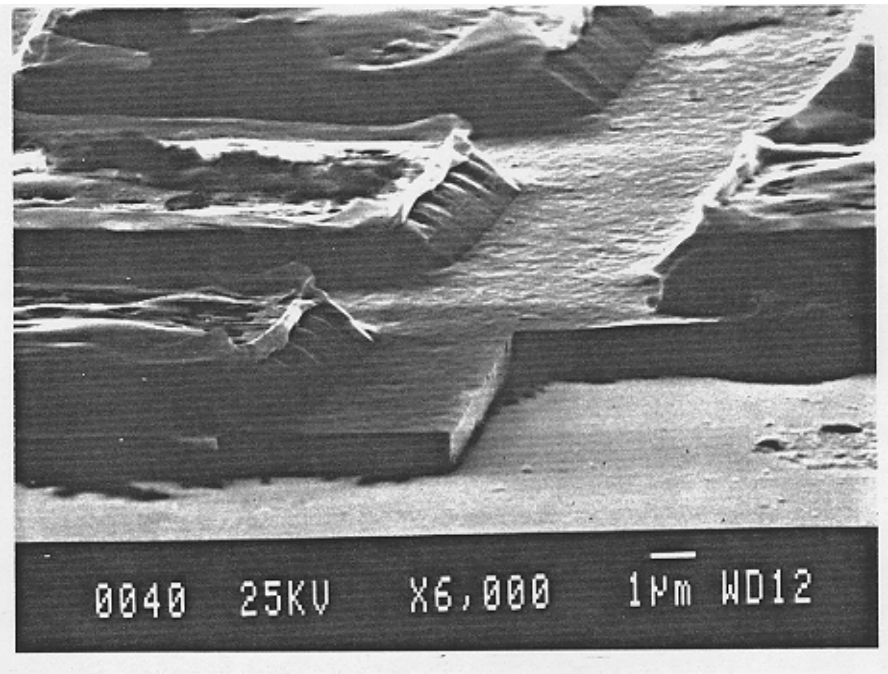

Figure 6.5: SEM micrograph of an ELO DEM-QWITT bonded to a Pd/AuCr coated n+ silicon substrate after an overnight bond in a vacuum bag. Note the smooth surface with no gaps, bumps or defects at the edges of the ELO film. This bond is much improved over the In based bonds in terms of bond strength and reduced defects.

The sample was alloyed at 350°C for 1 minute in forming gas to see if an improvement in the backside ohmic contact resistance would occur. After the alloy, no improvements electrically were found and in addition, there was some damage to the ELO film as some large bumps and cracks formed in the film. Once cracks form in the ELO film, there can be a tendency for the film to lift up from the surrogate substrate which can peel up additional areas of film, which will be discussed further in Section 6.4. A rough estimate of the backside specific contact resistivity, using the extraction program mentioned earlier, was found to be around 1.3 x 10^{-5} Ω-cm^2. This specific contact resistivity is slightly worse than those extracted using an In-based bond.

In an attempt to improve the backside ohmic contact resistance, the common PdGe recipes for normal topside ohmic contacts [*MaZ87*] [*YuW89*] [*WaL89*] are used in a second device structure. The second device structure described here is an ELO $Al_{0.3}Ga_{0.7}As$/AlAs/GaAs chair barrier QWITT (MBE Run# 1437). The J-V characteristics of this device, before ELO, have already been described in Chapter 5, section 5.4. A cross-sectional diagram of this device is given in Figure 5.9. After complete device characterization, the samples were separated from the substrate and bonded to a PdGe coated Si substrate as shown in Figure 6.6. Subsequently, the ELO device/bonding medium/substrate combination were alloyed at 300°C for 5 minutes in forming gas in an effort to create ohmic contacts to the backside. As in the previous sample, the high temperature step created a significant amount of bumps and cracks in the film. The origins of this type of defect are related to trapped gas around particles which may expand at high temperatures, which will be discussed further in Section 6.4.

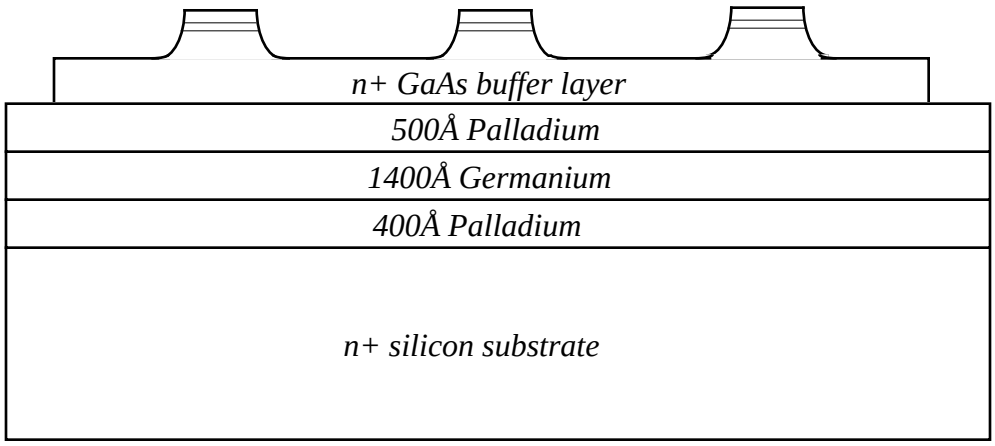

Figure 6.6: Illustration showing a mesa isolated ELO DBRTD or QWITT bonded to a typical Pd/Ge/Pd coated silicon substrate. This bond is created using a vacuum bag/oven combination, discussed in Chapter 3, which provides the proper pressure/temperature combination to cause a solid phase reaction between the GaAs and Pd to form Pd_4GaAs. Subsequently, the ELO film/Pd/Ge/Pd combination are alloyed at 300°C for 5 minutes in order to form an ohmic contact.

The results of the measured J-V characteristics before and after ELO are given in Table 6.4. From the data presented in Table 6.4, it is observed that the PVCR increased and the valley current density decreased. The ΔV was also observed to decrease which indicates that the Pd/Ge/Pd ohmic backside contacts after anneal still did not provide an adequate specific backside contact resistance. Several factors may have contributed to the poor backside specific contact resistance. The Pd/Ge/Pd metallization scheme was not tested as a topside ohmic contact to the mesa isolated DBRTDs or QWITTs and furthermore, no Cox-Strack specific contact resistance measurements were performed yet. Ideally, a vacuum system with a very low base pressure (in the 10^{-7} Torr range) is desired for this type of metallization since Ge is very reactive and can be oxygen contaminated from the alumina coated tungsten boats or a high base pressure.

	BEFORE ELO MBE Run # 1437		AFTER ELO MBE Run # 1437	
Parameters	**Forward Bias**	**Reverse Bias**	**Forward Bias**	**Reverse Bias**
Peak Voltage, V_p	0.61 ± 0.07	-2.71 ± 0.1	1.1 ± 0.18	-3.2 ± 0.1
V_p - V_v, ΔV	0.36 ± 0.05	-0.98 ± 0.09	0.07 ± 0.04	-0.54 ± 0.04
Peak Current Density J_p (kA/cm^2)	46.8 ± 1.5	-64.4 ± 1.9	46.3 ± 1.7	-60.1 ± 2.0
Valley Current Density, J_v	15.6 ± 0.3	-17.1 ± 0.4	14.2 ± 0.5	-14.5 ± 0.6
Peak-to-Valley Current Ratio	3.0 ± 0.1	3.8 ± 0.2	3.3 ± 0.1	4.1 ± 0.1

Table 6.4: Characteristic J-V data for an $Al_{0.3}Ga_{0.7}As$/AlAs/GaAs QWITT (MBE Run# 1437) both before and after ELO. Note that the PVCR is actually higher and the valley current lower after ELO, in both bias modes. The ΔV has decreased after ELO, indicating that the backside ohmic contact has an overall higher series resistance.

The evaporation system used in this study, named "Philvac", has a base pressure of only 3 x 10^{-6} Torr. Furthermore, the high backside contact resistance may also be related to the damage that occurred to the film during the alloy cycle. The extracted specific contact resistance of the backside ohmic contacts is approximated to be 1.2 x 10^{-5} Ω-cm^2. From this section, it is observed that no degradation in the PVCR and J_v were observed after ELO, but there was significant decrease in ΔV as a result of the higher backside ohmic contact resistance. In Figure 6.7, a comparison between the J-V curves of the ELO chair barrier QWITT before and after ELO is shown.

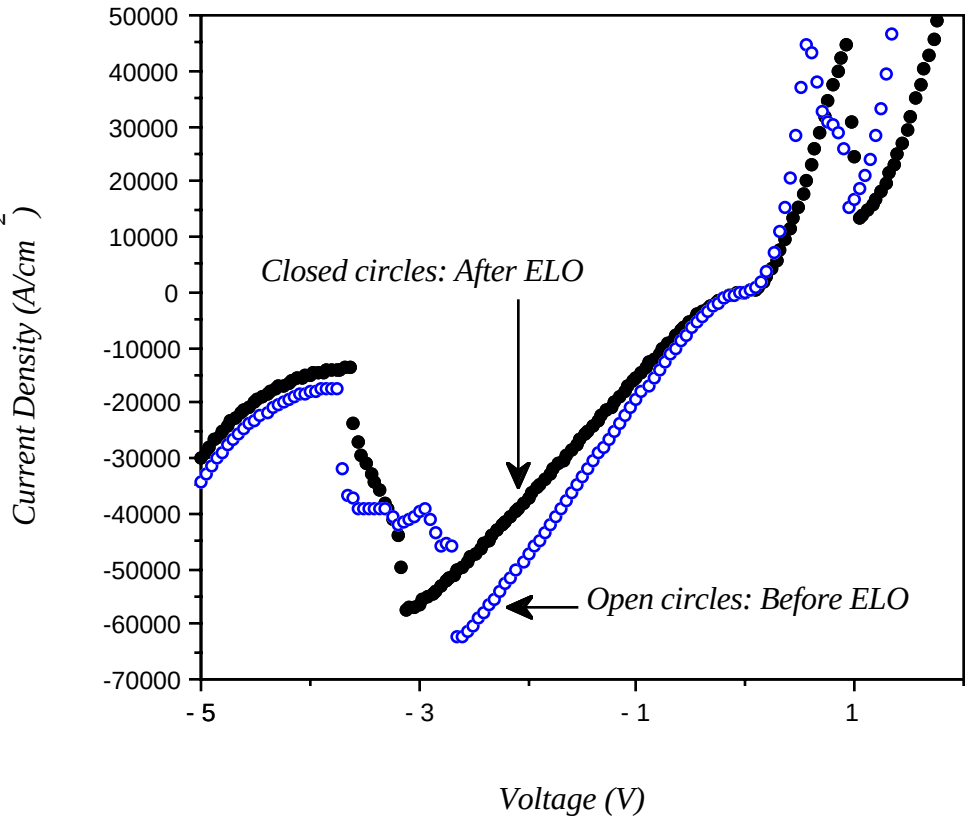

Figure 6.7: Characteristic J-V data for the ELO Chair barrier QWITT before and after ELO. Note that the PVCR in both bias directions improved slightly with the only significant degradation in device characteristics occurring in the ΔV due to a higher backside contact resistance after ELO.

The samples described in this section and the previous section represent the first time, to the best of this author's knowledge, that AlAs/GaAs DBRTD or QWITT structures have been integrated with Si substrates. Other substrates have been investigated as possible surrogate substrates based on their thermal conductivities, as shown in Table 6.5.

Alternative Substrate Material	Thermal Conductivity, k, (Watts/°C-cm)
GaAs (n)	0.5
GaAs (n+)	0.4
Si (undoped)	1.45
Si (high doping)	1.15
Diamond IIa	22.0
Copper (OFHC)	4.0
Gold	3.16

Table 6.5: Thermal conductivities for various materials. Taken from B.S. Perlman [*Col76*] .

For cases of constant thermal conductivity and no internal heat generation, the appropriate form of the steady state heat conduction equation is Laplace's equation:

$$\left\{\frac{d^2T}{dx^2}+\frac{d^2T}{dy^2}+\frac{d^2T}{dz^2}\right\}=\nabla^2T=0 \tag{6.1}$$

The thermal conductivity is defined from Fourier's heat conduction equation, as shown in equation 6.2.

$$q_x=-kA\frac{dT}{dx} \tag{6.2}$$

where q_x is the rate at which heat is transferred per unit area by conduction (heat flux), k is the thermal conductivity, T is the temperature, and A is the area through which the heat is transferred. Simple solutions to these equations were used as a guide in determining the possible benefits of using a particular substrate and how much the thermal resistance could be reduced. Complex solutions, which were performed in this work, must take into account arbitrary shapes, the temperature dependent thermal conductivity of the materials used, the aluminum mole fraction dependent thermal conductivity of the $Al_xGa_{1-x}As$/GaAs layers [*Ada85*], internal heat generation, and the thermal contact resistance of the interfaces between the device and

its corresponding hybrid substrate. The thermal resistance, R_{th}, for a particular device can be determined in an analogous fashion to electrical resistance, which is defined as:

$$R_{th} = \frac{T_{\max} - T_a}{P_{diss}} \tag{6.3}$$

where R_{th} is the thermal resistance, T_{max} is the maximum temperature at the source of heat, T_a is the ambient temperature, and P_{diss} is the power generated from the device and is equal the rate of heat transfer. One way to reduce the thermal resistance is to thin the substrate as much as possible, for which the ELO method is ideal, and bond it to an alternative substrate of higher thermal conductivity.

It should be noted that ELO DBRTDs and QWITTs have been lifted from their original growth substrates and bonded to Pd coated copper substrates, which have higher thermal conductivities than silicon, but the resultant J-V characteristics were nominally worse in all parameters of interest. The cause of this degradation of all parameters may be due to the rough surface of the commercially purchased copper foil. Ideally, this copper foil should have been optically polished for the smoothest surface before an ELO bond was attempted. As a result, future work must include optically polishing the copper foil before ELO. Therefore the electrical measurements obtained thus far on copper substrates will not be presented.

6.4 Process Problems Associated with ELO DBRTDs and QWITTs

As already discussed in Chapter 3, sections 3.5-3.7 and Chapter 6, sections 6.2-6.3, achieving reliable bonds between the ELO devices and their surrogate substrates is one of the most difficult parts of the ELO process. Obtaining good backside ohmic contacts to the back of the ELO layers puts further restraints on this process. One of the major problems in obtaining good contact between the ELO device and its surrogate substrate is particulate contamination. Even in a DI-H_2O environment, complete removal of particulates is very difficult. Particulates on the order of $\leq 1\mu m$ can severely degrade the overall reliability of the bond between an ELO film and its surrogate substrate, as shown in Figure 6.8.

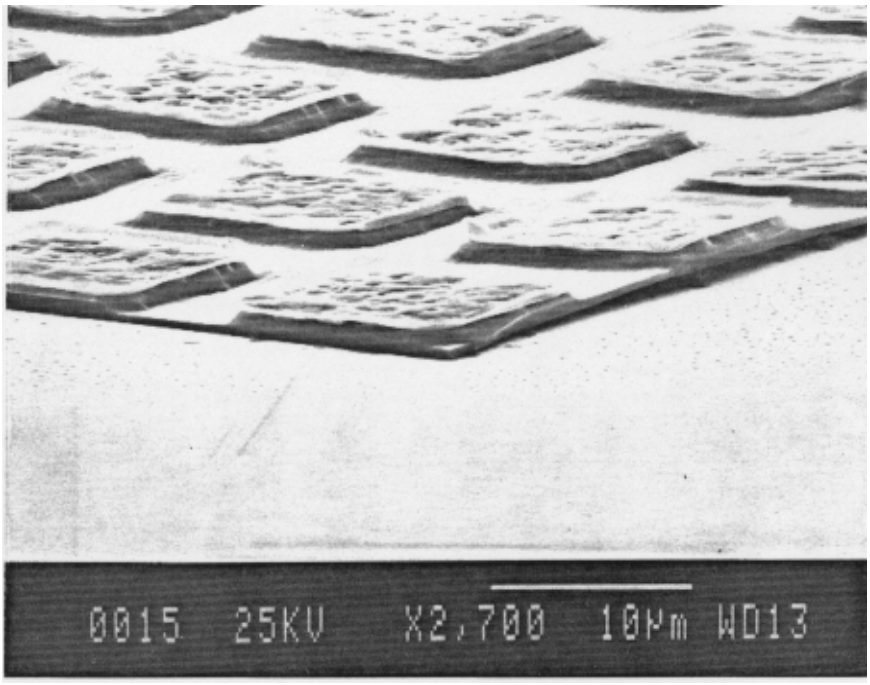

Figure 6.8: SEM micrograph of particles on the order of 1µm preventing a reliable bond at the edge of an ELO QWITT layer and its alternative silicon substrate.

To avoid particulate problems, cleaving the original growth substrate up to the edges of the Apiezon W black wax carrier before ELO will aid in preventing excessive amounts of the ELO film from extending beyond the mechanical support of the wax carrier and therefore preventing loose, broken pieces of the ELO film from re-adhering to the bottom of the ELO layer. Even in a DI-H_2O environment, these broken pieces of the ELO film can cause severe particulate contamination. A clean

room environment would also be ideal for performing the particle sensitive ELO bonding procedure. Other types of particulates can also trap gas bubbles. These bubbles prevent any formation of a VDW or metal/alloy bond. In addition, during the alloy stages of creating a metal/alloy bond, the particulates and/or bubbles tend to expand and burst causing pits or extremely small "craters", as shown in Figure 6.9.

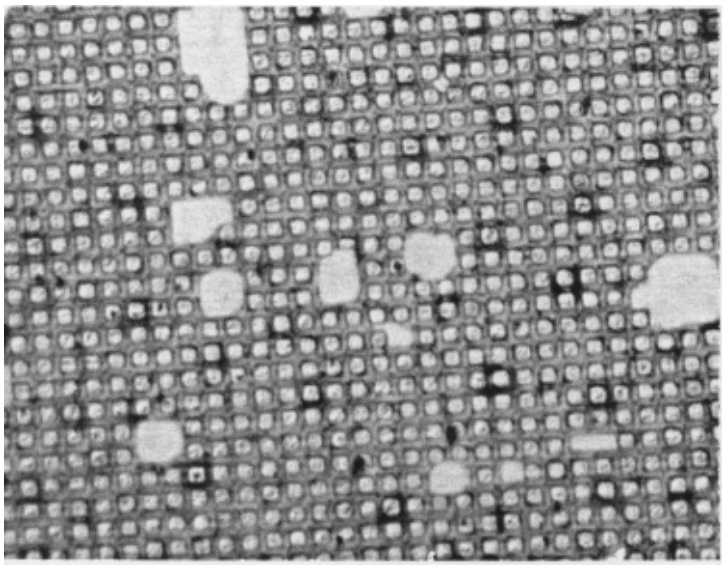

Figure 6.9: Photograph showing regions where there were very small bubbles that burst or broke upon rapid thermal annealing the backside ohmic contacts.

Preventing excessive bubble formation can be done through using the proper vacuum bag/oven temperature settings and proper substrate cleaning methods. The strong vacuum in the vacuum bag helps draw out both moisture and any trapped air that may be underneath the ELO film. While under vacuum, the vacuum bag/ELO sample combination can be placed in a Blue M Bake oven at slightly elevated temperatures. These raised temperatures initiate the solid phase reaction between the ELO film and the In-based or Pd-based bonding medium. Pressures of 15 lb/in^2 and oven temperatures of 50°C for one overnight period have been found to work very well in preventing bubble formation during ELO bonding to In-based or Pd-based bonding mediums. Pre-existing cracks in the ELO films, due to damage that can occur to an ELO film if it is not suspended or anchored after it has separated from its original substrate, can also result in poor bonds to the alternative substrate, as shown in Figure 6.10.

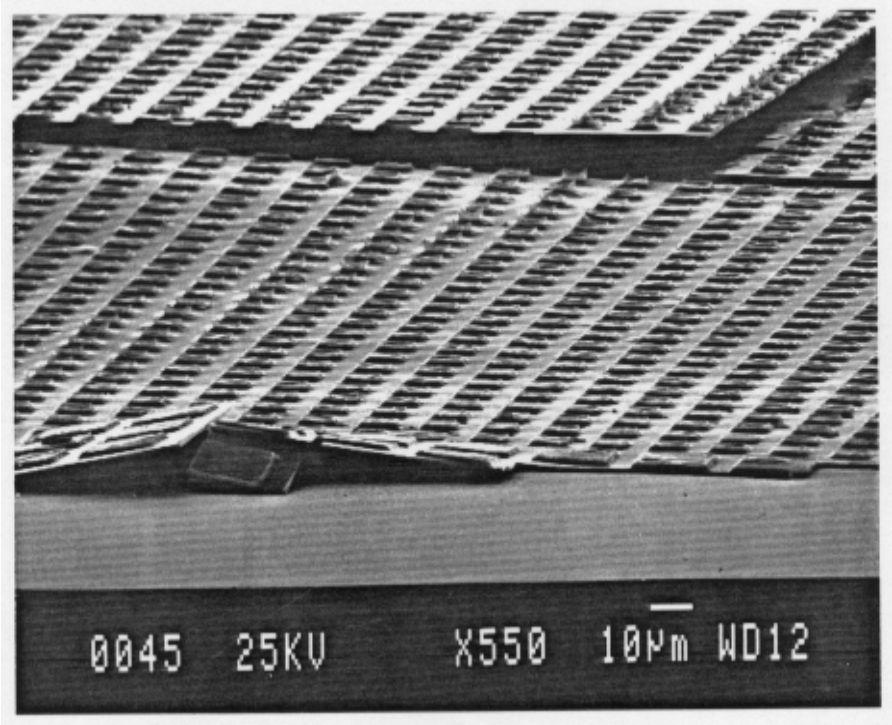

Figure 6.10: SEM micrograph of cracks that formed in an ELO DEM-QWITT and its subsequent release from the surrogate substrate.

Specific to the DBRTDs and QWITTs, it is very important to apply the Apiezon W black wax properly over the mesa isolated devices since the AlAs barriers of the quantum wells can also get attacked by the 10% HF during the lift off procedure. In Figure 6.11, a DBRTD at the edge of the ELO film was not properly protected with Apiezon W black wax.

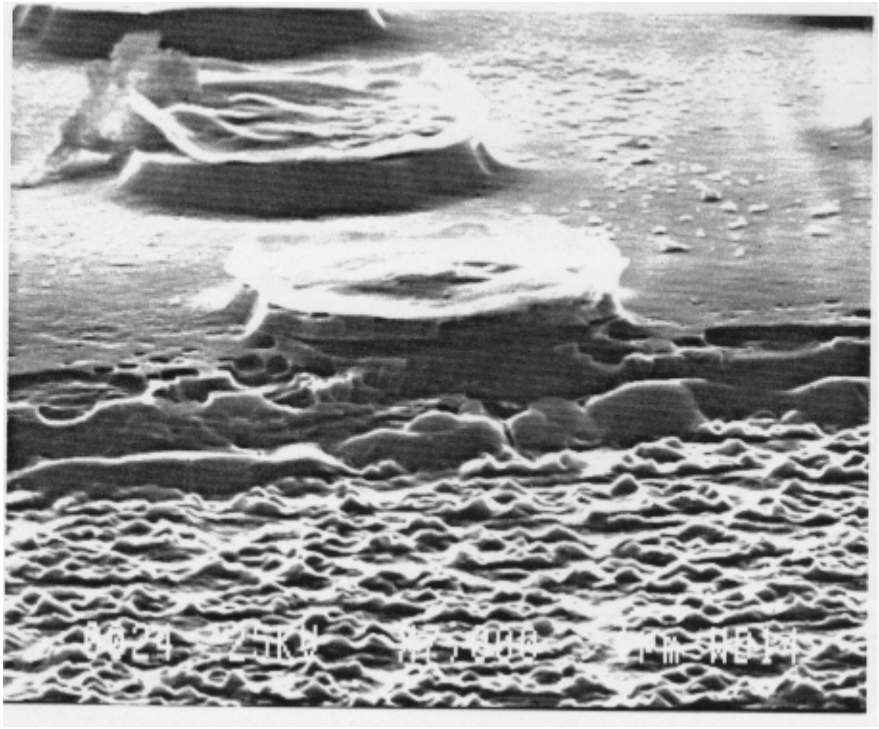

Figure 6.11: SEM micrograph showing the peeling up of the top half of an AlAs/GaAs DBRTD, above the quantum well, which was not covered properly with Apiezon W black wax during the lift off in 10% HF.

6.5 Epitaxial Lift Off of an Optically Controlled Schottky Contacted Coplanar Waveguide (CPW) Phase Shifter and Bonds to Transparent Substrates

The purpose of this section is to show the significant improvement in the performance of a Schottky-contacted coplanar waveguide (CPW) structure as a result of using the ELO method. Device fabrication and testing of this device is performed by M. Saiful Islam [*Isl93*] with the ELO fabrication methods performed by this author. The ELO Schottky-contacted CPW phase shifter is a device that allows microwave signals to be carried along its length which undergo large phase shifts due to optically controlling the RC shunt admittance of the transmission line. The Schottky contacts are heavily reverse biased until the lightly n-type doped epi film is almost fully depleted, as shown in Figure 6.12. For the layer thicknesses shown in Figure 6.12, reverse biases of about 20 V are needed to fully deplete the epi-layer. At these voltage biases, small amounts of illumination can cause significant changes in the admittance of the device structure. For this optically sensitive device to be useful, the metallization must be made very thick to avoid any losses. If the optical illumination is incident from the top of the sample, it is apparent that the thick metallization shadows or blocks the majority of the illumination. Typical parameters of interest for this type of device are the insertion loss, the optically induced phase shift, and most importantly, the loss per degree of phase shift or the "loss figure".

In the fabrication of this devices [*Isl93*], the metallization pattern is laid down on the epitaxial GaAs/semi-insulating GaAs substrate using a photoresist/polyimide lift off process. Since the metallization is extremely thick, the photoresist profile is very important where a reverse gradient in the profile is desired. Unfortunately, this profile does not always occur and therefore 1μm tall metal flags remain after the photoresist has been removed. These flags can break and sometimes short out the r.f. signal line to r.f. ground. In the ELO process, the application of the Apiezon W black wax apparently helps remove these flags, many times improving the device yield after ELO compared to the yield before ELO.

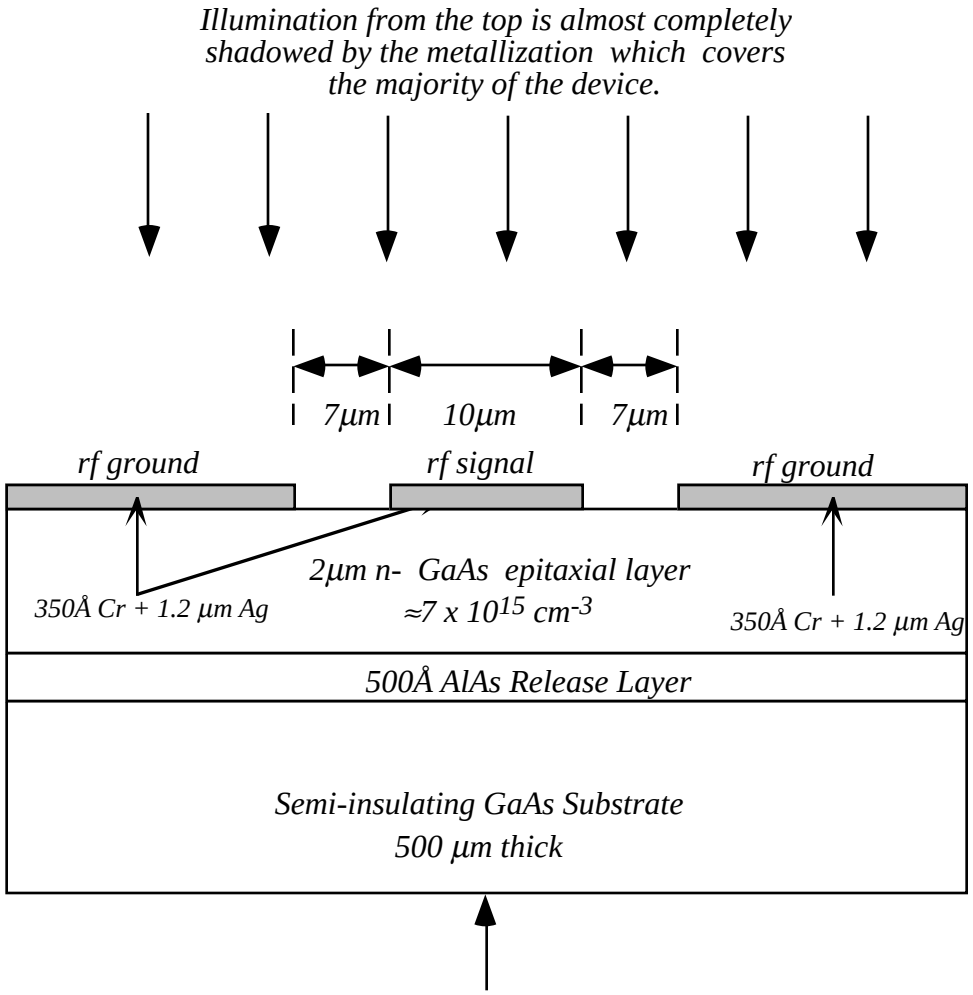

Figure 6.12: Illustration depicting a typical Schottky contacted CPW phase shifter before ELO. Note all device processing and testing performed by M. Saiful Islam. The ELO processing of this device is performed by this author.

Since these devices are fairly large, typical dimensions of the ELO films for these devices are about 0.8 inches by 0.5 inches. Films as large as 1 inch by 1 inch have been separated from their substrate. The ELO process, as applied to the ELO CPWs, follows the process described in Chapter 3 with some minor variations to the process. First, since these device structures are very large, the time for complete separation from the GaAs substrate may be realistically as long as 64 hours due to bubble

formation, indium on the edges of the chip, and improper tension in the wax carrier. Once separated from the substrate, the ELO film is quite sturdy due to the thick topside metallization. These ELO CPWs are usually bonded by VDW bonds or cyanoacrylates to clear fused quartz slides with dimensions of 1.5 inches by 0.75 inches. If VDW bonds are used, then the ELO film's manipulation and bonding all occur under DI-H_2O which is the cleanest environment that was available. If adhesives such as cyanoacrylates or UV curable epoxies are used, then the film manipulation and bonding are performed in a fume hood. The bond line of the cyanoacrylates is very thin and uniform and offer a very good bond to the transparent quartz slides. During the bonding stage of these ELO CPWs, attention must be paid to the thick topside metallization which occasionally extends beyond the wax carrier's periphery. Since the topside metallization is very flexible, it has a tendency to wrap around the bottom of the wax carrier during VDW or cyanoacrylate bonding. The best way to avoid this problem is to cleave the sample/substrate to the edges of the Apiezon black wax carrier on all sides such that this topside metallization does not become a problem. Furthermore, excessive amounts of cyanoacrylates should be avoided since any extra cyanoacrylate that gets pushed out from underneath the sample during vacuum bag bonding will spread onto the top of the wax carrier. Cyanoacrylate on top of the wax carrier prevents subsequent removal of the black wax with TCA. Although acetone can remove the cyanoacrylate, it can also degrade the backside bond of the ELO film to the quartz slide at the edges. The use of cyanoacrylates over VDW bonds has allowed the freedom to work in a non-cleanroom environment and given much more reliable bonds to transparent substrates. A typical schematic of an ELO CPW after ELO is shown in Figure 6.13. Once the ELO CPW has been bonded to the quartz slide, the sample is now on a transparent substrate as well as a substrate of lower dielectric constant. GaAs has a relative dielectric constant of $\varepsilon_r = 13$ whereas quartz has a relative dielectric constant of $\varepsilon_r = 3.8$ [*Bal89*] . Through the use of a transparent surrogate substrate, greater optical control of the ELO CPW can be obtained now that optical contact to the backside of the fully depleted n- GaAs epi-layer can be obtained. Optical illumination of the device can be done by either a light emitting diode or semiconductor laser diode operating at $\approx$ 800nm.

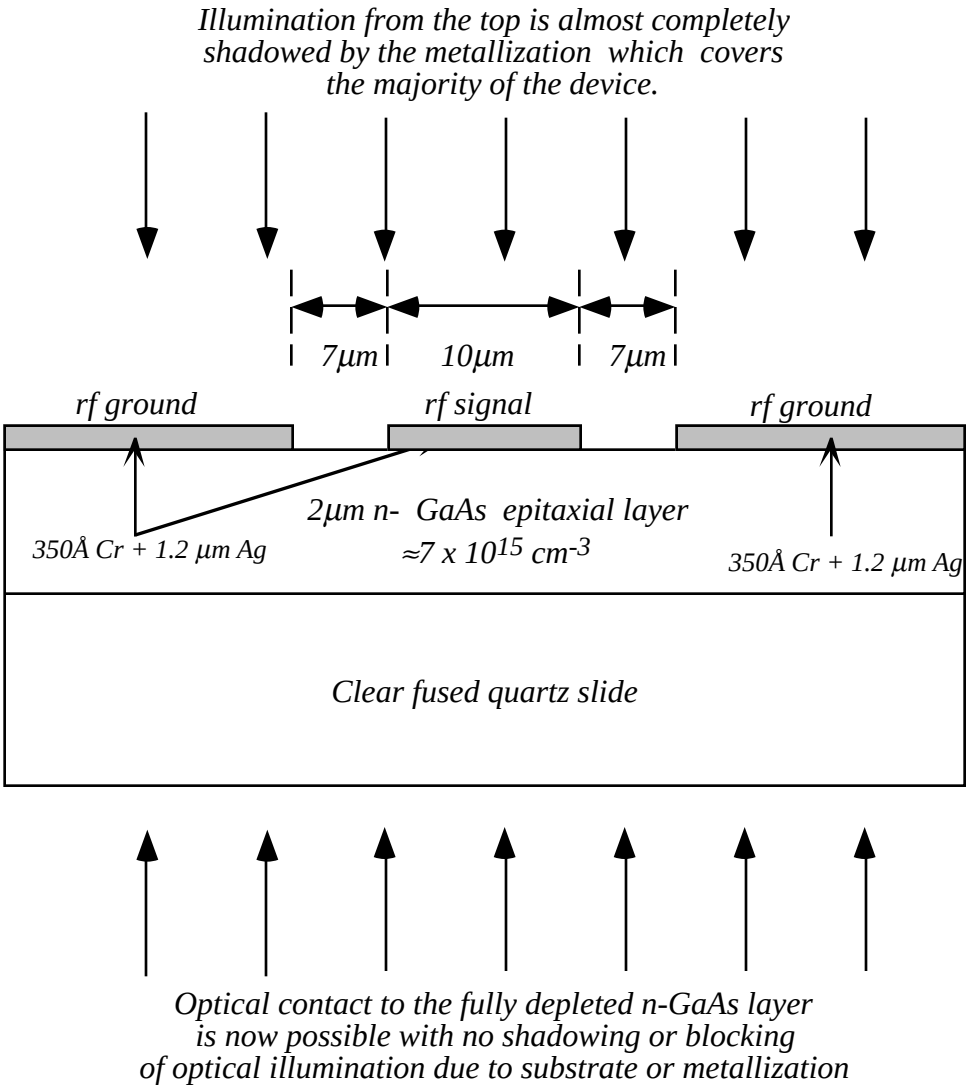

Figure 6.13: Illustration showing the ELO CPW bonded to a clear fused quartz slide using either cyanoacrylates or VDW bonds.

The following data [*Isl93*] is taken for an ELO CPW using a semiconductor laser diode operating at 809nm with an optical intensity of 0.65 mW/cm^2.

	Before ELO, illumination from the topside.	After ELO, illumination from the topside.	After ELO, illumination from the backside.
Phase shift (°/cm) at 30 GHz	45°	250°	350°
Insertion Loss (dB/cm) at 30 GHz	-15	-25	-40
Approximate Loss Figure (dB/degree) at 30 GHz	-1.0	-0.1	-0.1

Table 6.6: Measurement taken on an ELO CPW before and after ELO. The measurements were taken by M. S. Islam [*IsT91*] .

The ELO CPW has achieved the best loss figures of ≈-0.1 dB per degree of phase shift for any optically controlled phase shifter. In the ELO CPW, it is observed that not only was an ELO device integrated with a surrogate substrate with certain desired characteristics, but the performance of the ELO device improved dramatically as a direct result of ELO. Improvements in a similar ELO device, an ELO GaAs Schottky photodiode [*KoS92*] , were reported after this work [*IsT91*] was already published. Another group has also used ELO to obtain significant improvements in the quantum efficiency of AlGaAs/GaAs/AlGaAs double heterostructures by placing these heterostructures on substrates of higher reflectivity [*ScY93*] .

In an effort to fully integrate an optically controlled Schottky contacted CPW with its light source, an attempt was made to perform a back-to-back integration of an ELO CPW and ELO light emitting diode (LED) with a clear quartz slide in between the two devices as shown in Figure 6.14.

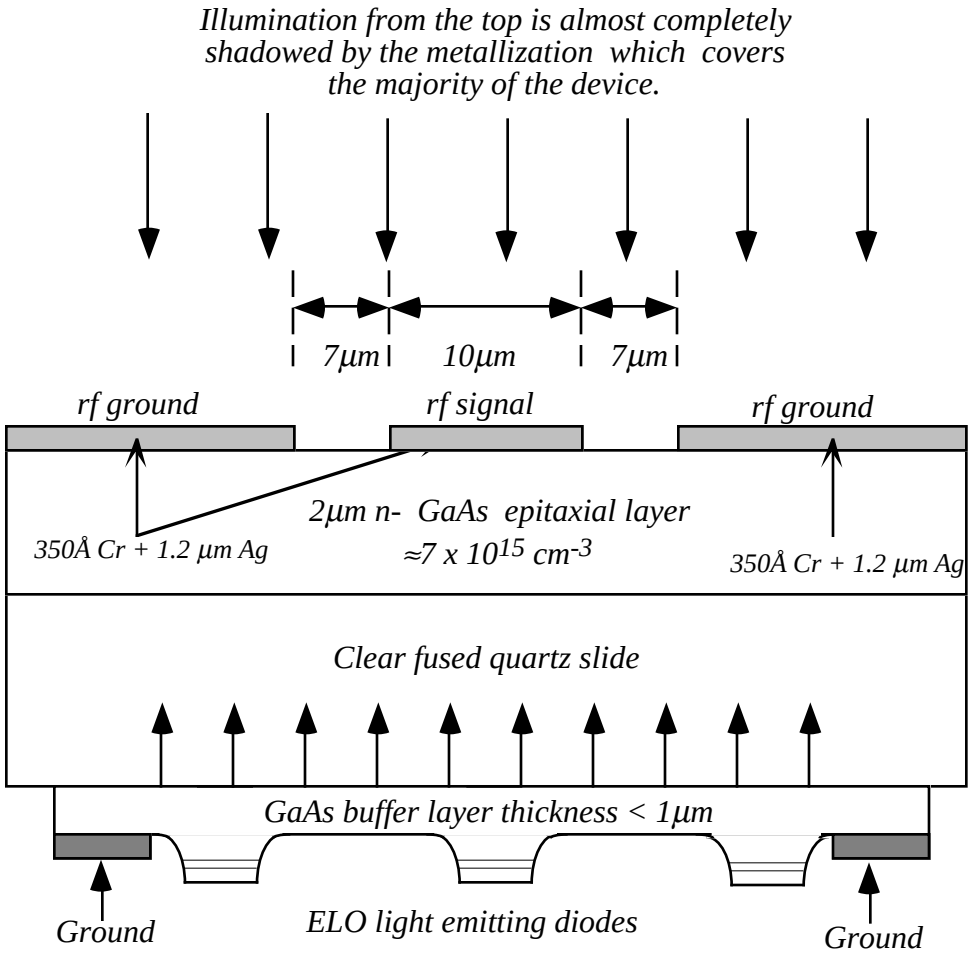

Figure 6.14: Hybrid back-to-back bonding of an ELO CPW and an ELO double heterostructure LED or multi-quantum well (MQW) LED. Both the ELO CPW and ELO LED are bonded to the surrogate quartz substrate with cyanoacrylate.

Several double heterostructure and multiquantum well (MQW) LEDs were grown by MBE and processed using a stripe mask for use as an integrated source of optical illumination for the ELO CPW. The designs and layer structures used for the double heterostructure LEDs follow those taken from the literature [*PoD90*] [*PoA90*] . The use of ELO on LEDs has been shown to produce significant improvement in output power by using a back reflector once the GaAs substrate has been removed [*PoA90*]. A typical cross-section of an ELO MQW LED grown in this study is shown in Figure 6.15.

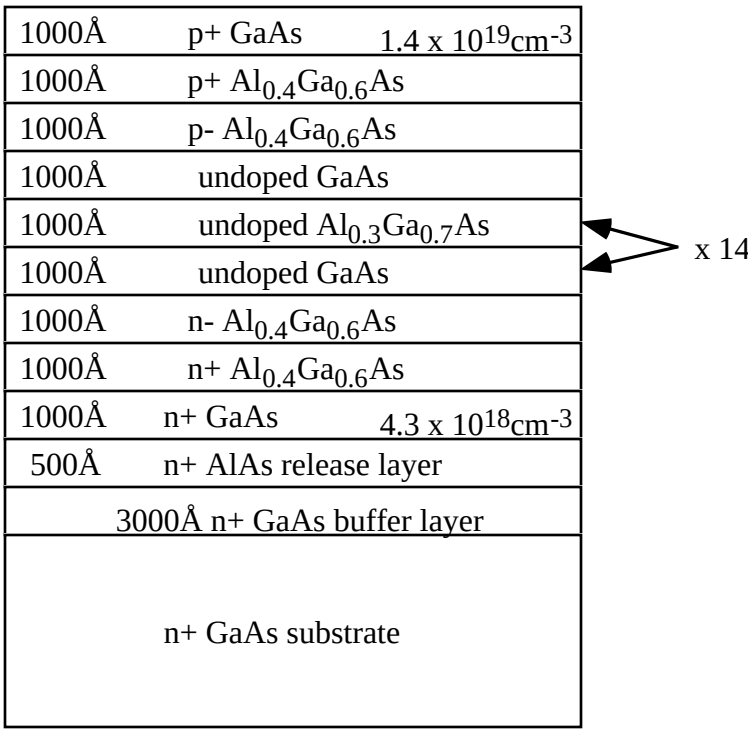

Figure 6.15: Illustration showing a typical MQW LED type structure designed for emission of light with a wavelength of ≈ 750nm using software written by T.R. Block.

Since a planarized LED was not possible due to the inavailability of a proper mask set, a single layer stripe mask or dot mask was used to pattern the topside contacts which consisted of 50Å Cr and 1000Å Au. Subsequently, the device was mesa isolated and then a ground contact (Ni/AuGe/Ni/Au) was made to the n+ GaAs buffer layer. Once the device was completely processed, it was separated from its substrate using the ELO method, as described above for the ELO CPW and in Chapter 3, and bonded to a clear fused quartz slide with cyanoacrylate. Upon testing this device, it was observed that minimal light was emitted from the backside or the edges. A possible explanation for this poor performance is due to the fact that these devices were grown by MBE during a time when there were a significant number of oval defects generated in these film. Furthermore, a planarized mask set for these devices

would have simplified the processing of these type of devices. With the above process, the alloy of Ni/AuGe/Ni/Au contacts had to occur after the AuCr stripes or dots were patterned. The alloy subsequently caused the stripes or dots to ball up. Mesa isolation may also not have been desired due to the high surface recombination velocity at the exposed edges of the mesas, but without a planarized mask, this step cannot be removed.

6.6 Future Work Involving Hybrid Integration of ELO Devices

A great majority of the possible ELO integration schemes could have been simplified if planarized processes were used where all external contacts are on the topside. For example, bonding ELO DBRTDs and QWITTs to substrates of higher thermal conductivity would be much simpler if the requirement of a good electrical ohmic contact were lifted and only the requirements of a good mechanical and thermal contact to the substrate were essential. Thus, the need for a special metallization or bonding medium that forms an ohmic contact to GaAs is not needed. Planarization of DBRTDs and QWITTs would allow the possible use of solventless, high thermal conductivity epoxies which contain no silver flakes dispersed within the epoxy. A four level planarized mask set has been designed for the DBRTDs and QWITTs which utilizes air-bridge isolation instead of dielectric isolation [*Jav91*] , as shown in Figure 6.16. By inserting a highly resistive, low temperature (LT) GaAs layer between the active device layers of a standard ELO AlAs/GaAs DBRTD or QWITT and the AlAs release layer, one can obtain electrical isolation between the active device layers and the alternative substrate after ELO. A few difficulties with this mask set are still being worked out and therefore this process has not be attempted yet. As this process is developed, a structure similar to the one shown in Figure 6.16 will allow the opportunity to integrate planarized DBRTDs and QWITTs to alternative substrates without any concern of obtaining an electrical ohmic contact to the backside of the ELO layers.

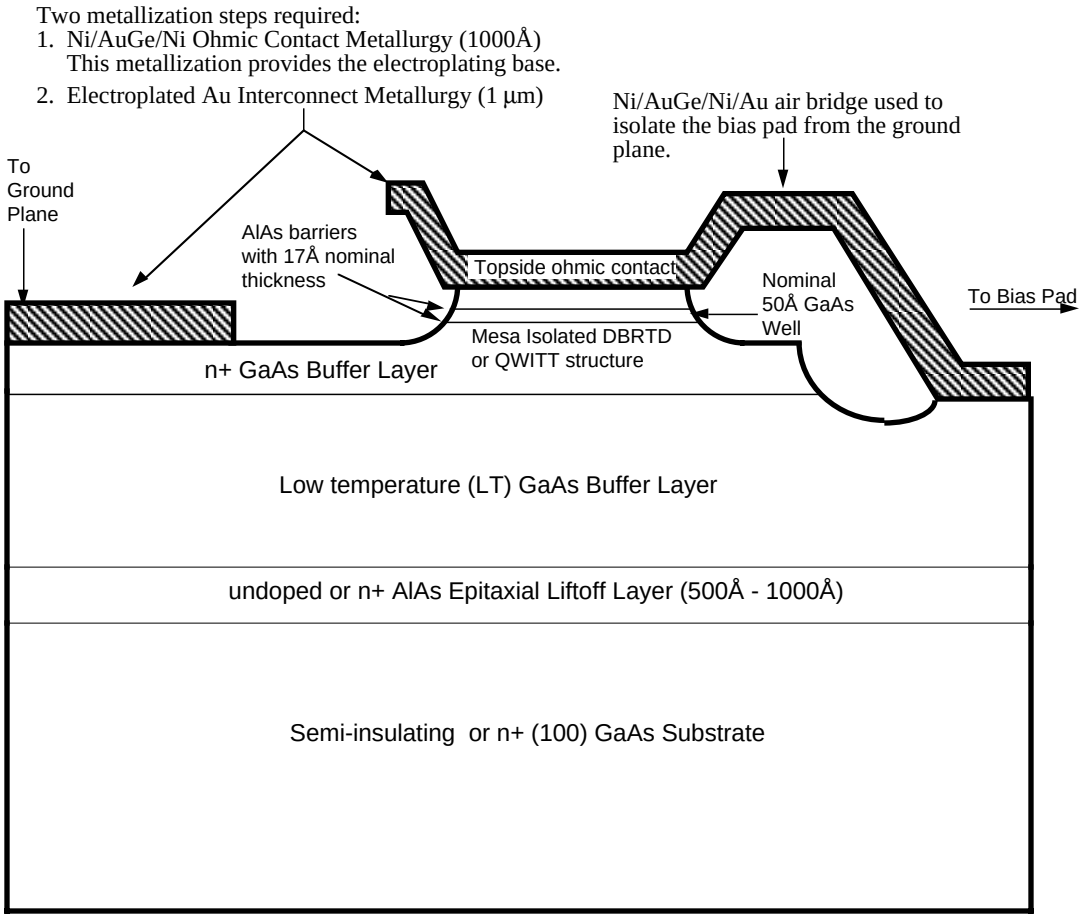

Figure 6.16: Illustration showing the planarized ELO DBRTD or QWITT utilizing an air-bridge for device isolation and an LT-GaAs layer for backside isolation.

In a similar manner, a planarized process for the LEDs used in this study would allow fabrication of device structures that have large pads that can be bonded to an external carrier using a wire bonder. With the ELO LED mounted on the external carrier, an ELO CPW can easily be integrated to the back of the LED's quartz substrate. This would allow easy external control of the ELO LED as it is used to optically control the ELO CPW.

Further work should be continued in the area of bonding ELO double heterostructure LEDs or MQW structures to pre-patterned substrates. Preliminary work has been performed where AlGaAs/GaAs double heterostructures and MQW

heterostructures have been patterned with stripes, separated from their substrates using ELO, and then bonded to pre-patterned silicon and copper substrates coated with Pd. These pre-patterned substrates are etched down ≥ 5μm with straight edges. After evaporating Pd on these pre-patterned substrates, the ELO stripe patterns are aligned orthogonally to the edge of the patterns in the substrate and bonded. Once placed in the vacuum bag for overnight bonding, the temperature in the oven is raised above the softening point of the Apiezon W black wax carrier. The pressure from the vacuum bag causes the film to bend over the edge of the pattern. Upon removing the black wax with TCA, it is found that the stripes are cleaved over the patterned edge of the surrogate substrate. Thus, this method may be applied to formed cleaved facets for stripe lasers with pre-defined lengths as specified by the patterns etched in the surrogate substrates. This method provides a simpler method of cleaving stripe lasers than the wedge-induced facet cleaving (WFC) method [*PoB91*] .