Chapter 1

Introduction

The solenoid type of inductor in free space exemplifies a high performance structure in terms of magnetic field point of view. However, it has been very difficult to create a solenoid type inductor on silicon until recently. The thick, high vertical aspect-ratio metallic structure required for an integrated solenoid is limited by thin metallization available in most very large scale integration (VLSI) technology. Some duct-shaped solenoid micromachined inductors have been reported [1][2]; however, these types of inductors are not effective in common IC processing and high volume manufacturing. Therefore, the planar coil inductor on silicon is used as an alternative due to being compatible to integrated circuit technique.

The planar inductors fabricated in monolithic microwave integrated circuit technologies make extensive use of transmission lines on silicon to realize an inductor. Actually, the inductor is a key component in many high performance wireless communication applications. However, it was concluded that use of silicon as a substrate was impractical in the radio and microwave range of frequency because of low self resonance frequency and low Q factor due to parasitic capacitance and substrate ohmic loss in transmission lines [3]. This view held until 1990 before it was shown that inductors on silicon could be used in silicon integrated circuits [4][5].

Since 1990, the characteristics of inductors fabricated with various silicon technologies have been studied and reported extensively in an effort to improve the inductor performance through a modification of the metallization, change of the geometry, and the change in the properties of the underlying substrate. The

following approaches have been employed: thicker inter-metal layer [4], thick gold metallization [5], inductor on silicon on sapphire [7], thicker metallization [5][8][9], changing of geometry [8][9][10], selective removal of silicon substrate by chemical etching [11], thick oxide for isolation [8][9][12] and fabrication using high resistivity silicon substrate [5].

This thesis confirms that inductor performance can be improved when the above approaches are combined with fabrication on a micromachined membrane. This thesis confirms this using both experimental and simulated investigations.

Chapter two discusses related studies and shows that although promising experimental and simulated results have been reported, a fundamental understanding of performance limitations of the integrated inductor is still lacking. Through studying other models, constraints of inductor performance will be discussed. The effect of modification of metallization, change of geometry and property of substrate will also be investigated to predict inductor performance.

In chapter three, to explain the effect of substrate conductivity and frequency, the physical model for an inductor on the silicon substrate is developed to include the phenomena which the previous models missed. The justification for removal of the substrate to enhance inductor performance is confirmed through the physical model and experimental investigation.

In chapter four, to improve the quality of the inductor, the micromachined inductor is fabricated on a $Si_3N_4/SiO_2/Si_3N_4$ membrane with removal of the underlying substrate by anisotropic etching. Various fabrication issues for micromachined inductors are studied. $Si_3N_4/SiO_2/Si_3N_4$ multiple stack membrane is fabricated using Low Pressure Chemical Vapor Deposition (LPCVD), and the silicon substrate is then etched anisotropically by Potassium Hydroxide (KOH). The nature of silicon anisotropic etching is discussed next. To make the coil

structure on a substrate, two techniques, metal wet etching and polyimide lift off process, are applied. These process are thoroughly investigated to fabricate the micromachined inductor.

Chapter five contains a final summary and addresses additional work needed.

Chapter 2

Review of a Planar Inductor on Silicon

This chapter reviews the silicon monolithic inductor models for describing the electrical behavior of the monolithic inductor at RF and microwave frequencies and the effect of layout geometry, metallization thickness, and substrate property on inductor performance.

2.1 Silicon Monolithic Inductor Model

A number of papers have provided an inductor model to predict inductor behaviors [9][12][13][14]. Long [10], basing his approach on Hasegawa's microstrip line model [15], showed that his model on silicon substrate is perhaps the most typical and comprehensive model.

To serve for flexible inductor design for RF and microwave application, the scalable inductor circuit models have attempted. Scalability can be defined as the electrical circuit parameters of inductor (series resistance, inductance and capacitance) can be determined from geometry and technological parameter specifications such as substrate conductivity, substrate thickness, oxide thickness for isolation, metal resistivity, and oxide and silicon dielectric constant.

Since a spiral inductor is an extension of microstrip on silicon, an inductor fabricated on silicon can be interpreted as a collection of short microstrip transmission line sections affected by the substrate and the geometry of entire inductor. Each transmission line section is electrically short in length; therefore, the resulting figure is a lumped-element model that includes series elements to model inductance and resistance per unit length and shunt elements to model the substrate parasitics and ohmic losses. These models can then be connected serially to model

the entire inductor structure. Figure 2.1 shows the typical silicon monolithic inductor model suggested by several authors. Each electrical parameter in this model is now discussed.

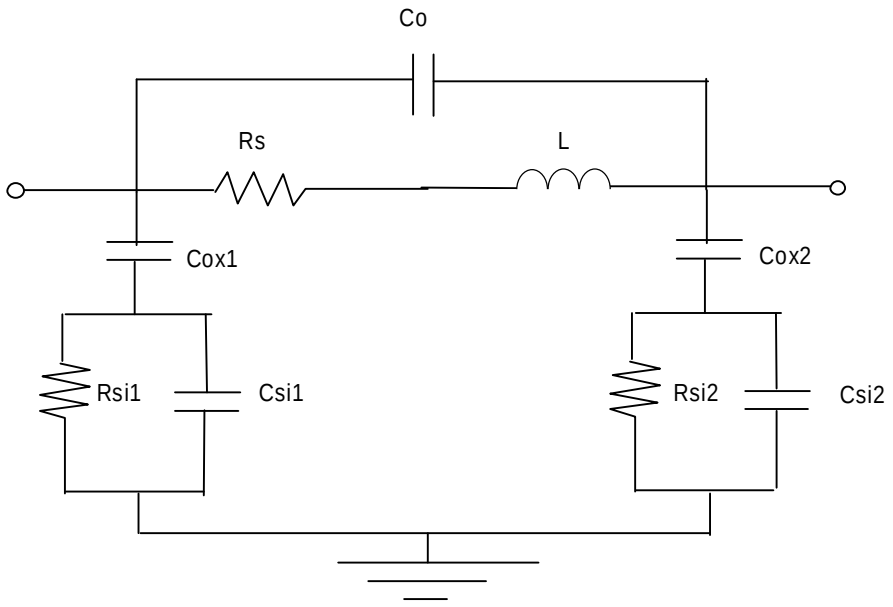


Figure 2.1 Typical silicon monolithic inductor model (*L:* Inductance; C_o: Self-capacitance; R_s: Resistance in coil, R_{si}: Resistance in silicon substrate; C_{ox}: Capacitance between coil and substrate).

2.1.1 Modeling of Inductance (*L*)

Most authors have adopted that Greenhouse inductance calculation algorithm based on Grover's model [10][12]. This model exploits the segmental approach for calculating inductance. Greenhouse used self and mutual inductance concepts to calculate the inductance of the rectangular spiral inductor.

Segmental concepts developed by Grover and Greenhouse had included the mutual inductance between conductor coils for accurate calculation of inductance [16][17]. The *mutual inductance* between two parallel segments is the flux linkage in a segment generated by a unit current in the other parallel segment or vice-versa. The *self inductance* of a segment is the mutual inductance between a segment and a parallel straight filament of infinitesimal width, spaced at the geometric mean distance of all the points of the segment from each other. The geometric mean distance (GMD) is the average of the logarithm of the distance between all the pairs of points that make up the segment. Therefore, self inductance can be considered as a special case of mutual inductance.

Based on those concepts, rectangular coils are divided into segments, and the self inductance of the individual segments is calculated. The total self inductance of the coils is the sum of the self-inductance of all the segments. The mutual inductance can be calculated between parallel conducting metal segments. However, the weak coupling between orthogonal segments is neglected since their mutual inductance is ideally zero. Coupling is zero because the mutual inductance between orthogonal segments is proportional to the dot product of the vector magnetic potential produced in each segments.

If segments have opposing currents, mutual inductance is calculated as a negative value, while the mutual inductance of segments having the same direction of currents is a positive number. The algebraic summation of the total self

inductance and the negative and positive mutual inductance is the inductance of the inductor. A schematic explanation of Greenhouse model is shown in Figure 4.2 with arrow direction corresponding to the direction of the flow of current in each segment.

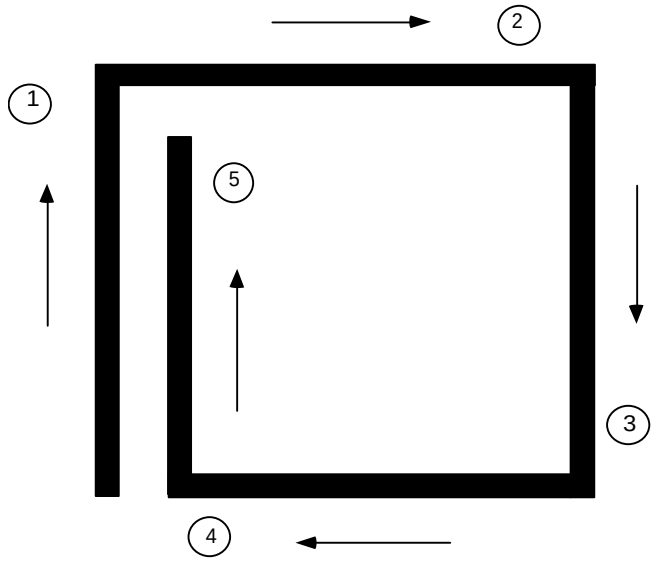


Figure 2.2 A schematic explanation of Greenhouse's model. Ref. 17

The total inductance, L_{total}, shown in figure 4.2, can be represented as [17]:

$$L_{total} = L_1 + L_2 + L_3 + L_4 + L_5 - 2(M_{1,3} + M_{2,4} + M_{3,5}) + 2M_{1,5} \ , \qquad (2.1a)$$

where L_i is the self inductance of segment '*i*' and $M_{i,j}$ is the mutual inductance between segments '*i*' and '*j*'.

Using the equation derived by Greenhouse [17], inductance can be calculated using:

$$L_i = 0.0002 l_i \left(\ln\left(2\frac{l_i}{GMD} \right) - 1.25 + \frac{AMD}{l_i} + m\frac{T}{4} \right) \tag{2.2}$$

$$M_{i,j} = 0.0002 l_i \cdot Q_i \tag{2.3}$$

$$\ln(GMD_i) = \ln(d) - \frac{1}{12\left(\frac{d}{w}\right)^2} - \frac{1}{60\left(\frac{d}{w}\right)^4} - \frac{1}{168\left(\frac{d}{w}\right)^6} - \frac{1}{360\left(\frac{d}{w}\right)^8} - \cdots\cdots \tag{2.4}$$

$$Q_i = \ln\left(\frac{l_i}{GMD} + \left[1 + \left(\frac{l_i}{GMD} \right)^2 \right]^{0.5} \right) - \left[1 + \left(\frac{GMD}{l_i} \right)^2 \right]^{0.5} + \frac{GMD}{l_i} \tag{2.5}$$

$$AMD = w + t\ , \tag{2.6}$$

where L_i is the self inductance of segment 'i', and $M_{i,j}$ is the mutual inductance between segments '*i*' and '*j*', *li* is the length of segment '*i*' in microns, *m* is the relative permeability of the conductor, *T* is the frequency correction factor(=1 for microwave frequencies), *d* is the distance between conductor filaments in microns, *w* is the width of the conductor in microns, *t* is the thickness of the conductor in microns, Q_i is the mutual inductance parameter of segment '*i*' , GMD_i is the Geometric Mean Distance of segment '*i*' , and *AMD* is the Arithmetic Mean Distance.

In most cases, the mutual inductance calculation should be performed for two segments of different lengths (j and m, where j > m). Figure 2.3 shows a case where the calculation is modified for unequal length segments.

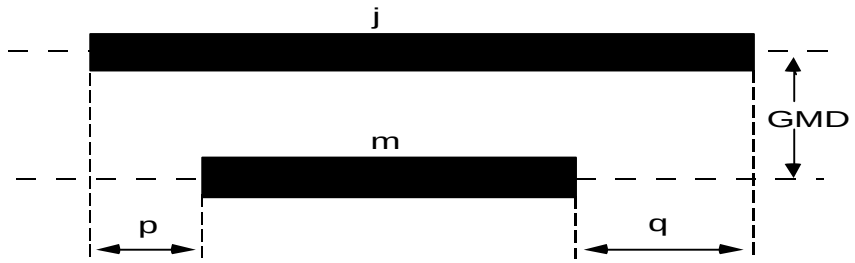


Figure 2.3 Calculation of the mutual inductance between two segments of different lengths. Ref. [17].

$$2M_{j,m} = (M_{m+p} + M_{m+p}) - (M_p + M_q), \tag{2.7}$$

where $M_{m+p} = 2(m+p)Q_{m+p}$.

However, the ideal case of the inductor in free space without ground plane was considered in the model by Greenhouse. To compensate for the ground plane, Krafesik used Greenhouse's segmental approach for imaging the spiral coil in the ground plane [18]. A reflected image in the ground plane produced by an inductor is located at twice the substrate thickness from the actual inductor. Image coils contribute a negative mutual inductance because the current flow is in the opposite direction as the inductor.

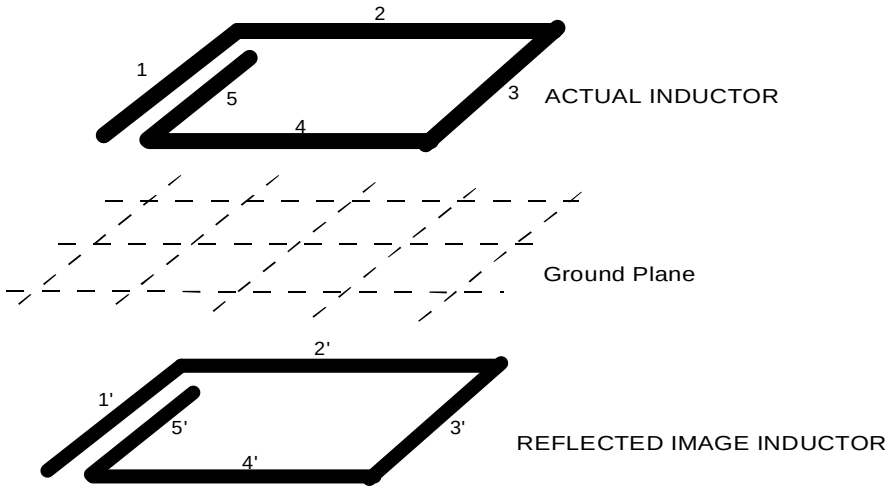


Figure 2.4 A reflected image in the ground plane produced by inductor.

Therefore, equation (2.1) should be modified to compensate for the ground plane effect

$$L_{total} = L_1 + L_2 + L_3 + L_4 + L_5 - 2(M_{1,3} + M_{2,4} + M_{3,5}) + 2M_{1,5} - (M_{1,1'} + M_{2,2'} + M_{3,3'} + M_{4,4'} + M_{5,5'}) + M_{1'5'}, \quad (2.1b)$$

where L_i is the self inductance of segment '*i*' and $M_{i,j}$ is the mutual inductance between segments '*i*' and '*j*',

Note that mutual inductance in this case is only counted once unlike the actual inductor calculation, because the image coils store half of the magnetic energy [18].

2.1.2 Modeling of Resistance in Coil (R_s)

The series resistance of the coil is the dominant electrical parameter that degrades inductor performance. At low frequencies, the resistance, R_s, is nearly the same as the DC resistance of the inductor on silicon. However, as frequency increases, the current over the conductor coil cross section tends to crowds closer to the surface due to a phenomenon known as *the skin effect*. The current is approximately concentrated near the surface over thickness corresponding to the skin depth [19]

$$d = \frac{1}{\sqrt{p \cdot f \cdot m \cdot s}} , \tag{2.8}$$

where f is the frequency, m is the relative permeability of the metal, and s is the conductivity of the metal.

In addition to the skin depth, as the frequency goes up, R_s is influenced by the substrate conductivity. Skin effect and magnetic fields influenced by substrate conductivity causes a non-uniform current flow in the inductor at high frequencies.

The frequency dependent resistance, R_s, is approximated from closed form expressions [13] proposed by Pettenpaul to represent the electrical circuit parameter in Long's model [10]. The experimental data published by Haefner [20] is used to fit the following closed formula:

$$R_s = \frac{l}{s \cdot w \cdot t}\left[\frac{0.43093 x_w}{1 + 0.041(w/t)^{1.19}} + \frac{1.1147 + 1.2868 x_w}{1.2296 + 1.287 x_w{}^3} + 0.0035\left(\frac{w}{t} - 1\right)^{1.8}\right], \tag{2.9a}$$

For $x_w < 2.5$

$$R_s = \frac{l}{s \cdot w \cdot t}\left[1 + 0.0122 x_w^{\left(3+0.01 x_w^2\right)}\right],$$

(2.9b)

where l is the length of conductor, s is the conductivity of metal, w is the width of conductor, t is the thickness of conductor, and x_w is the normalized frequency ($(2f\,sm\,wt)^{1/2}$).

In Yue's paper [12], the frequency dependent R_s, is given as follows:

$$Rs = \frac{l}{w \cdot s \cdot \left(1 - e^{-t/d}\right)}\ , \qquad (2.10)$$

where l is the length of conductor, s is the conductivity of metal, w is the width of conductor, t is the thickness of conductor, and $d$is the skin depth in the conductor.

The above closed form formulae only consider the skin effect at high frequency. To match the experimental data, some fitting parameter must be included to explain the effect of the substrate.

2.1.3 Modeling of R_{si}, C_{ox}, and C_{si}

Modeling of R_{si}, C_{ox}, and C_{si} is well established by many authors [5][7][10][12]. It originated from Hesegawa's quasi-static model [15] for microstrips over semiconducting layers that describe the impact of finite conductivity on the shunt admittance per unit length l of the transmission line. As

mentioned previously, an inductor fabricated on silicon can be interpreted as a collection of short microstrip transmission line sections.

The equivalent circuit for the substrate is C_{ox}, representing the capacitance of dielectric between the spiral inductor and substrate. The semiconducting layer is modeled as C_{si} and R_{si}. Each electrical parameter can be represented using the following closed form expressions [21].

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} w \tag{2.11}$$

$$G_{si} = \frac{\sigma_{semi}}{\varepsilon_{semi}} C_{si} \ , \qquad \text{where } R_{si} = \frac{1}{G_{si}} \tag{2.12}$$

and where ε_{ox} and ε_{semi} are the dielectric constants of dielectric layer (Silicon dioxide) and silicon substrate, respectively, t_{ox} is the thickness of dielectric material, w is the width of conductor, σ_{semi} is the conductivity of silicon substrate, and C_{si} is extracted from measured data.

Equation (2.11) assumes that the dielectric layer thickness t is much less than the microstrip width, w. For the silicon substrate, the shunt conductance G_{si} is scalable with its capacitance, since it is proportional to the area covered by the spiral conductor.

2.1.4 Modeling C_o and Other Parameters

The self capacitance, C_o, is the capacitance between each unit per length. It is quite small when compared with C_{ox} and C_{si} and can often be neglected [13] even though it can be extracted from measurement data and a parameter extraction

simulator [5][9][10]. Current crowding at the corners of a spiral inductor adds parasitic resistance, capacitance and inductance. However, this effect can be quite small and can be ignored below the low GHz frequencies range [22].

2.1.5 Modeling of Quality Factor, *Q*

The performance of an inductor can be measured by its Quality factor, *Q*, which is limited by substrate resistance loss and parasitic capacitance. *Q* is determined by the ratio of inductive imaginary component to total resistive real component of the total impedance, since measured data includes possible parasitic parameters.

Q factor can be directly extracted from a well established inductor model without significant error. The accuracy in *Q* depends on the accuracy of the inductor model. The *Q* of a typical inductor model, as shown at figure 2.1, is proposed by Long [9].

$$Q - fator \approx \frac{\nu \cdot L}{Rs + \frac{\left(\frac{\nu}{\nu_{ox}}\right)^4 \cdot Rsi}{1 + (\nu \cdot C_{ox} \cdot Rsi)}} \tag{2.13}$$

where w_{ox} is the oxide resonant frequency defined by inductance L and oxide capacitance C_{ox} ($w_{ox} = 1/(LC_{ox})^{0.5}$) .

C_o and C_{si} are ignored in this expression to simplify the resulting equation. It can be seen that decreasing C_{ox} through using thicker oxide layer results in an increased resonant frequency, causing the increase of *Q* [9].

2.2 The Effect of Layout Geometry, Metal Thickness, and Substrate Property.

2.2.1 The Effect of Layout Geometry

The key parameters in the layout geometry of a planar spiral inductor are the shape of metal line, the width of the metal line, the spacing between lines, and the number of turns. Each effect has been investigated independently in many previous work.

First of all, a planar spiral coil can have three kinds of shapes: rectangular, octagon, and circular shape. The previous work shows that the Q of an octagon and circular shaped inductor is as much as 10 percent larger than that of a rectangular shaped inductor [11]. This is because of the10% smaller resistance of circular and octagon spiral inductors that have the same inductance as a square shaped inductor. However, the circular and octagon spiral inductors introduce difficulties in photolithography and interpretation through modeling: Therefore, a rectangular spiral inductor was widely adopted in most of the previous work.

The effect of the spacing between conductor filament, the width of conductor filament, and the number of turns on the inductor performance was investigated experimentally [8][10]. Narrowing conductor filament space was found to decrease resistance (R_s) at the same inductance (L) under 1 GHz, resulting in a higher Q. When the conductor filament became wide, resistance (R_s) decreases at the same inductance (L) under 1 GHz, which also results in higher Q. However, the penalty of widening the conductor filament is to lower the resonant frequency due to increasing of the capacitance (C_{ox}). This is because C_{ox} is proportional to width of coil [10].

Increasing the number of turns with the same width of metal and spacing between segments causes in inductance to increase more slowly than the inductance in the number of turns due to negative mutual inductance. Table 2.1

shows the published data on the effect of number of turns on inductor performance [8].

Number of Turns	Peak Q- factor	Outer Length	Gap Between Opposite Sides	Total Length of Inductor
3.5	5.8	255 μm	177 μm	3.02 mm
4.5	5.7	216 μm	115 μm	2.98 mm
5.5	5.6	199 μm	75 μm	3.00 mm
6.5	5.3	191 μm	45 μm	3.06 mm
7.5	5.0	190 μm	20 μm	3.12 mm

Table 2.1 Number of turns versus the peak *Q* factor for a Constant Inductance 5nH (W = 10 μm, S = 1.5 μm) Ref. [8]

2.2.2 The Effect of Metal Thickness

The thickness of the metal influences inductor performance, as shown in intensive experimental study [5][8][9][10]. As metal thickness increases, inductance decreases in agreement with Greenhouse's inductance model. In addition, the resistance of a thick coil inductor increases more slowly than that of a thin coil inductor, resulting in higher *Q* for thick metal inductors.

2.2.3 The Effect of Changing the Substrate Property

The substrate conductor loss is well known as the main factor for degrading the inductor performance. Attempts to minimize the effect of substrate conductivity include fabrication of the inductor on silicon-on-sapphire [7],

fabrication using high resistivity silicon substrate [5], and selective removal of the silicon substrate [11]. Each of these methods attempts to make a high resistive, low lossy substrate layer underneath an inductor with resistivity value of 10^{14} ohm-cm, 200 ohm-cm, and higher than 10^{14} ohm-cm, respectively. Using these techniques, the resistance of R_s at high frequency dramatically decreases, and a high performance inductor is created.

2.3 Discussion

In the previous work, models are described using the concept of 'per unit length' as shown figure 2.1. However, as long as the Greenhouse inductance calculation method is used, the 'per unit length' presentation is inappropriate due to the nature of this algorithm. For example, if the length of the inductor coil is doubled, inductance can not double because of the logarithm for calculation and the mutual inductance between coils. If every possible geometric and physical parameter is used for the model, resistance and capacitance per unit length can be represented properly to model the inductor. Therefore, a new inductor model should be constructed for the entire structure, but it can be made up of series units, coupled to Greenhouse's model.

The fundamental understanding of resistive loss is also unclear: The inductor model for the increase of resistance with frequency caused by the skin effect and substrate conductivity has yet to be established. The model for R_s developed in the previous work is only analyzed for skin effect consideration, which results in using fitting parameters to explain the previous data and in exaggerating the increasing of R_s caused by skin effect.

By using an optimally designed inductor (optimizations of the number of turns, spacing between coils, the width of coil, and thick metallization), the best

way to improve an inductor performance is to minimize the effect of substrate. However, the demerit of fabricated inductor on silicon-on-sapphire is that it is not compatible with ordinary IC fabrication. Selective removal of silicon substrate does not remove the entire silicon substrate underneath the inductor, which can result in substrate ohmic loss and parasitic capacitance due to the remaining substrate. In addition, since the inductor was suspended on silicon, it was mechanically unstable and fragile [11]. Fabricating an inductor on a high resistivity substrate (200 ohm-cm) can be combined with common IC processing and it has satisfactory inductor performance [11]. Unfortunately, this approach costs more due to the higher resistivity substrate.

The micromachined inductor proposed in this thesis is expected to produce better performance by removing the entire silicon substrate underneath the inductor while being compatible with IC processes without substantial cost.

2.5 Summary

This chapter reviews the previous work on the well established silicon monolithic inductor model and presents promising previous experimental results. The Greenhouse algorithm is utilized for calculating inductance, and closed form expressions are also represented for calculating resistance caused by skin effect.

The effect of modification of metallization, change of geometry and property of substrate was investigated to predict inductor performance. The information discussed in this chapter provides a background for discussion of physical inductor modeling and the characteristics of inductor performance.

Chapter 3

Silicon Monolithic Inductor Modeling and Measurement

3.1 Introduction

An Inductor fabricated on silicon can be interpreted as a collection of short microstrip transmission line sections affected by the substrate and the geometry of entire inductor. This is because spiral inductor is based on the structure of a microstrip on an insulating layer on a silicon substrate with a ground plane on the back. Tuncer's quasi-static model of microstrip lines is a well- established explanation of the effect of substrate conductivity and frequency on series impedance of the microstrip [21]. However, when applying Tuncer's model for inductor modeling, three additional components should be included: DC resistance affected by geometry of coils (width, thickness, conductivity of metal, and length), frequency dependent resistance caused by skin effect on the metal conductor, and frequency independent mutual inductance from the geometry of the coils.

Resistance caused by skin effect on the coils is independent of substrate conductivity, and mutual inductance between coils is only determined by the geometry of the inductor coils. Independent investigation of the skin effect in the metal and the effect of substrate conductivity for resistive loss leads to a better understanding of how they degrade inductor performance.

3.2 Silicon Monolithic Inductor Model

The silicon monolithic inductor model combines others models: Tuncer's quasi-static model [21], Greenhouse's mutual inductance model [16], and

Kamon's skin effect model in the metal used in 'FastHenry' [23]. These models are combined to better describe the behavior of an inductor.

3.2.1 Review of Tuncer's Quasi-Static Model

The distribution of magnetic and electric fields must be considered to determine series impedance change in microstrip lines caused by substrate conductivity and frequency [15][21].

The magnetically induced currents are only effective at very high frequencies or/and high substrate conductivity levels. When the thickness of the silicon substrate becomes greater than the skin depth, it induces significant loss due to series resistance. In contrast, if the skin depth is larger than the thickness of the silicon substrate due to low frequency or/and low conductivity, the magnetic field determining the value of inductance will be decided mainly by the length, spacing, and width of the microstrip and by the ground plane.

Unlike magnetic fields, the distribution of electric fields is determined according to the frequency and substrate conductivity. If the frequency of the applied signal is less than the dielectric relaxation frequency of the silicon substrate ($f < s_{semi}/(2pe_{semi})$), the electric fields behave as if the silicon substrate were a metal sheet; therefore, capacitance can be determined by the distance of microstrip to silicon substrate, nearly independent of the distance to the ground plane.

However, if the frequency of the applied signal is larger than the dielectric relaxation frequency of silicon substrate ($f > s_{semi}/(2pe_{semi})$), the electric fields behave as if the silicon substrate were a dielectric layer, resulting in a reduced capacitance compared with the previous case.

At the crossover region where ($f \approx s_{semi}/(2pe_{semi})$), loss represented by a shunt conductance can be very large due to the impact of the substrate conductivity and frequency.

An accurate model using a non-uniform transverse cross section that takes into account the spreading of fields is shown in figure 3.1. If the effective cross section is assumed to vary linearly with depth x, approximating the spreading of the fields between the microstrip and the ground plane, the desired surface impedance can be determined from this nonuniform spreading of fields.

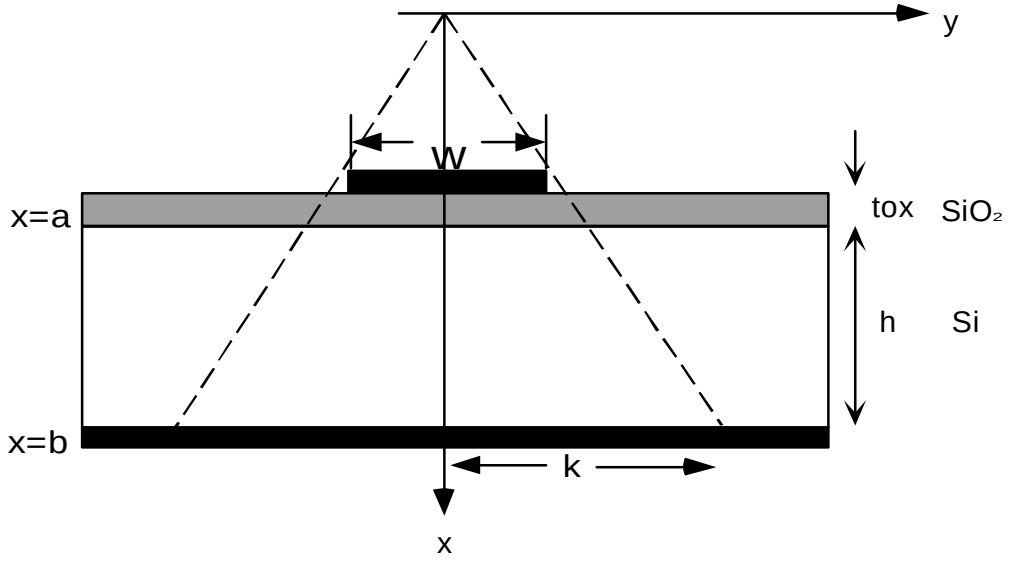


Figure 3.1 Cross section of a microstrip over a silicon substrate. K represents the effective spreading distance of the fields between the strip and the ground plane; the best agreement between this model and conventional microstrip calculation is achieved for $k=3h+w/2$ Ref. [21].

The closed form solution for series impedance on the surface microstrip can be obtained by (3.1) below, where $H_n^{(1)}$ and $H_n^{(2)}$ are Hankel functions of the first and second kind, $b = \sqrt{j2p \cdot fm_0(j2p \cdot fe_{semi} + s_{semi})}$, $k = 3h + w/2$, $a = \frac{hw}{2k - w}$, and $b = a + h$ [21]. K represents the effective spreading distance of the fields between the strip and the ground plane.

$$Z_{semi} = \frac{1}{jw}\sqrt{\frac{j2p \cdot fm_0}{j2p \cdot fe_{semi} + s}} \frac{H_0^{(2)}(jbb)H_0^{(1)}(jba) - H_0^{(2)}(jba)H_0^{(1)}(jbb)}{H_0^{(2)}(jbb)H_1^{(1)}(jba) - H_1^{(2)}(jba)H_0^{(1)}(jbb)}, \quad (3.1)$$

where h is the thickness of the silicon substrate, w is the width of microstrip, f is the frequency of applied signal, m_0 is the permeability of the silicon substrate, e_{semi} is the dielectric constant of the silicon substrate, and s_{semi} is the conductivity of the silicon substrate.

If the microstrip is on a silicon dioxide layer, the total impedance per unit length for the microstrip is [21]:

$$Z = Z_i \frac{Z_{semi} + Z_i \tanh(gt_{ox})}{Z_i + Z_{semi} \tanh(gt_{ox})}, \quad (3.2)$$

where $Z_i = \left(\sqrt{m_0 / e_{ox}}\right) / w$, $g = j2pf\sqrt{m_0 e_{ox}}$, and ε_{ox} is the dielectric constant of the silicon dioxide.

The real part of impedance represents resistance caused by the substrate conductivity, while the imaginary part of impedance divided by $2pf$ is the inductance caused by the substrate conductivity and geometry of the microstrip. Therefore, in the case of zero conductivity in the substrate, the impedance calculated using (3.1) or (3.2) should reduced to the inductance determined by the simple microstrip without resistance (R_s). The impedance calculated using the above equation is represented in the equivalent circuit model as inductance, L and resistance, R_s , respectively.

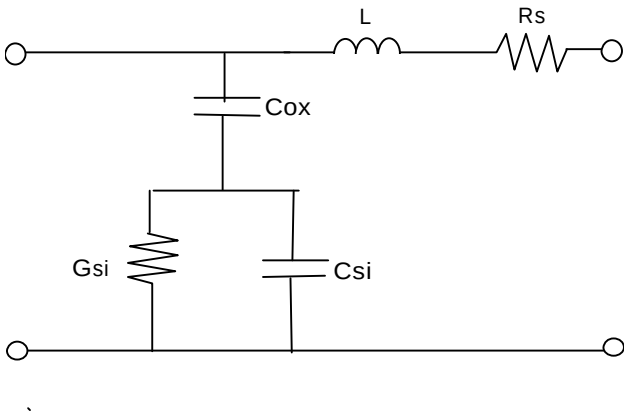


Figure 3.2 Circuit model for a microstrip line on an insulating layer on a silicon substrate with ground plane on the back.

The equivalent circuit used to find the admittance of the microstrip is shown in figure 3.2. The admittance of the microstrip consists of a capacitor, C_{ox} , standing for the dielectric layer, in series with a conductance shunted by a capacitor C_{si} representing the silicon substrate. C_{si} is dependent on the properties of the silicon substrate found using Wheeler's equations for a microstrip [21][24]. The expression for C_{ox} and G are :

$$C_{ox} = \frac{e_{ox}}{t_{ox}} w \tag{3.3}$$

$$G_{si} = \frac{s_{semi}}{e_{semi}} C_{si} . \tag{3.4}$$

The total admittance per unit length for the microstrip is given by [21]:

$$Y = \frac{jwC_{ox}G_{si} - w^2 C_{si}C_{ox}}{G_{si} + jw(C_{si} + C_{ox})} \tag{3.5}$$

where e_{ox} and e_{semi} are the dielectric constants of the dielectric layer (Silicon dioxide) and silicon substrate, respectively, t_{ox} is the thickness of the dielectric material, w is the width of the conductor, s_{semi} is the conductivity of the silicon substrate, and C_{si} is as discussed above.

In Tuncer's microstrip model, the thickness of the microstrip is not considered, since the resistance component caused by the substrate conductivity in this impedance is nearly independent of metal thickness and inductance is not much affected by metal thickness is quite small.

3.2.2 Inductor Modeling on Silicon Substrate

To apply Tuncer's model for inductor modeling, three additional components should be included: DC resistance affected by geometry of coils (width, thickness, conductivity of metal, and length), frequency dependent

resistance caused by the skin effect on the metal conductor, and frequency-independent mutual inductance between coils.

For calculating the frequency dependent resistance, the program Fast-Henry [24] algorithm is used, representing r_{metal} , Combing with R_{dc}, R_{metal} can be calculated. Frequency independent mutual inductance is calculated by Greenhouse's mutual inductance algorithm . In the end, impedance affected by substrate conductivity is obtained using Tuncer's quasi-static microstrip model.

Combining these models for the silicon monolithic inductor is justified becasue these models are independent of each other and clearly represent the various behaviors of the inductor.

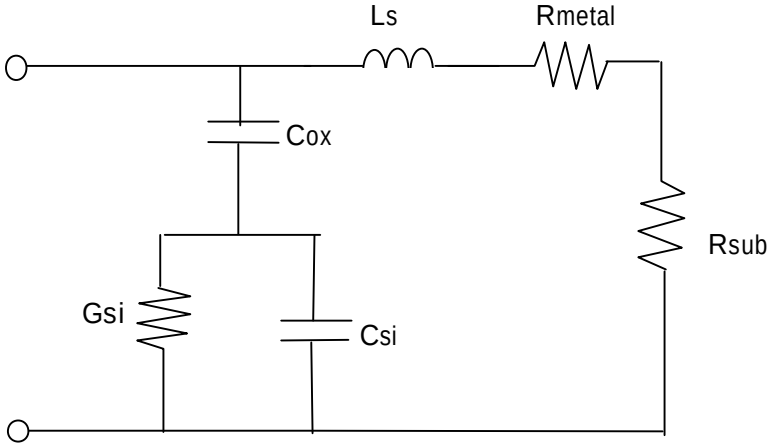


Figure 3.3 Circuit model for silicon monolithic inductor. The signal is applied between the two ports. R_{metal} is the function of the thickness (t), width (w), length (l), and conductivity (s_{metal}) of the coil and the frequency of the applied signal (f); R_{sub} is a function of the width of coil (w), the length of coil (l), the thickness of silicon substrate (h), the thickness of oxide (t_{ox}), the conductivity of substrate (s_{semi}) and the frequency of applied signal (f); L_s is a function of the width of coil (w), the spacing between coils (s), the length of coil segment 'i' (l_i), the thickness of silicon substrate (h), the thickness of oxide (t_{ox}), the conductivity of substrate (s_{semi}) and the frequency of applied signal (f).

Unlike Tuncer's model, impedance and admittance in an inductor model can not be represented as per unit length since Greenhouse's algorithm is used for calculating the mutual inductance between coils. Therefore, an inductor model should be made for the entire structure, combining the series units to make up the entire inductor. The silicon monolithic inductor model is shown in Figure 3.3.

The equations for the inductor are :

$$R_{metal} = (R_{dc} + r_{metal}) \cdot l \tag{3.6}$$

$$R_{sub} = \mathrm{Re}\left[Z_i \frac{Z_{semi} + Z_i \tanh(\gamma t_{ox})}{Z_i + Z_{semi} \tanh(\gamma t_{ox})} \right] \cdot l \tag{3.7}$$

$$L_s = \mathrm{Im}\left[Z_i \frac{Z_{semi} + Z_i \tanh(\gamma t_{ox})}{Z_i + Z_{semi} \tanh(\gamma t_{ox})} \right] \cdot \frac{l}{2 \cdot \pi \cdot f} - L_{mutual} \tag{3.8}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} w \cdot l \tag{3.9}$$

$$G_{si} = \frac{\sigma_{semi}}{\varepsilon_{semi}} C_{si} \cdot l, \tag{3.10}$$

where

$$Z_{semi} = \frac{1}{j\omega} \sqrt{\frac{j2\pi \cdot f\mu_0}{j2\pi \cdot f\varepsilon_{semi} + \sigma}} \frac{H_0^{(2)}(jkb) H_0^{(1)}(jka) - H_0^{(2)}(jka) H_0^{(1)}(jkb)}{H_0^{(2)}(jkb) H_1^{(1)}(jka) - H_1^{(2)}(jka) H_0^{(1)}(jkb)},$$

$$b_s = \sqrt{j2p \cdot fm_0\left(j2p \cdot fe_{semi} + s_{semi}\right)},\ k = 3h + w/2,\ a = \frac{hw}{2k - w},\ b = a + h$$

$$Z_i = \left(\sqrt{m_0 / e_{ox}}\right) / w,\ \text{and } g = j2pf\sqrt{m_0 e_{ox}},\ \text{and } R_{dc} = \frac{1}{wt_{metal}\, s_{metal}},$$

where e_{ox} and e_{semi} are the dielectric constants of the dielectric layer (Silicon dioxide) and silicon substrate, respectively, m_0 is the permeability of the silicon substrate, t_{ox} is the thickness of the dielectric material, w is the width of the metal, t_{metal} is the thickness of the conductor, h is the thickness of the silicon substrate, l is the overall length of coil, f is the frequency of applied signal, s_{semi} is the conductivity of silicon substrate, s_{metal} is the conductivity of metal, $H_n^{(1)}$ and $H_n^{(2)}$ are Hankel functions of the first and second kind and C_{si} is found using Wheeler's equations for a microstrip [21][24].

L_{mutual} is calculated the same way as the mutual inductance values explained in chapter 2. As long as the Greenhouse inductance calculation method is used, 'per unit length' presentation for inductance unlike other parameters is inappropriate due to the nature of this algorithm. For example, if the length of inductor coil is expanded twice, the mutual inductance can not be doubled because of the logarithm used for this calculation. Therefore, L_{mutual} is configured as the mutual inductance of the overall coil making up the inductor.

If the frequency of the applied signal reaches the resonant frequency ($f = 1/\sqrt{LC}$), the imaginary term of impedance changes from inductive to capacitive. After the resonant frequency, the coil loses its inductive characteristic.

If the parasitic capacitance in the coil is high, the resonant frequency can be lower, limiting the operating range of frequency.

Since dielectric relaxation frequency is approximately 30 GHz with the substrate resistivity of 1 ohm-cm, C_{ox} is the dominant capacitance in the model. Therefore, the resonant frequency can be approximated by $f \approx 1/\sqrt{L_s C_{ox}}$ for microwave and lower frequencies.

The Q is a measure of the efficiency of an inductor. It is limited by resistive losses (R_{metal} *and* R_{sub}) caused by the skin effect on the coil and the conductivity of the silicon substrate, and is also limited by the lowered resonant frequency affected by the parasitic capacitance. From well-established inductor models, Q can be directly extracted without significant error, determined by the ratio of inductive imaginary component to the total resistive real component of the device impedance

3.3 Model Validation

In order to verify the accuracy of the silicon monolithic inductor model, the behavior of a one turn spiral inductor predicted by its model is compared with the experimental results. Three one turn spiral inductors were fabricated on different substrates: on glass, on a silicon substrate with resistivity of 1 ohm-cm, and on a silicon substrate with resistivity of 0.005 ohm-cm. Each substrate has a thickness of about 500 μm. All coils have $l_1 = l_2 = 1000$ μm with the metal (silver) thickness of 0.9 μm and metal line of 50 μm, as shown in figure 3.4.

The model should be verified by testing at the upper limit of conductivity of the substrate and the upper limit of frequency (the range of GHz). However, due to the limitation of measuring equipment, only the high conductivity of substrate case was examined. Using the three different substrates, the effect of the substrate conductivity can be compared in the limit of zero conductivity, moderate

conductivity, and very high conductivity cases. The series resistance and the series inductance of the coils was measured for frequency from 100 kHz to 100 MHz using the HP 4194 A with the z-probe.

The measured impedance from a one turn coil on glass gives the resistance (R_{metal}) and inductance (L_s) in the case of a zero conductivity substrate, reducing to the inductance determined by the coil without substrate resistance (R_{sub}). The increase of resistance with increasing frequency is due to purely the skin effects on the metal coil itself.

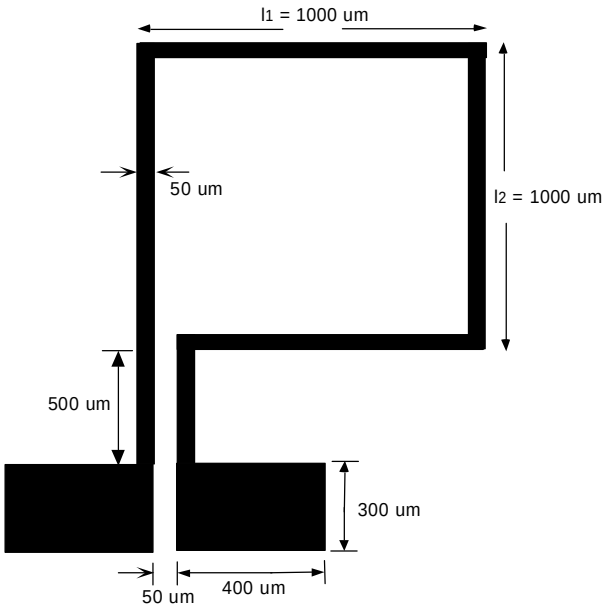


Figure 3.4 A one turn spiral inductor fabricated on three different substrates: on the glass, on the silicon substrate with resistivity of 1 ohm-cm, and on the silicon substrate with resistivity of 0.005 ohm-cm.

To compare the behavior of the one turn coil on different substrates, the measured data from the three different substrates is presented in figure 3.5. The solid lines on all the graphs correspond to the inductance and resistance of the coil on the glass, the dashed lines correspond to the substrate with resistivity of 1 ohm-cm, and the dotted lines corresponding to the substrate with resistivity of 0.005 ohm-cm.

In the measured range up to 100 MHz, only 1.9 % increase of resistance is shown from DC resistance to 100 MHz. At 100 MHz the skin depth in silver is 6.34 μm, compared the thickness of 0.9 μm. If a higher frequency were applied, more increase in resistance would be expected, caused by the skin depth in the metal.

In the case of the one turn coil on the silicon substrate with non-zero conductivity, the real part from the measured impedance consists of R_{metal} from skin effect in the metal and R_{sub} from the substrate conductivity. R_{metal} and R_{sub} can not be separately determined in the measurement. However, the difference of resistance measured between coil on the glass and coil on the silicon substrate with the conductivity can be attributed to as R_{sub}, caused by the conductivity of substrate, because the increase of resistance caused by the skin effect can only be seen on the coil on the glass.

When a substrate with resistivity of 1 ohm-cm is used for fabricating the one turn coil, a 10.5 % increase of resistance occurs between the DC resistance and resistance at 100 MHz. The higher the conductivity of substrate, the larger the resistance. In case of the substrate with the resistivity of 0.005 ohm-cm, a 16.8 % increase in the resistance is measured from DC resistance to 100 MHz.

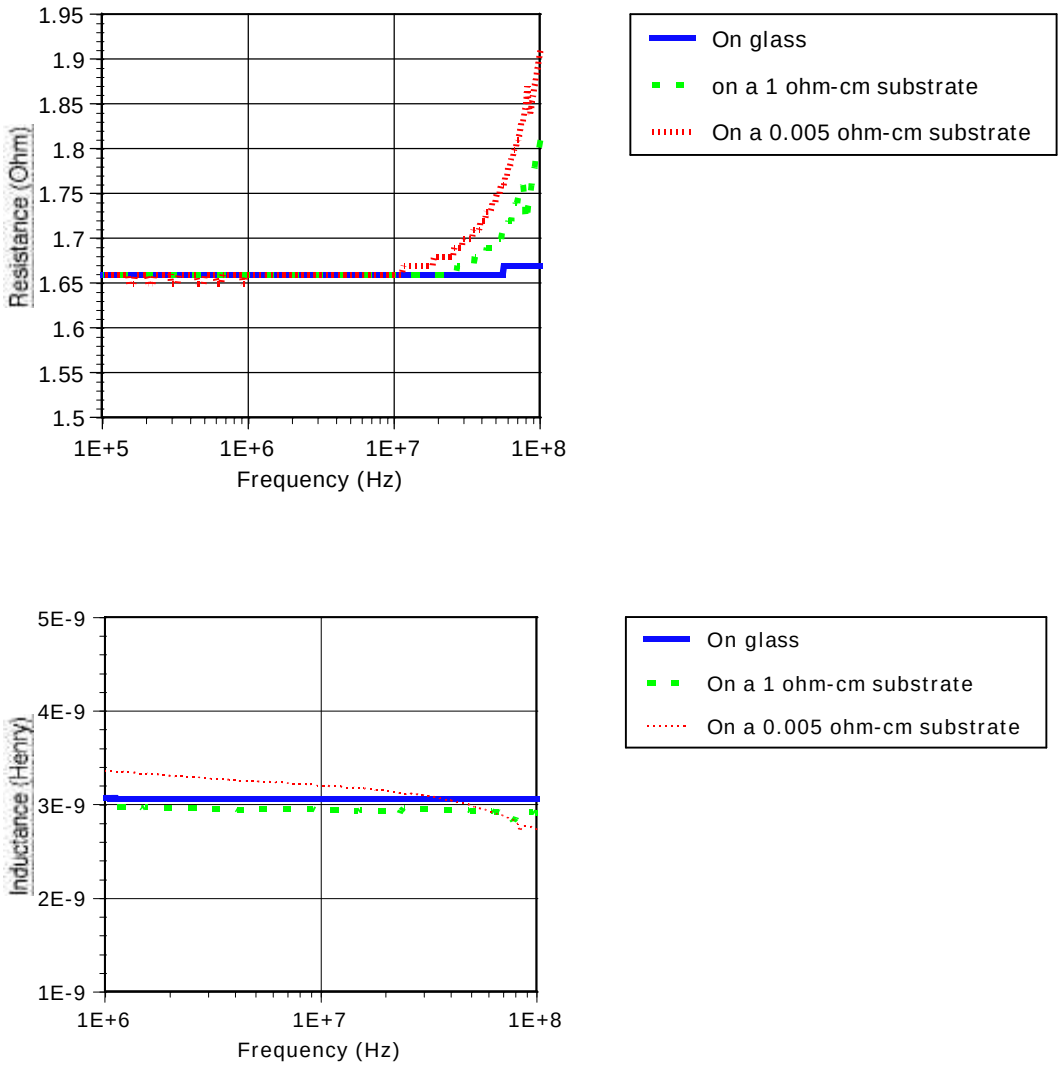


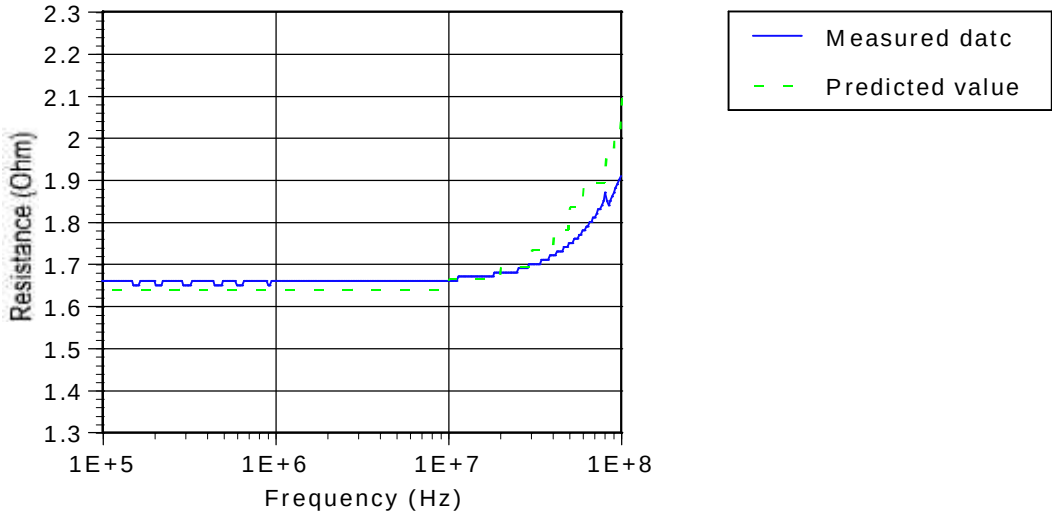
Figure 3.5 The comparison between the measured impedance on three different substrates: on glass, on a silicon substrate with resistivity of 1 ohm-cm, On a silicon substrate with resistivity of 0.005 ohm-cm.

Inductance changes 1.7% in the coils on glass and on the substrate with the resistivity of 1 ohm-cm, with increasing the frequency from DC to 100 MHz. The measured inductance in the both cases shows similar results. However, in the case of high conductivity (the substrate with resistivity of 0.005 ohm-cm), inductance is changed more with increasing frequency.

The comparison of impedances of the inductors is shown in figure 3.6 and table 3.1 to verify the model. The solid lines on all the graphs correspond to the inductance and resistance of the coil from the measured data, using the substrate with resistivity of 0.005 ohm-cm. The dashed lines correspond to the predicted values based on the model. The measured data is adjusted to the calculated DC value for comparison of resistance according to the frequency dependent change. Therefore, the difference between data at 100 MHz is not from noise or wrong calibration , but from the change of resistance with increasing frequency.

The resistivity of substrate	*Resistance* extracted from Measurement			*Resistance* predicted from Model		
	R_{metal}	R_{sub}	R_{total}	R_{metal}	R_{sub}	R_{total}
Infinity	1.67 Ω	0 Ω	1.67Ω	1.65 Ω	0 Ω	1.65 Ω
1 ohm-cm	1.67 Ω	0.14 Ω	1.81 Ω	1.65 Ω	0.072Ω	1.73 Ω
0.005 ohm-cm	1.67 Ω	0.24 Ω	1.91 Ω	1.65 Ω	0.443Ω	2.10 Ω

Table 3.1 The comparison of R_{metal} and R_{sub} between the measured and predicted impedance at 100 MHz. The extracted DC resistance is 1.64 Ω and the difference between DC value and R_{metal} is the increase of resistance caused by the skin effect in the metal.



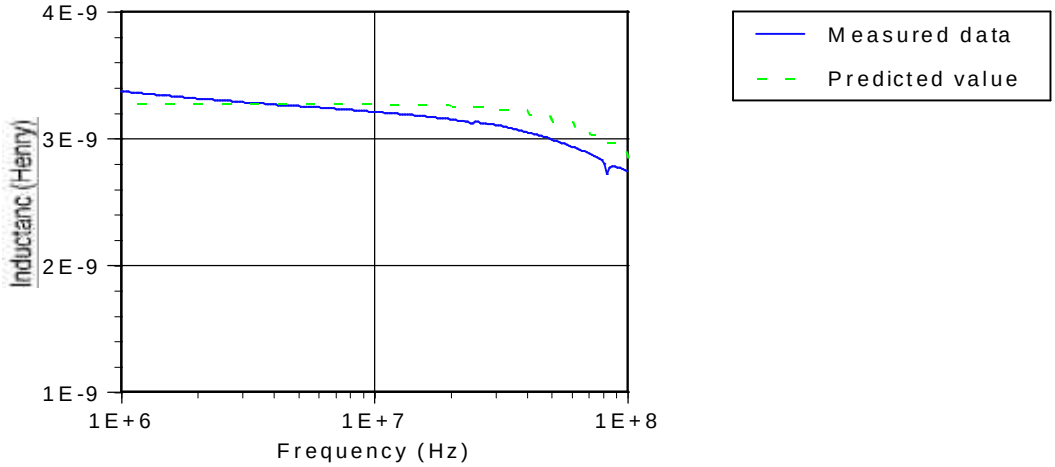


Figure 3.6 The comparison between measured and predicted impedance for a one turn coil on a silicon substrate with resistivity of 0.005 ohm-cm.

The resistance calculated in this model matches the experimental measurement closely within 9% over the range of measured frequency and for different conductivity of substrates. The predicted inductance also matches the measured values very closely within 4 % over the same ranges.

Therefore, it can be said that the conductivity of the substrate influences the performance of the inductor through its resistive loss and inductance decrease, according to both the predicted and experimental results. As seen in both predicted and experimental results, inductance decrease with increasing frequency is not significant above the resistivity of 1 ohm-cm substrate, which is commonly used in IC processing. Inductance decrease is not problematic in inductor performance in microwave circuits. To the contrary, resistive loss is significant even for a 1 ohm-cm substrate due to the conductivity of the substrate.

By removing the substrate, the resistive loss caused by the substrate can be eliminated and the resonant frequency also can be increased by minimizing the parasitic capacitance generated by the substrate. Removing the substrate is a good approach to build a high performance inductor.

3.4 Result of measurement on the inductor and Discussion

The micromachined inductor was fabricated on the membrane by removing the substrate underneath the inductor. To compare inductor performance, three additional inductors were fabricated on glass, on a silicon substrate with resistivity of 15 ohm, and on a silicon substrate with resistivity of 0.005 ohm.

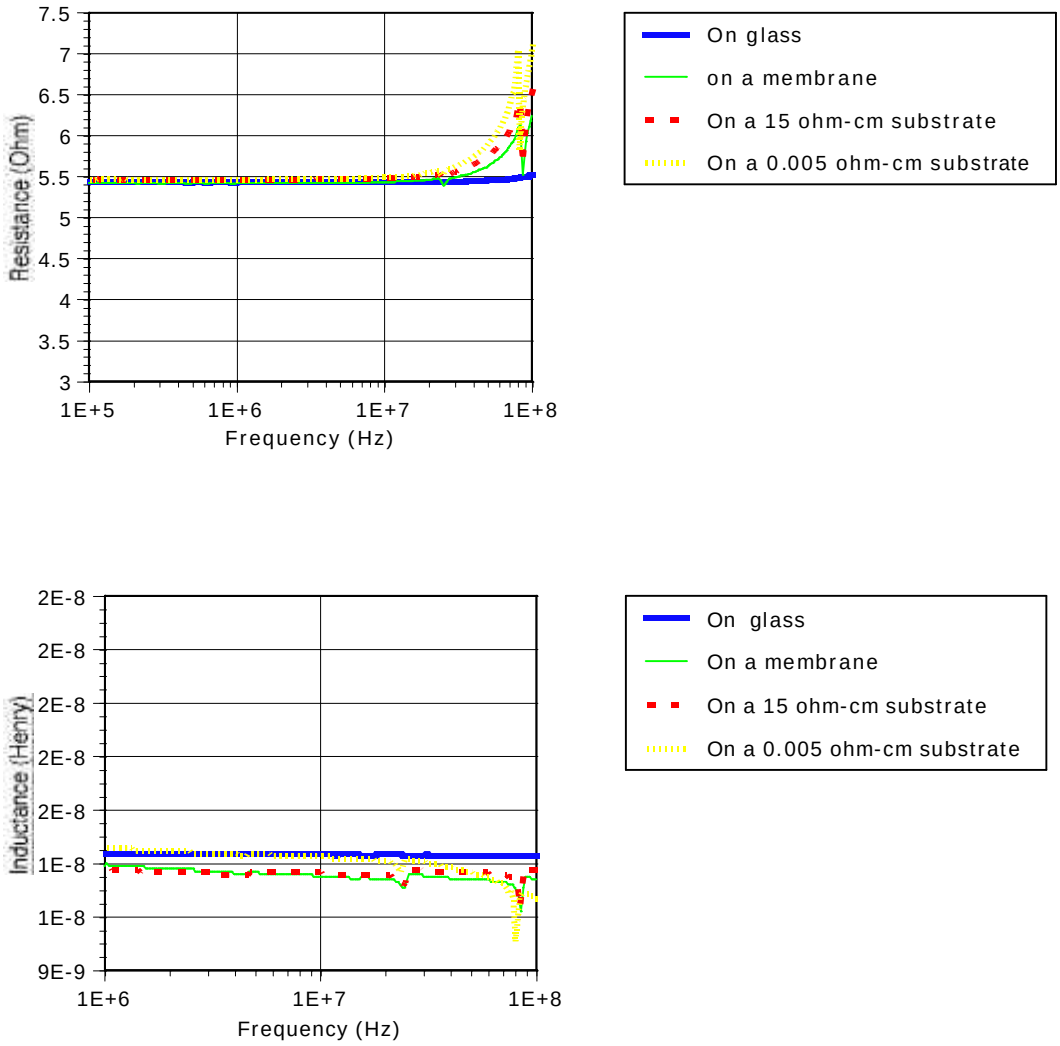


Figure 3.7 The measured impedance of different inductors on glass, a micromachined membrane, a 15 ohm-cm substrate, and a 0.005 ohm-cm substrate.

The measured impedance of the different inductors on glass, the micromachined membrane, a 15 ohm-cm substrate, and a 0.005 ohm-cm substrate is shown in figure 3.7. The inductor fabricated on glass is the ideal case of a substrate without losses. Measuring the inductor on glass, the resistive loss caused by the skin effect in the metal can be determined.

In the micromachined inductor, since the silicon substrate is removed, the model established in this study can be simple and the parameters in the model can be reduced to R_{metal}, and L_s. The physical meaning of removing the substrate is to provide a high resistivity substrate, almost infinity (the zero conductivity), underneath the inductor. It results in reducing the resistive loss due to the conductivity of the substrate. However, in reality, the metal lines on the substrate are needed as interconnects between the inductor and other components. Thus, the model proposed in this study is meaningful because the effect of the substrate conductivity with frequency is clearly defined and proven.

In the measured range of frequency, the enhanced performance of the inductor can be seen only between the inductor on the membrane and on the 0.005 ohm-cm substrate. If higher frequency (in the range of GHz) of signal were applied, the enhanced performance of the inductor would be more clearly seen based on the predicted model and on previous results [5][9][11][12] by reducing the resistance (R_{sub}) and the parasitic capacitance.

3.5 Discussion

Inductance is treated in other studies as a constant nearly independent of the frequency of the applied signal because the range of the resistivity of the silicon

substrate used is above 1 ohm-cm, which is common for substrates used in IC processing. Under that range, the inductance value is shown as remaining constant until reaching the resonant frequency. The calculation from the Greenhouse model, which analyzed inductance in air, does not deviate as much in measured results since the resistivity of substrate used is above 1 ohm-cm.

Therefore, resistive loss caused by the conductivity of the substrate is a significant factor in degrading inductor performance. The understanding of the resistive loss for inductor performance is not clearly investigated in previous work. In this study, by separating the investigation of the skin effect on the metal and the effect of substrate conductivity on resistance loss, it is possible to have a clear understanding of how inductor performance is degraded by substrate conductivity.

High frequency (above 100 MHz) is not tested due to limitation of measuring equipment used. Resonant frequencies located above 100 MHz can not determined through measurement. Also, even though the proposed model is confirmed with the experimental results up to 100 MHz, it is still importanct to verify the model in the range of GHz for microwave application.

3.1 Summary

A silicon monolithic inductor model was presented based on Tuncer's quasi-static model, Greenhouse's mutual inductance model, and Kamon's skin effect model for metal used in 'Fast-Henry'. Tuncer's quasi-static model is reviewed to explain the inductor model.

The resistance calculated in this model matches the experimental measurement closely within 9% over the range of measured frequency and the different conductivity of substrate. The predicted inductance also matches the measured values very closely within 4 % over the same ranges.

The measured impedances of inductors on the different substrates were also compared show that the micromachined inductor has better performance than the others.

Chapter 4

Fabrication of Micromachined Inductor

4.1 Process for Planar Membrane Fabrication

The planar membrane is built using bulk micromachining technique, in which the substrate beneath the inductor is removed. Contrary to conventional hybrid micromachined inductors [1][2], this approach allows monolithic integration of an inductor with other components.

The dominant process for removing the silicon substrate in bulk micromachining is to use a wet anisotropic silicon etching which is crystal orientation dependent. Many anisotropic etchants can be used for silicon, such as EthyleneDiamine Pyrocatechol (EDP), Potassium Hydroxide (KOH) and Cesium Hydroxide (CsOH) [3][24]. KOH is more frequently used for anisotropic etching because it exhibits much higher anisotropic (100)-(111) etch ratio (400:1) than the others[25]. Depending on the choice of etchants, silicon dioxide or silicon nitride can be used as an etch mask, since a photoresist is easily peeled off at on early stage of etching and also can not endure long wet etching at high temperature.

If KOH is used, silicon dioxide is not suitable for etch masks because it is less selective to silicon. Silicon nitride made by Low Pressure Chemical Vapor Deposition (LPCVD) can endure for long times (several hours) in KOH solution as a mask. However, silicon nitride made by Plasma Enhanced Chemical Vapor Deposition (PECVD) is less selective compared with silicon nitride made by LPCVD. The etching rate of silicon nitride made by LPCVD is observed to be about 10 Å/hour, while that of silicon nitride made by PECVD is approximately

400 Å /hour. PECVD silicon nitride is unsuitable as a mask for removing the entire substrate (350μm -500μm) underneath the membrane.

In addition to the selectivity of the dielectric, the mechanical stability should also be taken into account. The dielectric should not buckle or crack because of stresses (tensile stress and compressive stress). To minimize these stresses, a multiple film stack of two silicon nitride layers cladding a silicon dioxide layer (Si_3N_4-SiO_2-Si_3N_4 multiple stack layers) is used as a membrane. The thickness of each layer is carefully chosen for mechanical stability.

Figure 4.1 shows a schematic drawing of the fabrication procedure of a planar membrane. 4-inch single crystal (100) double polished silicon wafers are used as substrates. The wafers are 500 μm thick with the resistivity of 1-5 ohm-cm and 0.005 ohm-cm. A 8000 Å thick silicon dioxide layer is sandwiched between two 1500 Å thick silicon nitride layers on the double-side polished wafer, all deposited by LPCVD. Silicon nitride is deposited in a reaction of ammonia (NH_3) and dichlorosilane ($SiCl_2H_2$) at a gas flow of 3.5:1 at 830 °C and 315mTorr. Silicon dioxide is deposited in a reaction of silane (SiH_4) and oxygen (O_2) at a gas flow rate of 1:10 at 460° C and 110 mTorr.

After depositing a multiple film layer on a wafer, the dielectric film stack on the back side of the double polished wafer is patterned and plasma etched. Before the plasma etching, the wafer must be coated with photoresist on the front side of the wafer to avoid unintentional etching. The plasma etching of the silicon dioxide and silicon nitride layers is performed by using CF_4 and O_2 with 100 watts power. The etch rate of silicon dioxide and silicon nitride is observed to be about 700 Å /min and 1000 Å /min, respectively. The remaining back-side multi-layer stacks become a masking layer for the subsequent wet KOH silicon anisotropic etching.

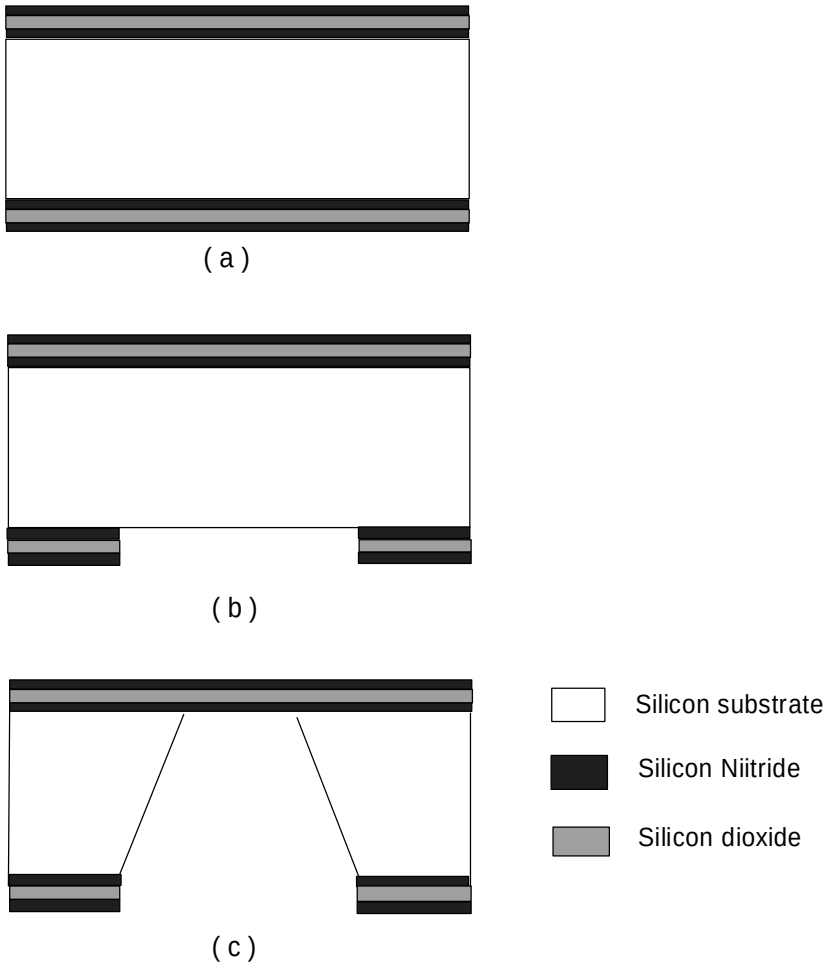
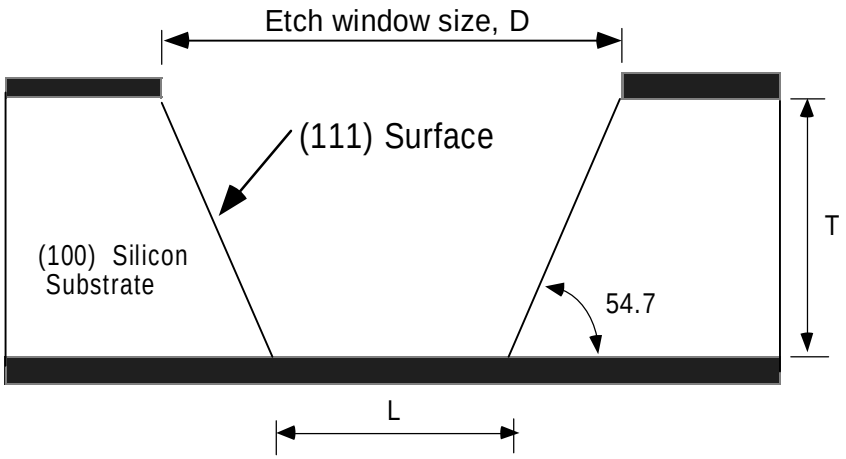


Figure 4.1 Schematic view of fabrication procedure of planar membrane: (a) Depositing silicon nitride, silicon dioxide, and silicon nitride by LPCVD; (b) Patterning and plasma etching on the back side of wafer; (c) Anisotropic etching using KOH at 100 ^{0}C.

The silicon substrate is anisotropically etched using 40% KOH solution (Silicon etchant PSE-200) at 100° C. The etch rate of the (100) silicon is about 1 μm/min at 100° C. The etch rate is critically dependent on the solution temperature; therefore, the high stable temperature should be maintained during etching for minimizing the etch time.

Figure 4.2 shows a cross section of an anisotropically etched (100) silicon substrate in detail. Due to the orientation dependency of the etch rate, the etched surface is bounded by the (111) planes, which have the slowest etch rates. The final length of the square dielectric membrane is determined by the etch time and the thickness of the silicon wafer since the etching produces (111) planes as the side walls at an angles of 54.7° [3].



D: Etch window size T: Thickness of wafer L: Final dimession

Membrane as etch mask

Figure 4.2 Cross section of an anisotropically etched (100) silicon substrate with Si_3N_4-SiO_2-Si_3N_4 membrane layers.

The relation to obtain the final length of the square dielectric membrane (L) is:

$$D = \frac{T}{Tan(54.7^{\circ})} \bullet 2 + L \qquad (4.1)$$

where T is silicon substrate thickness, L is the desired final size of the membrane, and D is the etch widow size for patterning.

Both a circular pattern and square pattern produce a square hole. If a circular pattern is used, it automatically aligns in the [110] direction on (100) plane silicon wafer. In case of square pattern, alignment of the patterns in the [110] direction on the surface of the silicon substrate must be confirmed to avoid unwanted overhang.

The formation of the membrane structure should be followed by a cleaning procedure for subsequent metallization for the inductor.

4.2 Process for Inductor Fabrication

Two different techniques are used to fabricate a planar inductor with approximately 9000Å thick silver on the membrane. The metal wet etching approach is investigated first and metal lift off with polyimide is then reviewed. Other approaches include Positive tone Reverse Gradient of Slope (PREGOS) and Chlorobenzene metal lift off. But, these processes do not provide easy processing and maximum yield [26].

Since the spiral coil structure needs a bridge to connect the center of the coils to the interconnects, two levels of metal separated by an inter-metal dielectric are needed. Several inter-metal dielectric materials such as silicon dioxide, silicon nitride, photoresist, and polyimide can be used. Among these materials, polyimide can be easily used on the silver evaporated layer since it has an appropriate thermal budget. However, for convenience, photoresist is used as an inter metal dielectric material here.

4.2.1 Metal Wet Etching Process

The metal wet etching process is a common process for patterning the metal interconnection layer in IC fabrication.

First, a thick silver layer on thin chrome is evaporated on a silicon substrate with a membrane. Then, the lithography process is applied for metal wet etching on the surface of evaporated metal layers. Since the metal layer consists of two different metals, chrome etchant (Transene Type 473) and silver etchant (Transene Type TFS) are used to make the first layer of the coil structure.

Silver evaporation is done on the micromachined structure in a vacuum system at a pressure of lower than $5x10^{-6}$ Torr. However, silver itself does not stick well on the sample. Without the chrome layer beneath the silver layer, the metal layer can be easily washed off even during the subsequent cleaning and drying process. Also, if the thickness of the chrome layer is below 150 Å , the pad where the probe lands is very easily peeled off during electrical measurement . A chrome rod is evaporated thermally to produce a thickness of 200 Å at a deposition rate of 5-10 Å /sec, followed by 8000Å thick silver at a deposition rate of 15-20Å /sec.

An Inficon crystal monitor is used to measure the real time deposition rate and thickness. 9000Å thick silver is evaporated in two or three steps to prevent the vacuum chamber from getting overheated. The Inficon measurement is taken during evaporation and the thickness of the evaporated chrome and silver is verified with an Alpha Step Profiler.

In general, the lithography process starts with the cleaning of the surface of the evaporated sample. The sample is first rinsed with acetone, then rinsed in methanol and de-ionized (DI) water for 1 minute, respectively. However, ultrasonic cleaning must be avoided when the inductor is fabricated on a membrane since it breaks the membrane easily.

Dehydration bake should be applied to remove the residual moisture at a temperature of 125 °C for 10 minutes in a convection oven after wet processing. An adhesion promoter (Microposit Primer) and a positive photoresist (AZ 5214-E) are spun on the sample at 3500 rpm for 40 second, which results in the 1.7 μm thick photoresist coating. The sample is then pre-baked for drying and hardening in a convection oven at 90° C for 10 minutes. An HTG UV-lamp mask aligner is used to expose the sample for 45 seconds, having aligned with the mask at a wavelength of 370nm with a constant intensity of 2.1 mW/cm^{-2}.

The sample is then developed in Microposit Developer 425 for approximately 45 seconds under mild agitation, and then rinsed immediately with DI water. After drying the sample, the pattern is inspected under a microscope. In the convection oven, post bake is performed at 110°C for 5 minutes to harden the photoresist and to improve adhesion of the photoresist to substrate for later wet etch steps. This post bake must be minimized for easy removal of the photoresist for subsequent metal interconnect.

Chrome and silver are etched with Chromium etchant (Transene Type 473) and Silver etchant (Transene Type TFS). To etch the silver first, care should be taken to control the etch time since the etch rate of silver is so fast, which may result in an undercut. The silver etchant used has an etch rate 200Å /sec; therefore, the etch time is approximately 45 seconds at room temperature. The sample is rinsed in DI water to remove all remaining silver etchant. The remaining chrome layer is dipped into chrome etchant at over 40°C. Since chrome is etched in a few seconds, the sample should be removed from the etchant immediately as soon as dipping into the etchant results in bubble formation which is an indication of the ending of the etching process.

A chemical etching reaction is not easily produced under 30°C. After chrome etching, the remaining photoresist is removed by using photoresist stripper (AZ 400T) instead of acetone. Since high temperature baking is applied for adhesion, AZ 400T is more effective than acetone in removing photoresist. The residual photoresist in contact with second metal interconnect will degrade the inductor performance.

For inter-metal dielectric material, the 5214-E photoresist is spun on the sample twice at 3000 rpm for 30 seconds, resulting in a 2 μm thick photoresist. The sample is then pre-baked in the oven for 10 minutes at 90° C and exposed in the HTG Aligner for 150 seconds at 2.1 mW/cm^2 UV light intensity with contact mask. The sample is developed for 70 seconds.

The second metal layer is evaporated on the prepared sample. Unlike the first metal layer, it is not necessary to use chrome for the purpose of adhesion since silver itself sticks quite well to the photoresist. The 9000 Å thick silver is evaporated in two or three steps to prevent the vacuum chamber from getting overheated.

After metallization, the same wet metal etching process for silver is used to fabricate the micromachined inductor. Figure 4.3 shows the micromachined inductor on a membrane made with metal wet etching process.

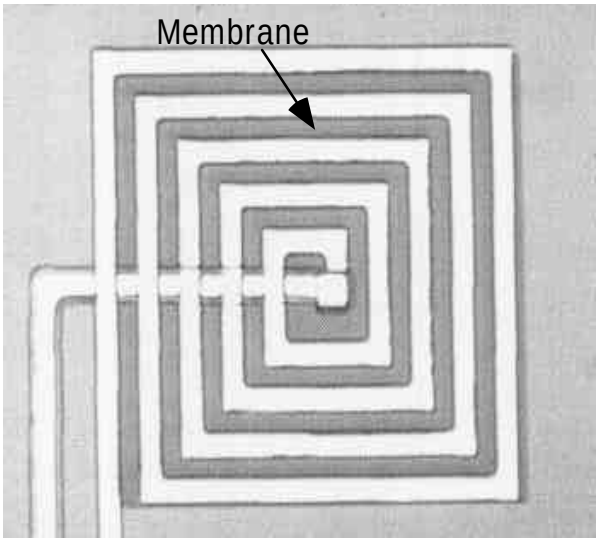


Figure 4.3 The micromachined inductor on a membrane made by metal wet etching process. The dark square is the membrane with silicon substrate removed from underneath inductor.

4.2.2 Polyimide Metal Lift Off Process

Sandra [27] reported that a high yield can be achieved by simply adding, spinning and baking the polyimide. Epo-Tek 600-3, a single component polyimide is used in this metal lift off process. Epo-Tek 600-3 has a low solubility in aqueous type developer, like 5200-series photoresist developer, MIF 425.

Figure 4.4 shows a schematic drawing of the polyimide metal lift off process. Processing starts with the cleaning of the sample's surface, similar to the metal wet etching process. The dehydration bake should be applied to remove the residual moisture at 125 °C for 10 minutes in a convection oven after wet processing.

The polyimide solution(Epo-Tek 600-3) without dilution is spun on the sample at 2000 rpm for 30 seconds and then cured moderately hard. The polyimide is cured by baking it at 125° C for 15 minutes in a convection oven. Curing time is critical to etch the polyimide by developer. Deviation of plus or minus 5° C will affect the etch rates of the polyimide. Higher temperatures will more completely imidize the polyimide, slowing the etch rate, while lower temperature will not imidize as much , speeding up the etch process.

After the polyimide is baked, the 5214-E photoresist is spun on the sample at 3500 rpm for 40 seconds. No adhesion promotor or primer is required because the photoresist itself sticks to cured polyimide very well. The sample is then prebaked on a hot plate in the oven for 90 seconds at 90° C. It is then exposed in the HTG Aligner for 45 seconds at 2.1 mW/cm^2 UV light intensity. Development time is very critical for this method.

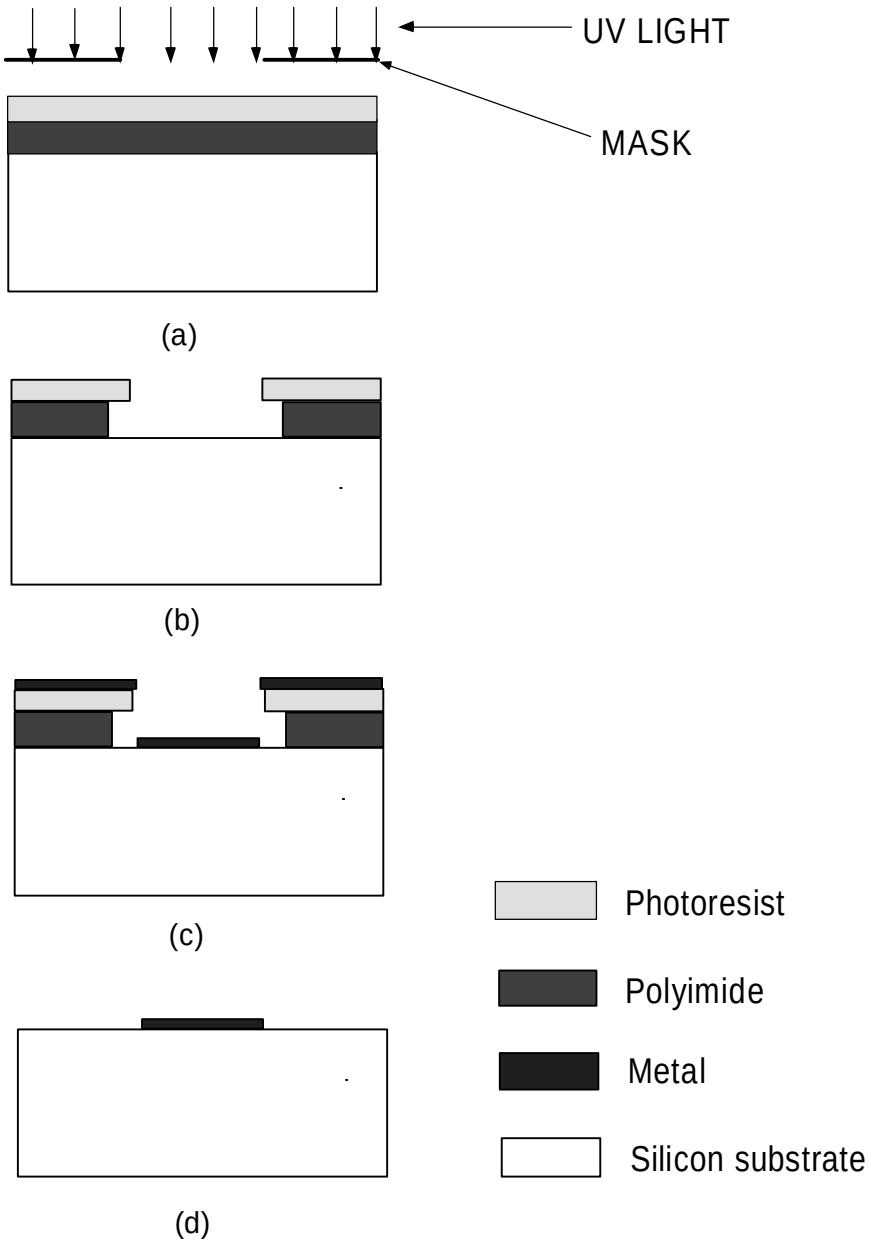


Figure 4.4 Sequence of polyimide metal lift off process : (a) UV exposure on polyimide and resist coated substrate; (b) Developing causes undercut in the

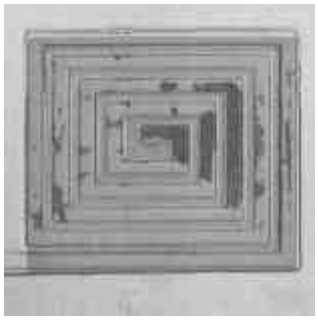
polyimide layer; (c) Metallization; (d) Removing resist-metal layer by acetone and dissolving the remain polyimide by developer.

The developer (MIF 425) not only removes the exposed region of the photoresist but also slowly starts to etch the underlying polyimide as soon as all the exposed region of the photoresist is removed. The lateral undercut of polyimide in the developer solution is nearly the same as its vertical etch depth.

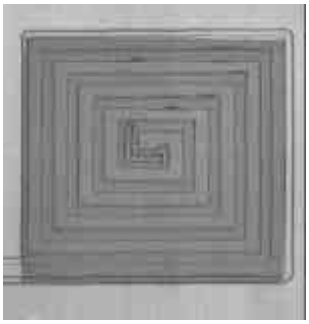
As a result, after the development, the resist layer forms an overhang pattern. The development time is critical in this case, and after the pattern becomes visible in the developer, it takes an additional 3-5 seconds for the optimum undercut in the polyimide. The sample is then checked under a microscope, and if properly developed, a small area of undercut can be distinguished by its different color. The optimum lateral undercut of polyimide measures approximately 1 μm; a smaller than 1 μm undercut does not produce a good lift off, whereas a larger one may destroy the resist pattern. Figure 4.5 shows the different resist patterns coming from developing time. In the figure (a), residual polyimide is not removed completely because of short developing time. In the figure (b) and (c), overdeveloping destroys the resist pattern.

Metallization is done with same procedure as is used in the metal wet etching process. 200 Å of chrome followed by 9000 Å thick silver is thermally evaporated. After the metallization, the sample is immersed in acetone for metal lift off, where acetone dissolves the photoresist and thus removes the metals on the top of that photoresist. As acetone slowly etches the polyimide, only a small portion of polyimide is removed, leaving behind most of the polyimide. The sample is rinsed in MIF 425 developer and DI water for subsequent removal of all polyimide.

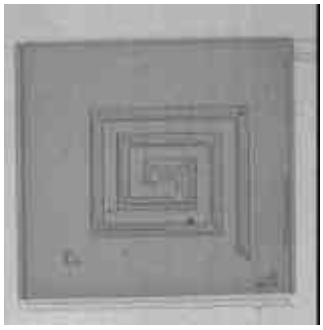
The same procedures are applicable to interconnect metallization as in the wet metal etching process. The inductor shown in figure 4.3 can be fabricated in this way.



(a)



(b)



(c)

Figure 4.5 Resist pattern caused by developing for polyimide lift off process: (a) polyimide residual in resist pattern because of short developing time; (b) Some loss

of resist pattern caused by overdeveloping; (c) Totally destroyed resist pattern by excessive developing.

4.3 Summary

The detail of fabrication procedures and issues for the micromachined inductor have been presented in this chapter. By adopting bulk micromachining technique, the multiple dielectric membrane containing the inductor was fabricated with the silicon substrate removed by using KOH anisotropic etching. Some relevant KOH etching issues were mentioned.

On the membrane, the inductor was fabricated with two ways: metal wet etching process and polyimide lift off process. Polyimide lift off process was investigated in detail.

Chapter 5

Summary and Conclusion

The Q is a measure of the efficiency of an inductor. It is limited by resistive losses (R_{metal} and R_{sub}) caused by the skin effect on the coil metal and the conductivity of the silicon substrate and by the lowered resonant frequency affected by the parasitic capacitance.

To improve inductor performance, a micromachined inductor was built using the bulk micromachining technique. By removing the substrate using KOH, the resistive loss caused by the substrate can be eliminated, and the resonant frequency can also be increased through minimizing the parasitic capacitance generated by the substrate. Removing the substrate is a good approach for fabricating a high performance inductor compatible with IC processing.

To quantify the effect of the substrate conductivity, this work proposes a silicon monolithic inductor model based on Tuncer's quasi-static model, Greenhouse's mutual inductance model, and Kamon's skin effect model for metal used in 'Fast-Henry'.

Even though the high limit of substrate conductivity and the high limit of frequency range of GHz should be tested for model validation, the case of high frequency was not tested due to limitation of measuring equipment. Using different substrates, the effect of the substrate conductivity was compared in terms of zero conductivity, moderate conductivity, and very high conductivity cases.

The resistance calculated in this model matches the experimental measurement closely within 9% over a range of the measured frequency and the

different conductivity of substrates. The predicted inductance also matches the measured values very closely within 4 % over the same ranges.

In the measured range of frequency, improved performance of the micromachined inductor can be seen compared with that of an inductor on the silicon substrate with resistivity of 0.005 ohm-cm. If higher frequency in range of GHz of signal were applied, improved performance of the inductor should be even more evident based on the predicted model by reducing the resistive loss caused by the conductivity of substrate and the parasitic capacitance.

The experiment confirms the proposed model is accurate up to 100 MHz ; additional research is needed to verify the model is accurate above 100 MHz. In addition, the procedures for optimizing Q factors in the inductor design need to be further developed.

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